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1988

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Memory Overview 1

CHAPTER 1: MEMORY OVERVIEW

MEMORY BACKGROUND AND DEVELOPMENT

Only fifteen years ago MOS LSI memories were little more than laboratory curiosities. Any engineer brave enough to design with semiconductor memories had a simple choice of which memory type to use. The 2102 Static RAM for ease of use or the 1103 Dynamic RAM for low power were the only two devices available. Since then, the memory market has come a long way, the types of memory devices have proliferated, and more than 3,000 different memory devices are now available. Consequently, the designer has many to choose from but the choice is more difficult, and therefore, effective memory selection is based on matching memory characteristics to the application.

Memory devices can be divided into two main categories: volatile and non-volatile. Volatile memories retain their data only as long as power is applied. In a great many applications this limitation presents no problem. The generic term random access memory (RAM) has come to be almost synonymous with a volatile memory in which there is a constant rewriting of stored data.

In other situations, however, it is imperative that a non-volatile device be used because it retains its data whether or not power is applied. An example of this requirement would be retaining data during a power failure. (Tape and disk storage are also non-volatile memories but are not included within the scope of this book, which confines itself to solid-state technologies in IC form.)

Thus, when considering memory devices, it's helpful to see how the memory in computer systems is segmented by applications and then look at the state-of-the-art in these cases.

Read/Write Memory

First examine read/write memory (RAM), which permits the access of stored memory (reading) and the ability to alter the stored data (writing).

Before the advent of solid-state read/write memory, active data (data being processed) was stored and retrieved from non-volatile core memory (a magnetic-storage technology). Solid-state RAMs solved the size and power consumption problems associated with core, but added the element of volatility. Because RAMS lose their memory when you turn off their power, you must leave systems on all the time, add battery backup or store important data on a non-volatile medium before the power goes down.

Despite their volatility, RAMs have become very popular, and an industry was born that primarily fed computer systems' insatiable appetites for higher bit capacities and faster access speeds.

RAM Types

Two basic RAM types have evolved since 1970. Dynamic RAMs are noted for high capacity, moderate speeds and low power consumption. Their memory cells are basically charge-storage capacitors with driver transistors. The presence or absence of charge in a capacitor is interpreted by the RAM's sense line as a logical 1 or 0. Because of the charge's natural tendency to distribute itself into a lower energy-state configuration, however, dynamic RAMs require periodic charge refreshing to maintain data storage.

Traditionally, this requirement has meant that system designers had to implement added circuitry to handle dynamic RAM subsystem refresh. And at certain times, refresh procedures made the RAM unavailable for writing and reading; the memory's control circuitry had to arbitrate access. LSI dynamic memory controllers reduce the refresh requirement to a minimal design by offering a monolithic controller solution.

Where users are less concerned with space and cost than with speed and reduced complexity, the second RAM type—static RAMs—generally prove best. Unlike their dynamic counterparts, static RAMs store ones and zeros using traditional flip-flop logic-gate configurations. They are faster and require no refresh. A user simply addresses the static RAM, and after a very brief delay, obtains the bit stored in that location. Static devices are also simpler to design with than dynamic RAMs, but the static cell's complexity puts these non-volatile chips far behind dynamics in bit capacity per square mil of silicon.

Read-Only Memory

Another memory class, read-only memory (ROM), is similar to RAM in that a computer addresses it and then retrieves data stored at that address. However, ROM includes no mechanism for altering the data stored at that address—hence, the term read only.

ROM is basically used for storing information that isn't subject to change—at least not frequently. Unlike RAM, when system power goes down, ROM retains its contents.

ROM devices became very popular with the advent of microprocessors. Most early microprocessor applications were dedicated systems; the system's program was fixed and stored in ROM. Manipulated data could vary and was therefore stored in RAM. This application split caused ROM to be commonly called program storage, and RAM, data storage.

The first ROMs contained cell arrays in which the sequence of ones and zeros was established by a metallization interconnect mask step during fabrication. Thus, users had to supply a ROM vendor with an interconnect program so the vendor could complete the mask and build the ROMs. Set-up charges were quite high—in fact, even prohibitive unless users planned for large volumes of the same ROM.

To offset this high set-up charge, manufacturers developed a user-programmable ROM (or PROM). The first such devices used fusible links that could be melted or programmed with a special hardware system.

Once programmed, a PROM was just like a ROM. If the program was faulty, the chip had to be discarded. But, PROMs furnished a more cost-effective way to develop program memory or firmware for low-volume purposes than did ROMs.

As one alternative to fusable-link programming, Intel pioneered an erasable MOS-technology PROM (termed an EPROM) that used charge-storage programming. It came in a standard ceramic DIP package but had a window that permitted die exposure to light. When the chip was exposed to ultraviolet light, high energy photons could collide with the EPROM's electrons and scatter them at random, thus erasing the memory.

The EPROM was not intended for use in read/write applications, but it proved very useful in research and development for prototypes, where the need to alter the program several times is quite common. Indeed, the EPROM market originally consisted almost exclusively of development labs. As the fabrication process became mature, however, and volumes increased, EPROM's lower prices made them attractive even for medium-volume production-system applications.

Intel currently supplies EPROMs in all densities ranging from 16K to 1 Megabit.

An alternative to UV-erasure was furthered with the introduction of a ROM that's user programmable and electrically erasable. Thus, instead of removing the device from its host system and placing it under ultraviolet light to erase its program, the E^{2}PROM (for electrically-erasable programmable ROM) can be reprogrammed in its socket. Information is erased on a byte-by-byte basis, rather than erasing the entire chip. Byte alterability makes E^{2}PROM a preferred solution for non-volatile storage of data values that must be altered during system operation.

Another non-volatile memory advance targets the need for alterable-code storage. Modifications to EPROM cell design effects the replacement of block UV-erasure with block electrical erasure. Thus, instead of erasing program code a byte at a time, the Flash-EPROM (for flash-erasable programmable ROM) electrically erases the entire device in one operation. The device may then be programmed with new code, by a PROM programmer or while the device resides on the circuit board.

Flash-EPROMs add flexibility, while contributing to cost savings, in code storage applications. During prototyping, code changes are quickly and easily implemented at the engineer's workstation through fast electrical erase and programming. At incoming test, multiple test patterns may be run during the same test socketing. Programs may be introduced to the device at anytime during system manufacture—during subassembly stages where alternate test codes are desirable, or at the final assembly level. Efficient electrical erase facilities after-sale code alterations by dealer or service networks.

Intel supplies a family of high-density Flash-EPROMs, providing a cost-effective solution for alterable-code storage.

APPLICATIONS OF MEMORY DEVICES

Besides the particular characteristics of each device that has been discussed, there are a number of other factors to consider when choosing a memory product, such as cost, power consumption, performance, memory architecture and organization, and size of the memory. Each of these factors plays an important role in the final selection process.

Performance

Generally, the term performance relates to how fast the device can operate in a given system environment. This parameter is usually rated in terms of the access time. Fast SRAMs can provide access times as fast as 20 ns, while the fastest DRAM cannot go much beyond the 100 ns mark. A bipolar PROM has an access time of 35 ns. RAM and PROM access is usually controlled by a signal most often referred to as Chip Select ($\overline{CS}$). $\overline{CS}$ often appears in device specifications. In discussing access times, it is important to remember that in SRAMs and PROMs, the access time equals the cycle time of the system whereas in DRAMs, the access time is always less than the cycle time.

Cost

There are many ramifications to consider when evaluating cost. Cost can be spread over factors such as design-in time, cost per device, cost per bit, size of memory, power consumption, etc.

Cost of design time is proportional to design complexity. For example, SRAMs generally require less design-in time than DRAMs because there is no refresh circuitry to consider. Conversely, the DRAM provides the lowest cost per bit because of its higher packing density.

Memory Size

Memory size is generally specified in the number of bytes (a byte is a group of eight bits). The memory size of a system is usually segmented depending upon the general equipment category. Computer mainframes and most of today's minicomputers use blocks of RAM substantially beyond 64K bytes—usually in the hundreds of thousands of bytes. For this size of memory, the DRAM has a significantly lower cost per bit. The additional costs of providing the refresh and timing circuitry are spread over many bits.

The microprocessor user generally requires memory sizes ranging from 2K bytes up to 64K bytes. In memories of this size, the universal site concept allows maximum flexibility in memory design.

Power Consumption

Power consumption is important because the total power required for a system directly affects overall cost. Higher power consumption requires bigger power supplies, more cooling, and reduced device density per board—all affecting cost and reliability. All things considered, the usual goal is to minimize power. Many memories now provide automatic power-down. With today's emphasis on saving energy and reducing cost, the memories that provide these features will gain an increasingly larger share of the market.

In some applications, extremely low power consumption is required, such as battery operation. For these applications, the use of devices made by the CMOS technology have a distinct advantage over the NMOS products. CMOS devices offer power savings of several magnitudes over NMOS. Non-volatile devices such as EPROMs or Flash-EPROMs are usually independent of power problems in these applications.

Power consumption also depends upon the organization of the device in the system. Organization usually refers to the width of the memory word. At the time of their inception, memory devices were organized as nK x 1 bits. Today, they are available in various configurations such as 4K x 1, 16K x 1, 64K x 1, 1K x 4, 2K x 8, etc. As the device width increases, fewer devices are required to configure a given memory word—although the total number of bits remains constant. The wider organization can provide significant savings in power consumption, because a fewer number of devices are required to be powered up for access to a given memory word. In addition, the board layout design is simpler due to fewer traces and better layout advantages. The wider width is of particular advantage in microprocessors and bit-slice processors because most microprocessors are organized in 8-bit or 16-bit architectures. A memory chip configured in the nK x 8 organization can confer a definite advantage—especially in universal site applications. All non-volatile memories other than bubble memories are organized nK x 8 for this very reason.

Types of Memories

The first step to narrowing down your choice is to determine the type of memory you are designing—data store or program store. After this has been done, the next step is to prioritize the following factors:

Performance
Power Consumption
Density
Cost

SUMMARY

Global Memory

Generally, a global memory is greater than 64K bytes and serves as a main memory for a microprocessor system. Here, the use of dynamic RAMs for read/write memory is dictated to provide the highest density and lowest cost per bit. The cost of providing refresh circuitry for the dynamic RAMs is spread over a large number of memory bits, thus minimizing the cost impact.

Local Memory

Local memories are usually less than 64K bytes and reside in the proximity of the processor itself—usually on the same PC board. Types of memories often used in local memory applications are SRAM and EPROM/Flash-EPROM/E^{2}PROM.

Memory Technologies 2

2 Memory Technologies

CHAPTER 2:
INTEL MEMORY TECHNOLOGIES

Most of this handbook is devoted to techniques and information to help you design and implement semiconductor memory in your application or system. In this section, however, the memory chip itself will be examined and the processing technology required to turn a bare slice of silicon into high performance memory devices is described. The discussion has been limited to the basics of MOS (Metal Oxide Semiconductor) technologies as they are responsible for the overwhelming majority of memory devices manufactured at Intel.

There are three major MOS technology families—PMOS, NMOS, and CMOS (Figure 1). They refer to the channel type of the MOS transistors made with the technology. PMOS technologies implement p-channel transistors by diffusing p-type dopants (usually Boron) into an n-type silicon substrate to form the source and drain. P-channel is so named because the channel is comprised of positively charged carriers. NMOS technologies are similar, but use n-type dopants (normally phosphorus or arsenic) to make n-channel transistors in p-type silicon substrates. N-channel is so named because the channel is comprised of negatively charged carriers. CMOS or Complementary MOS technologies combine both p-channel and n-channel devices on the same silicon. Either p- or n-type silicon substrates can be used, however, deep areas of the opposite doping type (called wells) must be defined to allow fabrication of the complementary transistor type.

Most of the early semiconductor memory devices, like Intel's pioneering 1103 dynamic RAM and 1702 EPROM were made with PMOS technologies. As higher speeds and greater densities were needed, most new devices were implemented with NMOS. This was due to the inherently higher speed of n-channel charge carriers (electrons) in silicon along with improved process margins. The majority of MOS memory devices in production today are fabricated with NMOS technologies. CMOS technology has begun to see widespread commercial use in memory devices. It allows for very low power devices and these have been used for battery operated or battery back-up applications. Historically, CMOS has been slower than any NMOS device. Recently, however, CMOS technology has been improved to produce higher speed devices. Up to now, the extra cost processing required to make both transistor types has kept CMOS memories limited to those areas where the technology's special characteristics would justify the extra cost. In the future, the learning curve for high performance CMOS costs will make a larger and larger number of memory devices practical in CMOS.

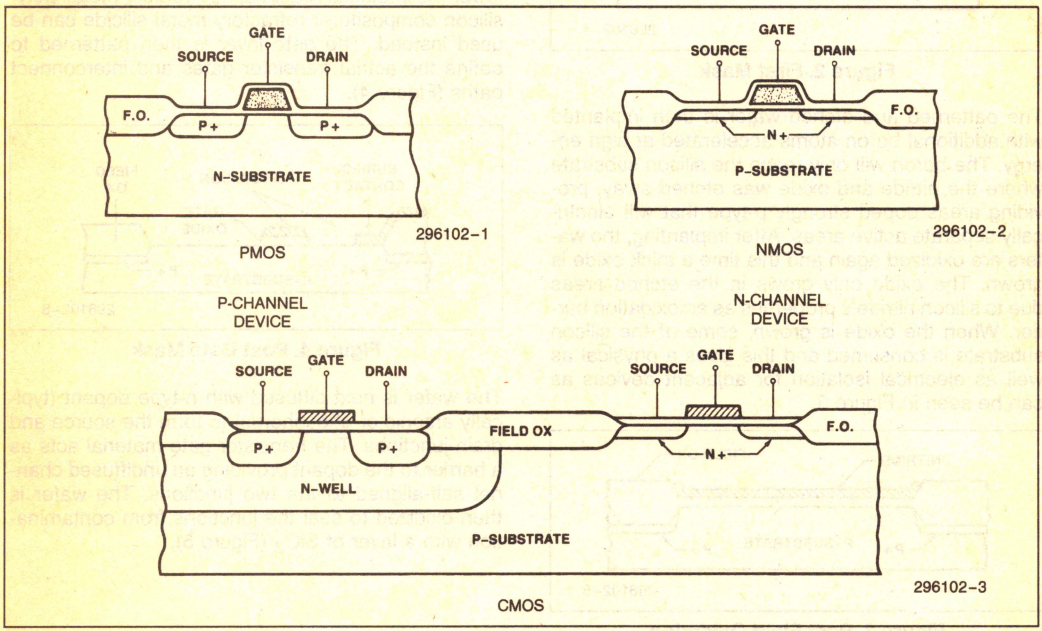


Figure 1. MOS Process Cross-sections

In the following section, the basic fabrication sequence for an HMOS circuit will be described. HMOS is a high performance n-channel MOS process developed by Intel for 5V single supply circuits. HMOS, along with its evolutionary counterparts HMOS II and HMOS III, CHMOS and CHMOS II (and their variants), comprise the process family responsible for most of the memory components produced by Intel today.

The MOS IC fabrication process begins with a slice (or wafer) of single crystal silicon. Typically, it's 100 or 150 millimeter in diameter, about a half millimeter thick, and uniformly doped p-type. The wafer is then oxidized in a furnace at around 1000°C to grow a thin layer of silicon dioxide (SiO_2) on the surface. Silicon nitride is then deposited on the oxidized wafer in a gas phase chemical reactor. The wafer is now ready to receive the first pattern of what is to become a many layered complex circuit. The pattern is etched into the silicon nitride using a process known as photolithography, which will be described in a later section. This first pattern (Figure 2) defines the boundaries of the active regions of the IC, where transistors, capacitors, diffused resistors, and first level interconnects will be made.

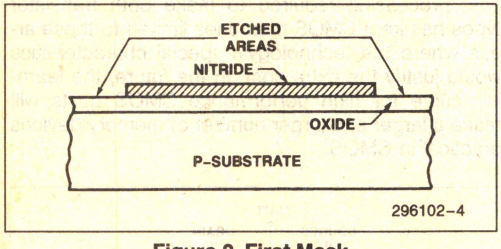


Figure 2. First Mask

The patterned and etched wafer is then implanted with additional boron atoms accelerated at high energy. The boron will only reach the silicon substrate where the nitride and oxide was etched away, providing areas doped strongly p-type that will electrically separate active areas. After implanting, the wafers are oxidized again and this time a thick oxide is grown. The oxide only grows in the etched areas due to silicon nitride's properties as an oxidation barrier. When the oxide is grown, some of the silicon substrate is consumed and this gives a physical as well as electrical isolation for adjacent devices as can be seen in Figure 3.

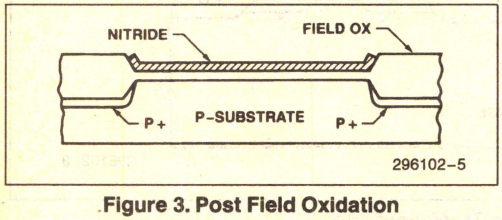


Figure 3. Post Field Oxidation

Having fulfilled its purpose, the remaining silicon nitride layer is removed. A light oxide etch follows taking with it the underlying first oxide but leaving the thick (field) oxide.

Now that the areas for active transistors have been defined and isolated, the transistor types needed can be determined. The wafer is again patterned and then if special characteristics (such as depletion mode operation) are required, it is implanted with dopant atoms. The energy and dose at which the dopant atoms are implanted determines much of the transistor's characteristics. The type of the dopant provides for depletion mode (n-type) or enhancement mode (p-type) operation.

The transistor types defined, the gate oxide of the active transistors are grown in a high temperature furnace. Special care must be taken to prevent contamination or inclusion of defects in the oxide and to ensure uniform consistent thickness. This is important to provide precise, reliable device characteristics. The gate oxide layer is then masked and holes are etched to provide for direct gate to diffusion ("buried") contacts where needed.

The wafers are now deposited with a layer of gate material. This is typically poly crystaline silicon ("poly") which is deposited in a gas phase chemical reactor similar to that used for silicon nitride. The poly is then doped (usually with phosphorus) to bring the sheet resistance down to 10–20 Ω/square. This layer is also used for circuit interconnects and if a lower resistance is required, a refractory metal/polysilicon composite or refractory metal silicide can be used instead. The gate layer is then patterned to define the actual transistor gates and interconnect paths (Figure 4).

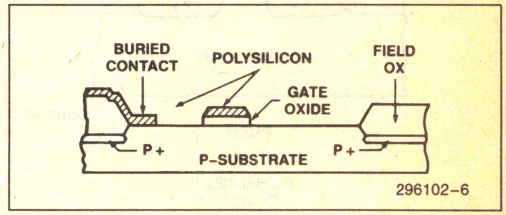


Figure 4. Post Gate Mask

The wafer is next diffused with n-type dopant (typically arsenic or phosphorus) to form the source and drain junctions. The transistor gate material acts as a barrier to the dopant providing an undiffused channel self-aligned to the two junctions. The wafer is then oxidized to seal the junctions from contamination with a layer of SiO_2 (Figure 5).

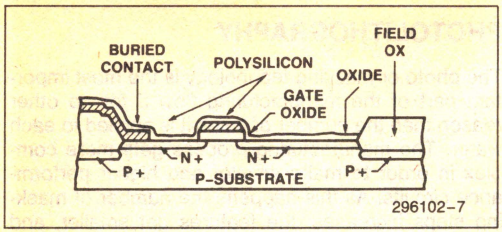


Figure 5. Post Oxidation

A thick layer glass is then deposited over the wafer to provide for insulation and sufficiently low capacitance between the underlying layers and the metal interconnect signals. (The lower the capacitance, the higher the inherent speed of the device.) The glass layer is then patterned with contact holes and placed in a high temperature furnace. This furnace step smooths the glass surface and rounds the contact edges to provide uniform metal coverage. Metal (usually aluminum or aluminum/silicon) is then deposited on the wafer and the interconnect patterns and external bonding pads are defined and etched (Figure 6). The wafers then receive a low temperature (approximately 500°C) alloy that insures good ohmic contact between the Al and diffusion or poly.

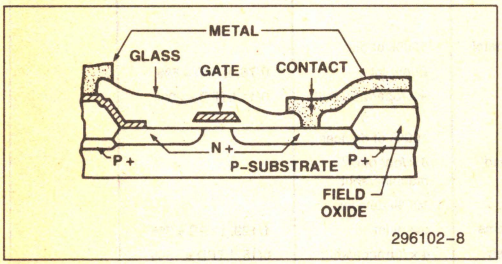


Figure 6. Complete Circuit (without passivation)

At this point the circuit is fully operational, however, the top metal layer is very soft and easily damaged by handling. The device is also susceptible to contamination or attack from moisture. To prevent this the wafers are sealed with a passivation layer of silicon nitride or a silicon and phosphorus oxide composite. Patterning is done for the last time opening up windows only over the bond pads where external connections will be made.

This completes basic fabrication sequence for a single poly layer process. Double poly processes such as those used for high density Dynamic RAMs, EPROMs, and E^2PROMs follow the same general process flow with the addition of gate, poly deposition, doping, and interlayer dielectric process modules required for the additional poly layer (Figure 7). These steps are performed right after the active areas have been defined (Figure 3) providing the capacitor or floating gate storage nodes on those devices.

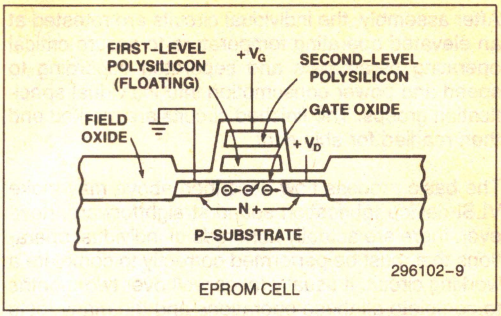


Figure 7. Double Poly Structure

After fabrication is complete, the wafers are sent for testing. Each circuit is tested individually under conditions designed to determine which circuits will operate properly both at low temperature and at conditions found in actual operation. Circuits that fail these tests are inked to distinguish them from good circuits. From here the wafers are sent from assembly where they are sawed into individual circuits with a paper-thin diamond blade. The inked circuits are then separated out and the good circuits are sent on for packaging.

Packages fall into two categories—hermetic and non-hermetic. Hermetic packages are Cerdip, where two ceramic halves are sealed with a glass fritt, or ceramic with soldered metal lids. An example of hermetic package assembly is shown in Table 1. Non-hermetic packages are molded plastics.

The ceramic package has two parts, the base, which has the leads and die (or circuit) cavity, and the metal lid. The base is placed on a heater block and a metal alloy preform is inserted. The die is placed on top of the preform which bonds it to the package. Once attached, wires are bonded to the circuit and then connected to the leads. Finally the package is placed in a dry inert atmosphere and the lid is soldered on.

The cerdip package consists of a base, lead frame, and lid. The base is placed on a heater block and the lead frame placed on top. This sets the lead frame in glass attached to the base. The die is then attached and bonded to the leads. Finally the lid is placed on the package and it is inserted in a seal furnace where the glass on the two halves melt together making a hermetic package.

In a plastic package, the key component is the lead frame. The die is attached to a pad on the lead frame and bonded out to the leads with gold wires. The frame then goes to an injection molding machine and the package is formed around the lead frame. After mold the excess plastic is removed and the leads trimmed.

After assembly, the individual circuits are retested at an elevated operating temperature to assure critical operating parameters and separated according to speed and power consumption into individual specification groups. The finished circuits are marked and then readied for shipment.

The basic process flow described above may make VLSI device fabrication sound straightforward, however, there are actually hundreds of individual operations that must be performed correctly to complete a working circuit. It usually takes well over two months to complete all these operations and the many tests and measurements involved throughout the manufacturing process. Many of these details are responsible for ensuring the performance, quality, and reliability you expect from Intel products. The following sections will discuss the technology underlying each of the major process elements mentioned in the basic process flow.

PHOTOLITHOGRAPHY

The photo or masking technology is the most important part of the manufacturing flow if for no other reason than the number of times it is applied to each wafer. The manufacturing process gets more complex in order to make smaller and higher performance circuits. As this happens the number of masking steps increases, the features get smaller, and the tolerance required becomes tighter. This is largely because the minimum size of individual pattern elements determine the size of the whole circuit, effecting its cost and limiting its potential complexity. Early MOS IC's used minimum geometries (lines or spaces) of 8–10 microns (1 micron = 10^{-6} meter ≅ 1/25,000 inch). The n-channel processes of the mid 1970's brought this down to approximately 5 microns, and today minimum geometries are less than 2 microns in production. This dramatic reduction in feature size was achieved using the newer

Table 1. Typical Hermetic Package Assembly

Flow	Process/Materials	Typical Item	Frequency	Criteria
	Wafer			
	Die saw, wafer break			
	Die wash and plate			
	Die visual inspection	Passivation, metal	100% of die	
	QA gate		Every lot	0/76, LTPD = 5%
	Die attach (Process monitor)	Wet out	4 x /operator/shift	0/11 LTPD = 20%
	Post die attach visual		100% of devices	
	Wire bond (Process monitor)	Orientation, lead dressing, etc.	4 x /operator/ machine/shift	
	Post bond inspection		100% devices	
	QA gate	All previous items	every lot	1/129, LTPD = 3%
	Seal and Mark (Process monitor)	Cap align, glass integrity, moisture	4 x /furnace/shift	0/15, LTPD = 15%
	Temp cycle		10 x to mil std. 883 cond. C	1/11, LTPD = 20%
	Hermeticity check (Process monitor)	F/G leak	100% devices	
	Lead Trim (Process monitor)	Burrs, etc. (visual) Fine leak	4 x /station/shift 2 x /station/shift	0/15, LTPD = 15% 1/129, LTPD = 3%
	External visual	Solder voids, cap alignment, etc.	100% devices	
1.	QA gate	All previous items	All lots	1/129, LTPD = 3%
	Class test (Process monitor)	Run standards (good and reject) Calibrate every system using "autover" program	Every 48 hrs.	
	Mark and Pack			
2.	Final QA	(See attached)		

296102-11

NOTES:
1. Units for assembly reliability monitor.
2. Units for product reliability monitor.

high resolution photo resists and optimizing their processing to match improved optical printing systems.

A second major factor in determining the size of the circuit is the registration or overlay error. This is how accurately one pattern can be aligned to a previous one. Design rules require that space be left in all directions according to the overlay error so that unrelated patterns do not overlap or interfere with one another. As the error space increases the circuit size increases dramatically. Only a few years ago standard alignment tolerances were $\geq \pm 2$ microns; now advanced Intel processes have reduced this dramatically due mostly to the use of advanced projection and step and repeat exposure equipment.

The wafer that is ready for patterning must go through many individual steps before that pattern is complete. First the wafer is baked to remove moisture from its surface and is then treated with chemicals that ensure good resist adhesion. The thick photoresist liquid is then applied and the wafer is spun flat to give a uniform coating, critical for high resolution. The wafer is baked at a low temperature to solidify the resist into gel. It is then exposed with a machine that aligns a mask with the new pattern on it to a previously defined layer. The photo-resist will replicate this pattern on the wafer.

Negative working resists are polymerized by the light and the unexposed resist can be rinsed off with solvents. Positive working resists use photosensitive polymerization inhibitors that allow a chemically reactive developer to remove the exposed areas. The positive resists require much tighter control of exposure and development but yield higher resolution patterns than negative resistance systems.

The wafer is now ready to have its pattern etched. The etch procedure is specialized for each layer to be etched. Wet chemical etchants such as hydrofluoric acid for silicon oxide or phosphoric acid for aluminum are often used for this. The need for smaller features and tighter control of etched dimensions is increasing the use of plasma etching in fabrication. Here a reactor is run with a partial vacuum into which etchant gases are introduced and an electrical field is applied. This yields a reactive plasma which etches the required layer.

The wafer is now ready for the next process step. Its single journey through the masking process required the careful engineering of mechanics, optics, organic chemistry, inorganic chemistry, plasma chemistry, physics, and electronics.

DIFFUSION

The picture of clean room garbed operators tending furnace tubes glowing cherry red is the one most often associated with IC fabrication. These furnace operations are referred to collectively as diffusion because they employ the principle of sold state diffusion of matter to accomplish their results. In MOS processing, there are three main types of diffusion operations: predeps, drives, and oxidations.

Predeposition, or "predep," is an operation where a dopant is introduced into the furnace from a solid, liquid, or gaseous source and at the furnace temperature (usually 900°C–1200°C) a saturated solution is formed at the silicon surface. The temperature of the furnace, the dopant atom, and rate of introduction are all engineered to give a specific dose of the dopant on the wafer. Once this is completed the wafer is given a drive cycle where the dopant left at the surface by the predep is driven into the wafer by high temperatures. These are generally at different temperatures than the predeps and are designed to give the required junction depth and concentration profile.

Oxidation, the third category, is used at many steps of the process as was shown in the process flow. The temperature and oxidizing ambient can range from 800°C to 1200°C and from pure oxygen to mixtures of oxygen and other gases to steam depending on the type of oxide required. Gate oxides require high dielectric breakdown strength for thin layers (between 0.01 and 0.1 micron) and very tight control over thickness (typically ± 0.005 micron or less than $\pm 1/5{,}000{,}000$ inch), while isolation oxides need to be quite thick and because of this their dielectric breakdown strength per unit thickness is much less important.

The properties of the diffused junctions and oxides are key to the performance and reliability of the finished device so the diffusion operations must be extremely well controlled for accuracy, consistency and purity.

ION IMPLANT

Intel's high performance products require such high accuracy and repeatability of dopant control that even the high degree of control provided by diffusion operations is inadequate. However, this limitation has been overcome by replacing critical predeps with ion implantation. In ion implantation, ionized dopant atoms are accelerated by an electric field

and implanted directly into the wafer. The acceleration potential determines the depth to which the dopant is implanted.

The charged ions can be counted electrically during implantation giving very tight control over dose. The ion implanters used to perform this are a combination of high vacuum system, ion source, mass spectrometer, linear accelerator, ultra high resolution current integrator, and ion beam scanner. You can see that this important technique requires a host of sophisticated technologies to support it.

THIN FILMS

Thin film depositions make up most of the features on the completed circuit. They include the silicon nitride for defining isolation, polysilicon for the gate and interconnections, the glass for interlayer dielectric, metal for interconnection and external connections, and passivation layers. Thin film depositions are done by two main methods: physical deposition and chemical vapor deposition. Physical deposition is most common for deposition metal. Physical depositions are performed in a vacuum and are accomplished by vaporizing the metal with a high energy electron beam and redepositing it on the wafer or by sputtering it from a target to the wafer under an electric field.

Chemical vapor deposition can be done at atmospheric pressure or under a moderate vacuum. This type of deposition is performed when chemical gases react at the wafer surface and deposit a solid film of the reaction product. These reactors, unlike their general industrial counterparts, must be controlled on a microscale to provide exact chemical and physical properties for thin films such as silicon dioxide, silicon nitride, and polysilicon.

The fabrication of modern memory devices is a long, complex process where each step must be monitored, measured and verified. Developing a totally new manufacturing process for each new product or even product line takes a long time and involves significant risk. Because of this, Intel has developed process families, such as HMOS, on which a wide variety of devices can be made. These families are scalable so that circuits need not be totally redesigned to meet your needs for higher performance.(1) They are evolutionary (HMOS I, HMOS II, HMOS III, CHMOS) so that development time of new processes and products can be reduced without compromising Intel's commitment to consistency, quality, and reliability.

The manufacture of today's MOS memory devices requires a tremendous variety of technologies and manufacturing techniques, many more than could be mentioned here. Each requires a team of experts to design, optimize, control and maintain it. All these people and thousands of others involved in engineering, design, testing and production stand behind Intel's products.

Because of these extensive requirements, most manufacturers have not been able to realize their needs for custom circuits on high performance, high reliability processes. To address this Intel's expertise in this area is now available to industry through the silicon foundry. Intel supplies design rules and support to design and debug circuits. This includes access to Intel's n-well CHMOS technology. Users of the foundry can now benefit from advanced technology without developing processes and IC manufacturing capability themselves.

(1)R. Pashley, K. Kokkonen, E. Boleky, R. Jecmen, S. Liu, and W. Owen, "H-MOS Scales Traditional Devices to Higher Performance Level," *Electronics*, August 18, 1977.

Static RAMs (Random Access Memories)

3

3

Static RAMs
(Random Access Memories)

2114A
1024 x 4 BIT STATIC RAM

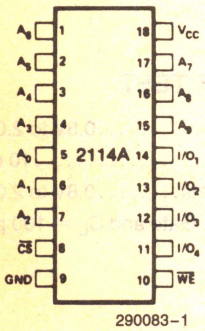
	2114AL-1	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
Max. Access Time (ns)	100	120	150	200	200	250
Max. Current (mA)	40	40	40	40	70	70

- **HMOS II Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18 Pin Package**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **High Reliability Plastic or Cerdip**
- **Available in EXPRESS**
  - **—Standard Temperature Range**
  - **—Extended Temperature Range**

The Intel 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS II, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

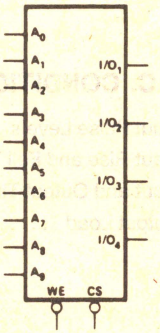
The 2114A is designed for memory applications where the high performance and high reliability of HMOS II, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is assembled in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.



290083-1

Pin Configuration

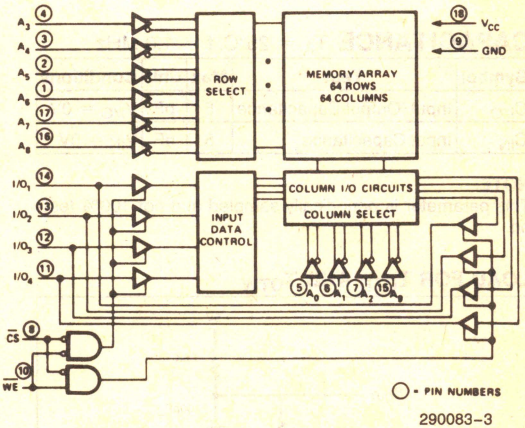


290083-2

Logic Symbol

Pin Names

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	



290083-3

Block Diagram

November 1986
Order Number: 290083-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin
With Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W
D.C. Output Current ..... 5 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%, unless otherwise noted

Symbol	Parameter	2114AL-1/L-2/L-3/L-4			2114A-4/-5			Unit	Conditions
		Min	Typ(1)	Max	Min	Typ(1)	Max		
$\|I_{LI}\|$	Input Load Current (All Input Pins)		0.01	1			1	µA	V_{IN} = 0V to 5.5V
$\|I_{LO}\|$	I/O Leakage Current		0.1	10			10	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0V to 5.5V
I_{CC}	Power Supply Current		25	40		50	70	mA	V_{CC} = max, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	4.0	9.0		4.0	9.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	−2.0	−2.5		−2.0	−2.5		mA	V_{OH} = 2.4V
I_{OS}(2)	Output Short Circuit Current			40			40	mA	V_{OUT} = GND

NOTES:
1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 1 second.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Max	Unit	Conditions
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V

NOTE:
This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8V to 2.0V
Input Rise and Fall Times ..... 10 ns
Input and Output Timing Levels ..... 0.8V to 2.0V
Output Load ..... 1 TTL Gate and C_L = 100 pF

LOAD FOR T_{OTD} AND T_{OTW}

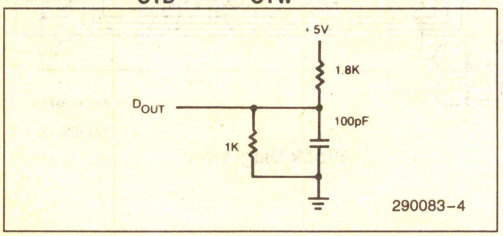


Figure 1

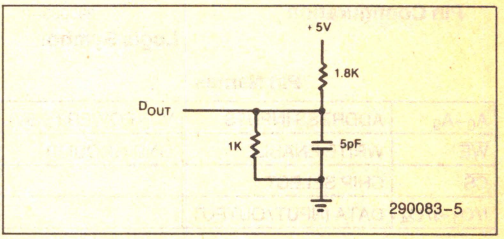


Figure 2

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%, unless otherwise noted.

READ CYCLE[1]

Symbol	Parameter	2114AL-1		2114AL-2		2114AL-3		2114A-4/L-4		2114A-5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		200		250		ns
t_A	Access Time		100		120		150		200		250	ns
t_{CO}	Chip Selection to Output Valid		70		70		70		70		85	ns
t_{CX}[3]	Chip Selection to Output Active	10		10		10		10		10		ns
t_{OTD}[3]	Output 3-state from Deselection		30		35		40		50		60	ns
t_{OHA}	Output Hold from Address Change	15		15		15		15		15		ns

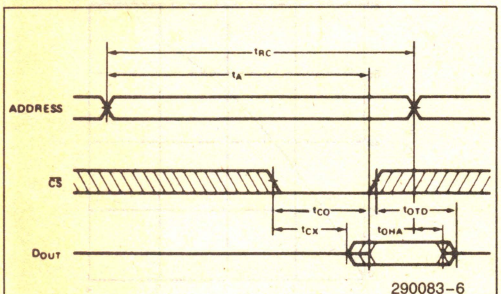
WRITE CYCLE[2]

Symbol	Parameter	2114AL-1		2114AL-2		2114AL-3		2114A-4/L-4		2114A-5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100		120		150		200		250		ns
t_W	Write Time	75		75		90		120		135		ns
t_{WR}	Write Release Time	0		0		0		0		0		ns
t_{OTW}[3]	Output 3-state from Write		30		35		40		50		60	ns
t_{DW}	Data to Write Time Overlap	70		70		90		120		135		ns
t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
3. Measured at ±500 mV with 1 TTL Gate and C_L = 5.00 pF.

WAVEFORMS

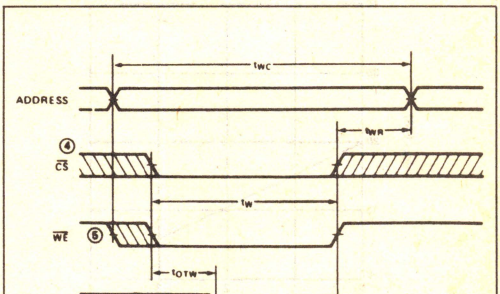
READ CYCLE[3]



290083-6

NOTES:
3. $\overline{WE}$ is high for a Read Cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
5. $\overline{WE}$ must be high during all address transitions.

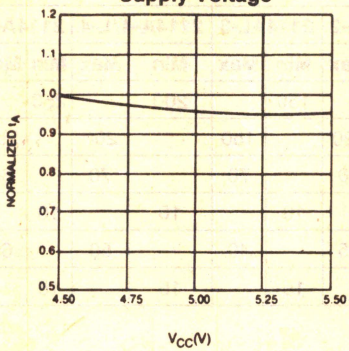
WRITE CYCLE



290083-7

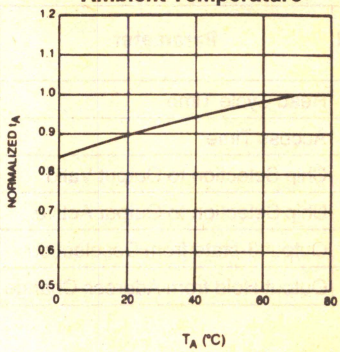
TYPICAL D.C. AND A.C. CHARACTERISTICS

Normalized Access Time vs Supply Voltage



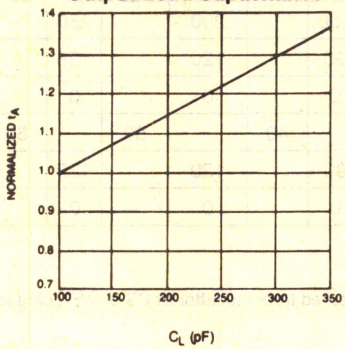
290083-8

Normalized Access Time vs Ambient Temperature



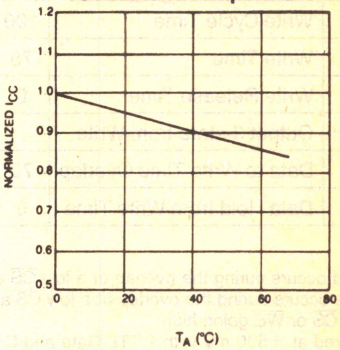
290083-9

Normalized Access Time vs Output Load Capacitance



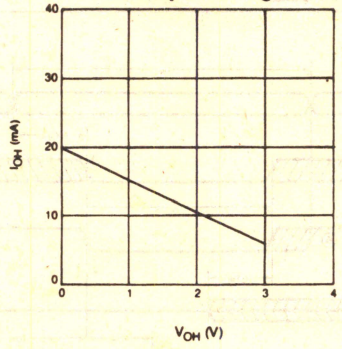
290083-10

Normalized Power Supply Current vs Ambient Temperature



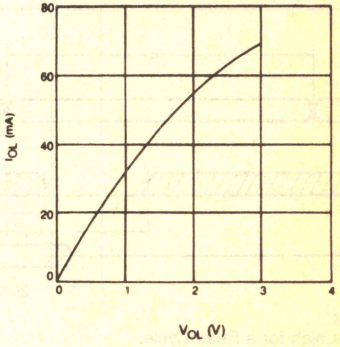
290083-11

Output Source Current vs Output Voltage



290083-12

Output Sink Current vs Output Voltage



290083-13

2115A, 2125A FAMILY
HIGH SPEED 1K x 1 BIT STATIC RAM

	2115AL, 2125AL	2115A, 2125A	2115AL-2, 2125AL-2	2115A-2, 2125A-2
Max. T_{AA}(ns)	45	45	70	70
Max. I_{CC}(mA)	75	125	75	125

- **Pin Compatible to 93415A (2115A) and 93425A (2125A)**
- **Fan-Out of 10 TTL (2115A Family) — 16 mA Output Sink Current**
- **Low Operating Power Dissipation — Max. 0.39 mW/Bit (2115AL, 2125AL)**
- **TTL Inputs and Outputs**
- **Available in EXPRESS — Standard Temperature Range — Extended Temperature Range**
- **Uncommitted Collector (2115A) And Three-State (2125A) Output**
- **Standard 16-Pin Dual In-Line Package**
  (See Packaging Spec. Order #231369)

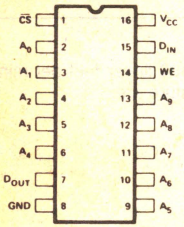
The Intel 2115A and 2125A families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115A) and three-state output (2125A) are available. The 2115A and 2125A use fully DC stable (static) circuitry throughout—in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

The 2115AL/2125AL at 45ns maximum access time and the 2115AL-2/2125AL-2 at 70 ns maximum access time are fully compatible with the industry-produced 1K bipolar RAMs, yet offer a 50% reduction in power of their bipolar equivalents. The power dissipation of the 2115AL/2125AL and 2115AL-2/2125AL-2 is 394 mW maximum as compared to 814 mW maximum of their bipolar equivalents. For systems already designed for 1K bipolar RAMs, the 2115A/2125A and the 2115A-2/2125A-2 at 45 ns and 70 ns maximum access times, respectively offer complete compatibility with a 20% reduction in maximum power dissipation.

The devices are directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

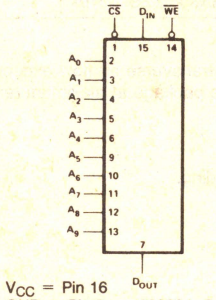
The 2115A and 2125A families are fabricated with Intel's N-channel MOS Silicon Gate Technology.

Pin Configuration



290084-1

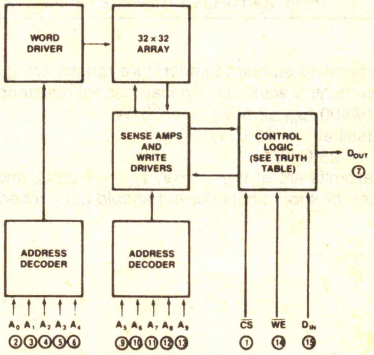
Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

290084-2

Block Diagram



290084-3

Pin Names

$\overline{CS}$	Chip Select
A_0 to A_9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Truth Table

Inputs			Output 2115A Family	Output 2125A Family	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	Not Selected
L	L	L	H	HIGH Z	Write "0"
L	L	H	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

November 1986
Order Number: 290084-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
All Output or Supply Voltage ..... −0.5V to +7V
All Input Voltages ..... −0.5V to +5.5V
D.C. Output Current ..... 20 mA

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min	Typ	Max	Unit	Conditions
V_{OL1}	2115A Family Output Low Voltage			0.45	V	I_{OL} = 16 mA
V_{OL2}	2125A Family Output Low Voltage			0.45	V	I_{OL} = 7 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max., V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max., V_{IN} = 4.5V
$\|I_{CEX}\|$	2115A Family Output Leakage Current		0.1	100	μA	V_{CC} = Max., V_{OUT} = 4.5V
$\|I_{OFF}\|$	2125A Family Output Current (High Z)		0.1	50	μA	V_{CC} = Max., V_{OUT} = 0.5V/2.4V
I_{OS}[3]	2125A Family Current Short Circuit to Ground			−100	mA	V_{CC} = Max.
V_{OH}	Family Output High Voltage	2.4			V	I_{OH} = −3.2 mA
I_{CC}	Power Supply Current: I_{CC1}: 2115AL, 2115AL-2, 2125AL, 2125AL-2		60	75	mA	All Inputs Grounded, Output Open
	I_{CC2}: 2115A, 2115A-2, 2125A, 2125A-2		100	125	mA	

NOTES:
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA}(@400 f_{PM} air flow) = 45°C/W
   θ_{JA}(still air) = 60°C/W
   θ_{JC} = 25°C/W
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and maximum loading.
3. Duration of short circuit current should not exceed 1 second.

2115A FAMILY A.C. CHARACTERISTICS[1,2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

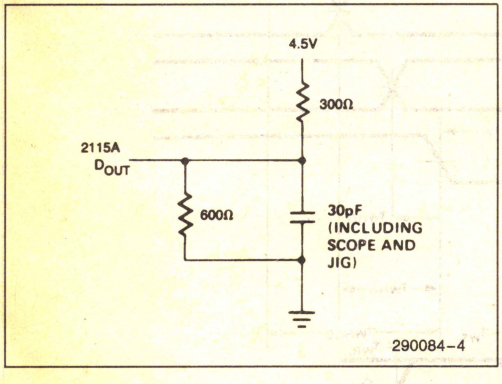
READ CYCLE

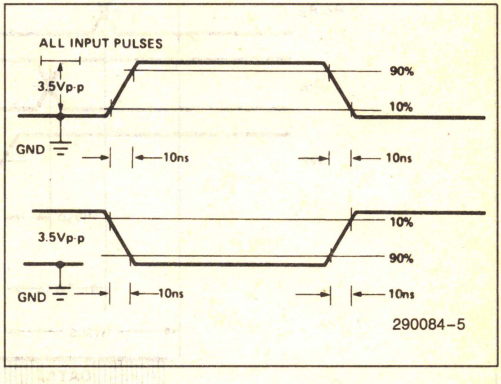
Symbol	Test	2115AL Limits			2115A Limits			2115AL-2 Limits			2115A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{RCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	Address Access Time		30	45		30	45		40	70		40	70	ns
t_{OH}	Previous Read Data Valid after Change of Address	10			10			10			10			ns

WRITE CYCLE

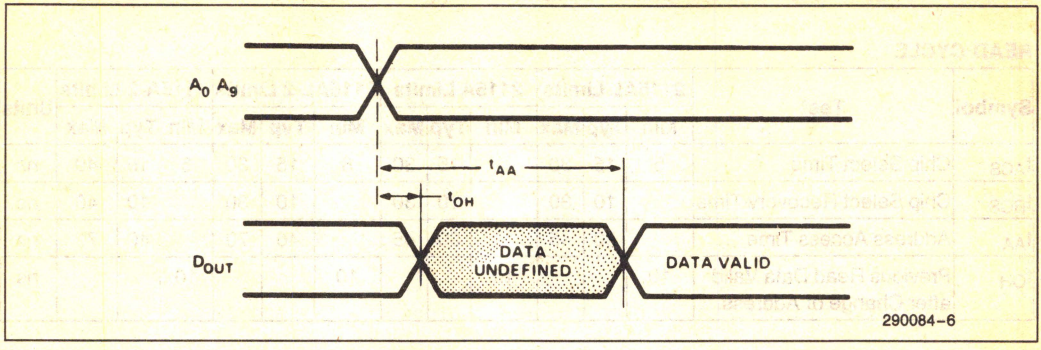
Symbol	Test	2115AL Limits			2115A Limits			2115AL-2 Limits			2115A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WS}	Write Enable Time		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	15		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time after Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

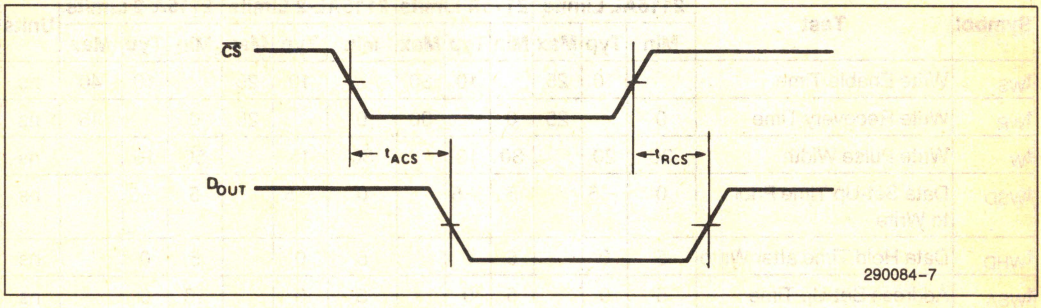




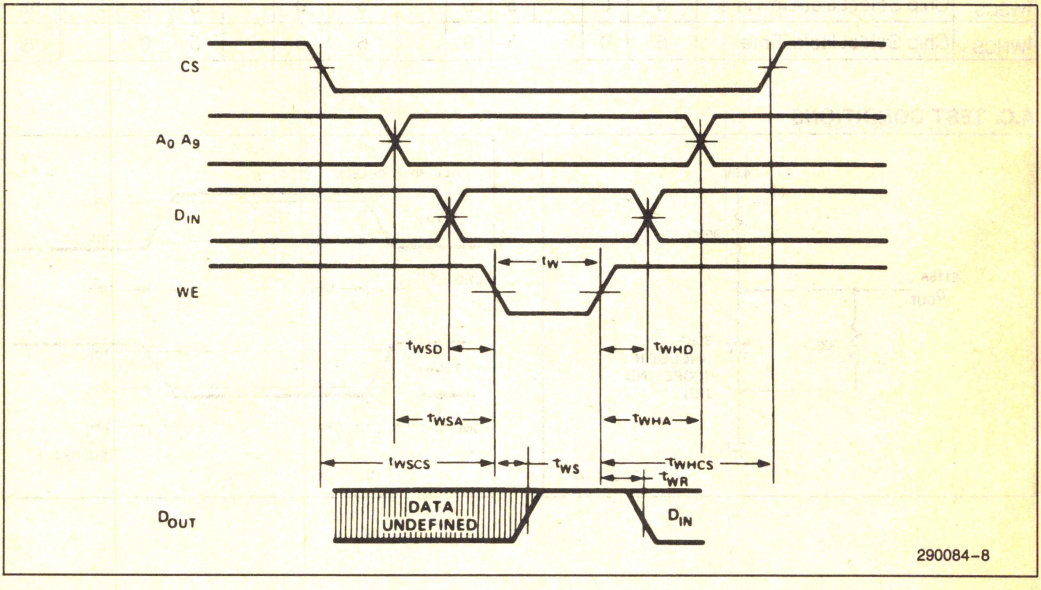
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



WRITE CYCLE



NOTE:
All above measurements referenced to 1.5V.

2125 FAMILY A.C. CHARACTERISTICS[1, 2] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

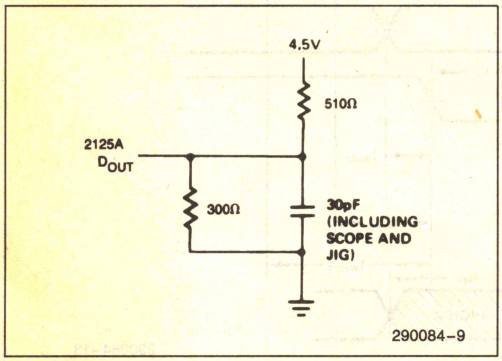
READ CYCLE

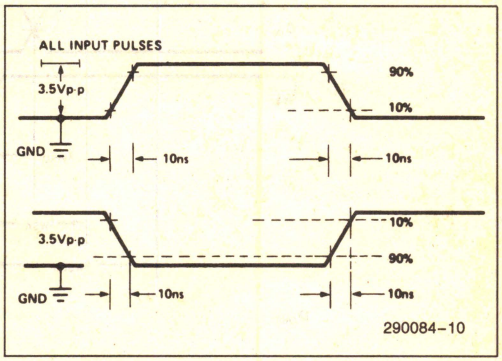
Symbol	Test	2125AL Limits			2125A Limits			2125AL-2 Limits			2125A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ACS}	Chip Select Time	5	15	30	5	15	30	5	15	30	5	15	40	ns
t_{ZRCS}	Chip Select Recovery Time		10	30		10	30		10	30		10	40	ns
t_{AA}	Address Access Time		30	45		30	45		40	70		40	70	ns
t_{OH}	Previous Read Data Valid after Change of Address	10			10			10			10			ns

WRITE CYCLE

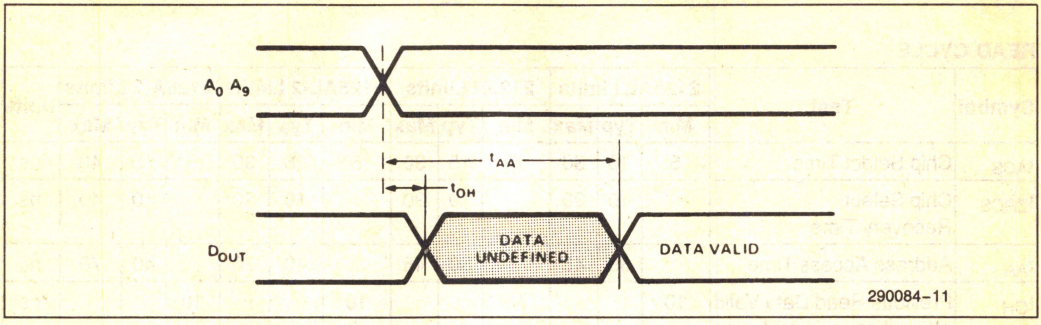
Symbol	Test	2125AL Limits			2125A Limits			2125AL-2 Limits			2125A-2 Limits			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ZWS}	Write Enable Time to HIGH Z		10	25		10	30		10	25		10	40	ns
t_{WR}	Write Recovery Time	0		25	0		30	0		25	0		45	ns
t_W	Write Pulse Width	30	20		30	10		30	10		50	15		ns
t_{WSD}	Data Set-Up Time Prior to Write	0	−5		5	−5		0	−5		5	−5		ns
t_{WHD}	Data Hold Time after Write	5	0		5	0		5	0		5	0		ns
t_{WSA}	Address Set-Up Time	5	0		5	0		5	0		15	0		ns
t_{WHA}	Address Hold Time	5	0		5	0		5	0		5	0		ns
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0		5	0		ns
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		5	0		ns

A.C. TEST CONDITIONS

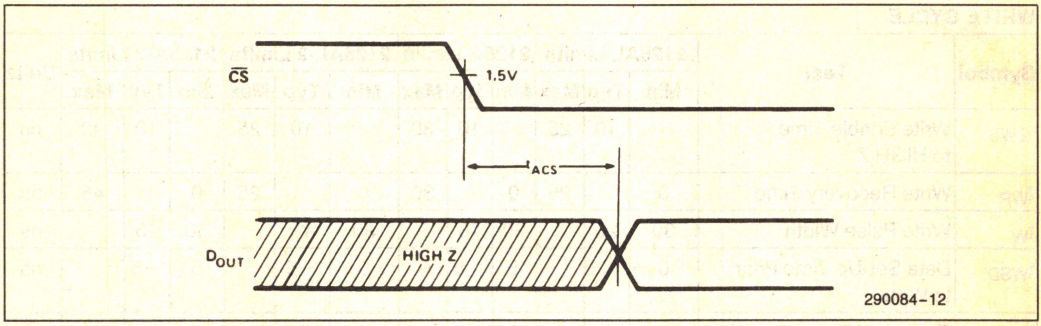




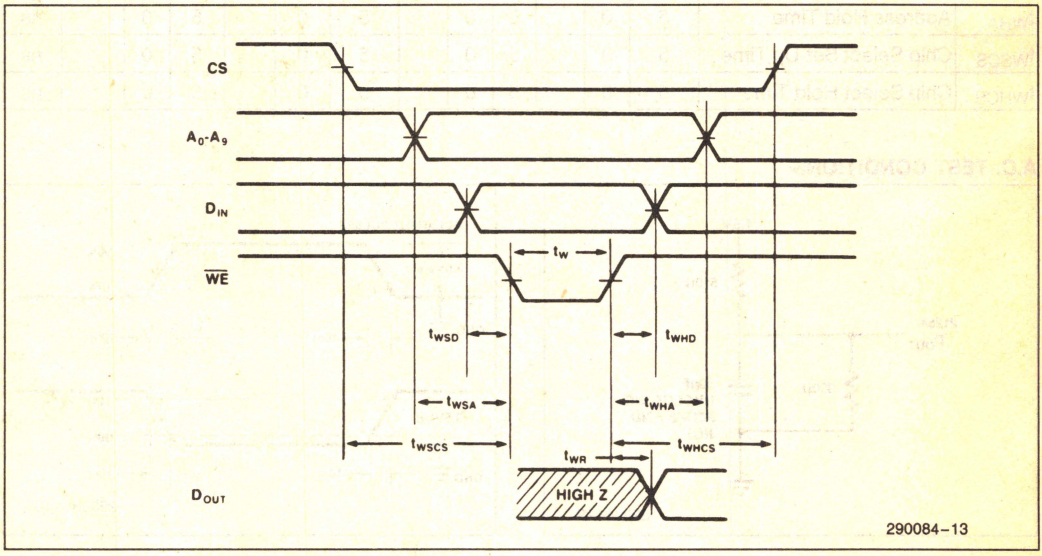
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

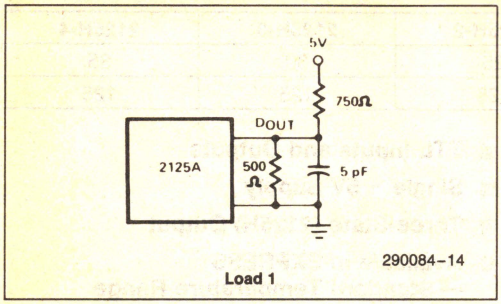


WRITE CYCLE

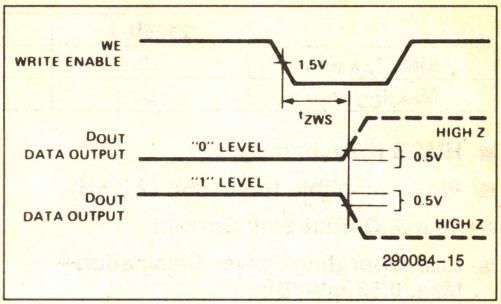


NOTE:
All above measurements referenced to 1.5V.

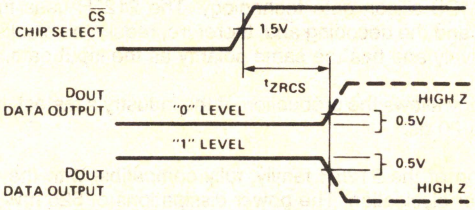
2125A FAMILY WRITE ENABLE TO HIGH Z DELAY



Load 1



2125A FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXX} parameters are measured at a delta of 0.5V from the logic level and using load 1.)

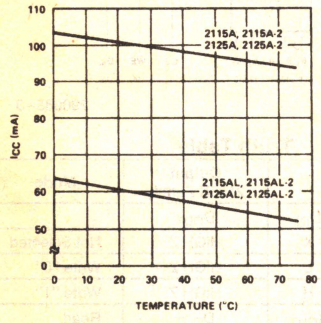
2115A/2125A FAMILY CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	2115A Family Limits		2125A Family Limits		Units	Test Conditions
		Typ.	Max.	Typ.	Max.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

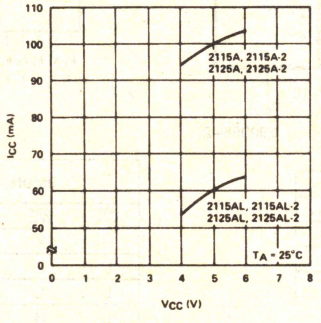
NOTE:
*This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

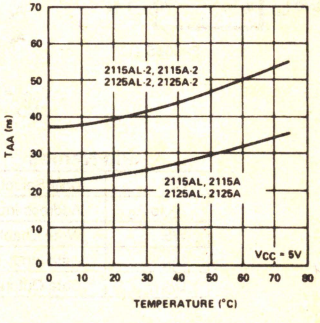
I_{CC} vs Temperature



I_{CC} vs V_{CC}



Access Time vs Temperature



290084-17

2125H
HIGH SPEED 1K × 1 BIT STATIC RAM

	2125H-1	2125H-2	2125H-3	2125H-4
Max. T_{AA} (ns)	20	25	30	35
Max. I_{CC} (mA)	150	125	125	125

- **HMOS II Technology**
- **Pin Compatible to 93425A (2125H)**
- **16 mA Output Sink Current**
- **Low Operating Power Dissipation— Max. 0.53 mW/Bit**
- **Standard 16-Pin Dual In-Line Package**
- **TTL Inputs and Outputs**
- **Single +5V Supply**
- **Three-State (2125H) Output**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

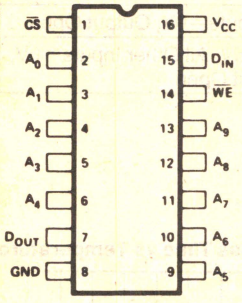
The Intel 2125H has high speed, 1024 words by 1-bit random access memories fabricated with HMOS II, Intel's advanced N-channel MOS silicon gate technology. The 2125H uses fully DC stable (static) circuitry throughout—in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

HMOS II's advanced technology allows the production of the industry's fastest, low power, 1K static RAM—offering access times as low as 20 ns.

HMOS II allows the production of the 2125H family, fully compatible with the 1K Bipolar RAMs yet offering substantial reductions in power dissipation. The power dissipations of 525 mW maximum and 656 mW maximum compared to 814 mW maximum offer reductions of 19% and 36% respectively.

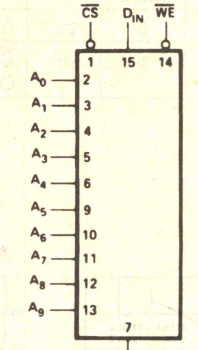
The device is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

Pin Configuration



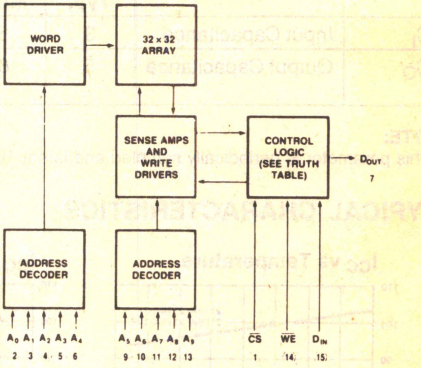
290085-1

Logic Symbol



290085-2

Block Diagram



290085-3

Pin Names

$\overline{CS}$	Chip Select
A_0 to A_9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Truth Table

Inputs			Output 2125H Family	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X_{OUT}	D_{OUT}	Read

November 1986
Order Number: 290085-003

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
All Output or Supply Voltages ..... −0.5V to +7V
All Input Voltages ..... −1.5V to +7V
D.C. Output Current ..... 20 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS(1,2) V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min	Typ	Max	Unit	Conditions
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 16 mA
V_{IH}	Input High Voltage	2.1			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IL}	Input Low Current		−0.1	−40	μA	V_{CC} = Max, V_{IN} = 0.4V
I_{IH}	Input High Current		0.1	40	μA	V_{CC} = Max, V_{IN} = 4.5V
$\|I_{OFF}\|$	Output Current (High Z)		0.1	50	μA	V_{CC} = Max, V_{OUT} = 0.5V/2.4V
I_{OS}	Current Short Circuit to Ground		125	200	mA	V_{CC} = Max.
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −5.2 mA
I_{CC}	Power Supply Current: 2125H-1	80	150	mA		All Inputs Grounded, Output Open
	I_{CC2}: 2125H-2, 2125H-4		80	125	mA	
	I_{CC3}: 2125H-3		80	125	mA	

NOTES:
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and maximum loading.

A.C. CHARACTERISTICS V_{CC} = 5V ±5%, T_A = 0°C to 75°C

READ CYCLE

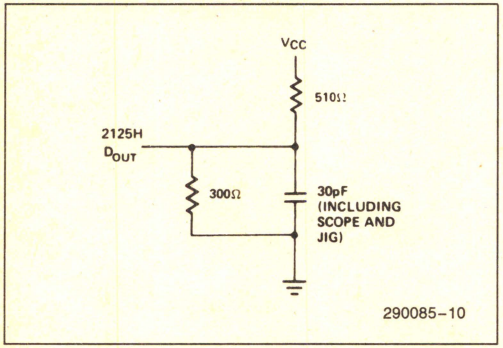
Symbol	Test	2125H-1 Limits		2125H-2 Limits		2125H-3 Limits		2125H-4 Limits		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACS}	Chip Select Time		15		15		20		20	ns
t_{ZRCS}(1)	Chip Select to HIGH Z		20		20		20		20	ns
t_{AA}	Address Access Time		20		25		30		35	ns
t_{OH}(1)	Previous Read Data Valid After Change of Address	0		0		0		0		ns

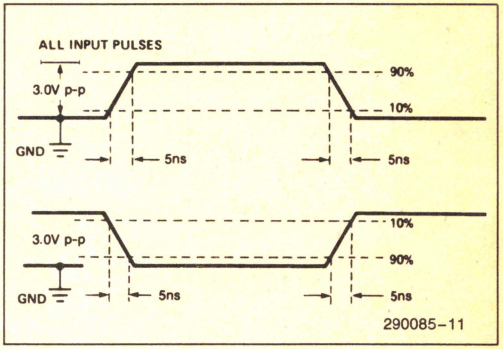
WRITE CYCLE

Symbol	Test	2125H-1 Limits		2125H-2 Limits		2125H-3 Limits		2125H-4 Limits		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZWS}(1)	Write Enable to HIGH Z		15		15		20		20	ns
t_{WR}	Write Recovery Time	0	15	0	15	0	20	0	20	ns
t_W	Write Pulse Width	20		20		20		25		ns
t_{WSD}	Data Set-Up Time Prior to Write	0		0		0		0		ns
t_{WHD}	Data Hold Time After Write	0		0		0		0		ns
t_{WSA}	Address Set-Up Time	5		5		5		5		ns
t_{WHA}(1)	Address Hold Time	0		0		0		0		ns
t_{WSCS}	Chip Select Set-Up Time	5		5		5		5		ns
t_{WHCS}	Chip Select Hold Time	5		5		5		5		ns

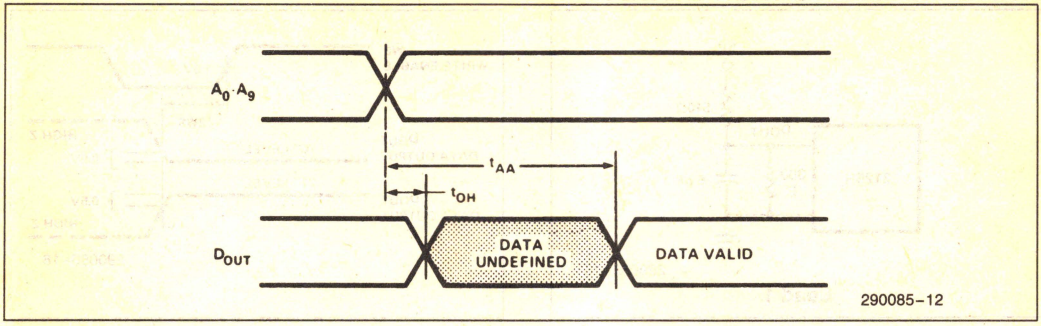
NOTE:
1. These specifications are guaranteed by design and not production tested.

A.C. TEST CONDITIONS

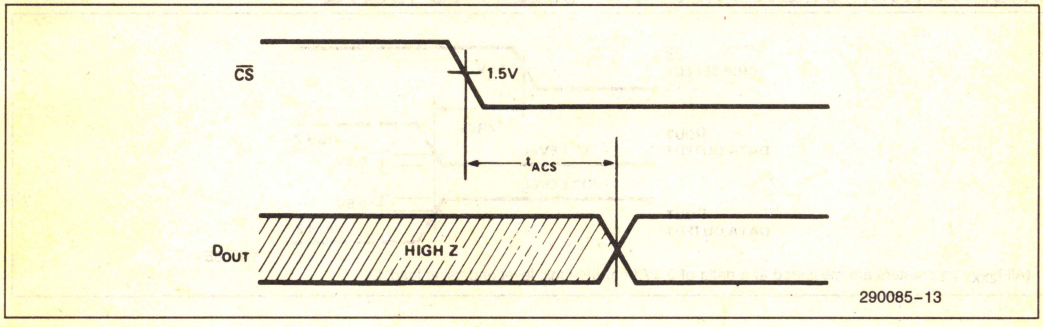




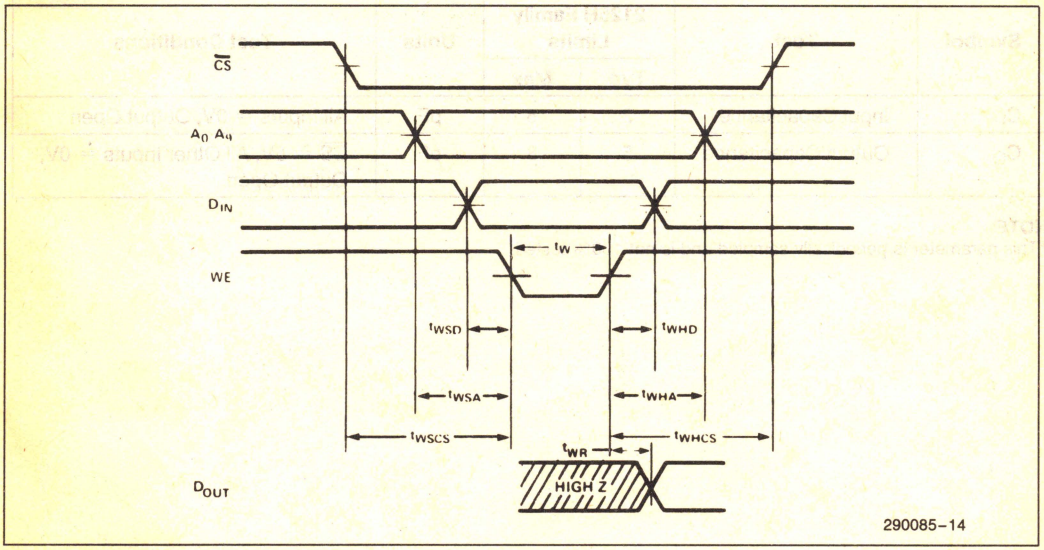
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT

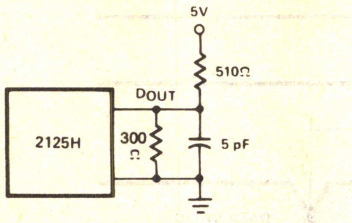


WRITE CYCLE



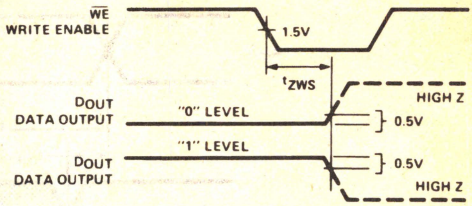
(All above measurements referenced to 1.5V.)

WRITE ENABLE TO HIGH Z DELAY



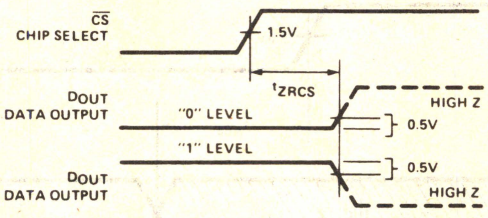
290085-15

Load 1



290085-16

PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



290085-17

(All t_{ZXXX} parameters are measured at a delta of 0.5V from the logic level and using load 1.)

CAPACITANCE* V_{CC} = 5V, f = 1 MHz, T_A = 25°C

Symbol	Test	2125H Family Limits		Units	Test Conditions
		Typ	Max		
C_I	Input Capacitance	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	pF	$\overline{CS}$ = 5V, All Other Inputs = 0V, Output Open

NOTE:
*This parameter is periodically sampled and is not 100% tested.

2147H
HIGH SPEED 4096 x 1 BIT STATIC RAM

	2147H-1	2147H-2	2147H-3	2147H
Max. Access Time (ns)	35	45	55	70
Max. Active Current (mA)	180	180	180	160
Max. Standby Current (mA)	30	30	30	20

- **Pinout, Function, and Power Compatible to Industry Standard 2147**
- **HMOS* III Technology**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **0.8–2.0V Output Timing Reference Levels**
- **Direct Performance Upgrade for 2147**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**
- **Separate Data Input and Output**
- **High Reliability Plastic or Cerdip**
- **Three-State Output**

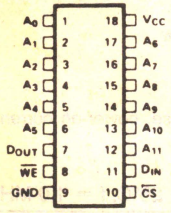
The Intel 2147H is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS III, an ultra high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—deselecting the 2147H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The 2147H is assembled in an 18-pin package configured with the industry standard 2147 pinout. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

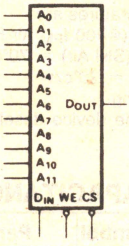
*HMOS is a patent process of Intel.

Pin Configuration



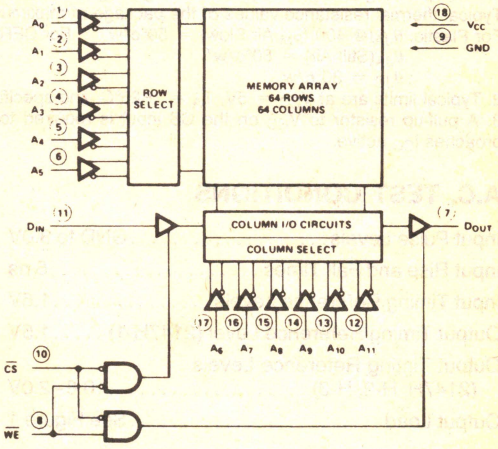
290086-1

Logic Symbol



290086-2

Block Diagram



290086-3

Pin Names

A_0–A_{11}	Address Inputs	V_{CC} Power (+5V)
$\overline{WE}$	Write Enable	GND Ground
$\overline{CS}$	Chip Select	
D_{IN}	Data Input	
D_{OUT}	Data Output	

Truth Table

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

November 1986
Order Number: 290086-003

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to 85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current ..... 20 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted

Symbol	Parameter	2147H-1, 2, 3			2147H			Unit	Test Conditions	
		Min	Typ	Max	Min	Typ(2)	Max			
I_{LI}	Input Load Current (All Input Pins)		0.01	1.0		0.01	1.0	µA	V_{CC} = Max., V_{IN} = GND to V_{CC}	
$\|I_{LO}\|$	Output Leakage Current		0.1	10		0.1	10	µA	$\overline{CS}$ = V_{IH}, V_{CC} = 5.5V V_{OUT} = GND to 4.5V	
I_{CC}	Operating Current		120	170		100	150	mA	T_A = 25°C	V_{CC} = Max., $\overline{CS}$ = V_{IL}, Outputs Open
				180			160	mA	T_A = 0°C	
I_{SB}	Standby Current		18	30		12	20	mA	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}	
I_{PO}(3)	Peak Power-On Current		35	70		25	50	mA	V_{CC} = GND to V_{CC} Min., $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V		
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V		
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA	

NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:
For Plastic: θ_{JA}(@ 400 f_{PM} Air Flow) = 50°c/w For CERDIP: θ_{JA}(@400 f_{PM} Air Flow) = 40°c/w
θ_{JA}(Still Air) = 80°c/w θ_{JA}(Still Air) = 70°c/w
θ_{JC} = 30°c/w θ_{JC} = 25°c/w
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
3. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Input Timing Reference Levels 1.5V
Output Timing Reference Level (2147H-1) 1.5V
Output Timing Reference Levels (2147H, H-2, H-3) 0.8–2.0V
Output Load ..... See Figure 1

CAPACITANCE(4) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

NOTE:
4.This parameter is sampled and not 100% tested.

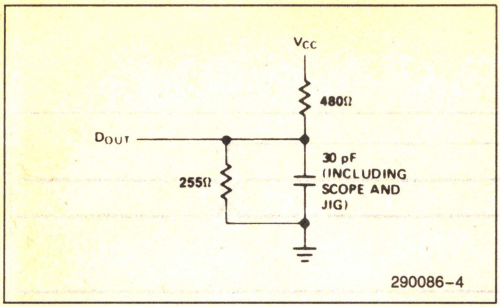


Figure 1. Output Load

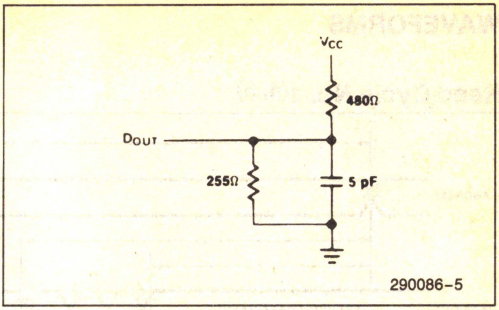


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

A.C. CHARACTERISTICS

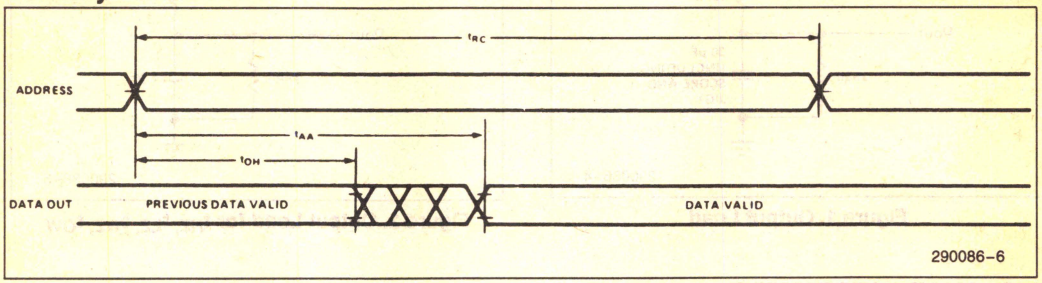
T_A = 0°C to 70°C, V_{CC} = +5V ±10% unless otherwise noted

Read Cycle

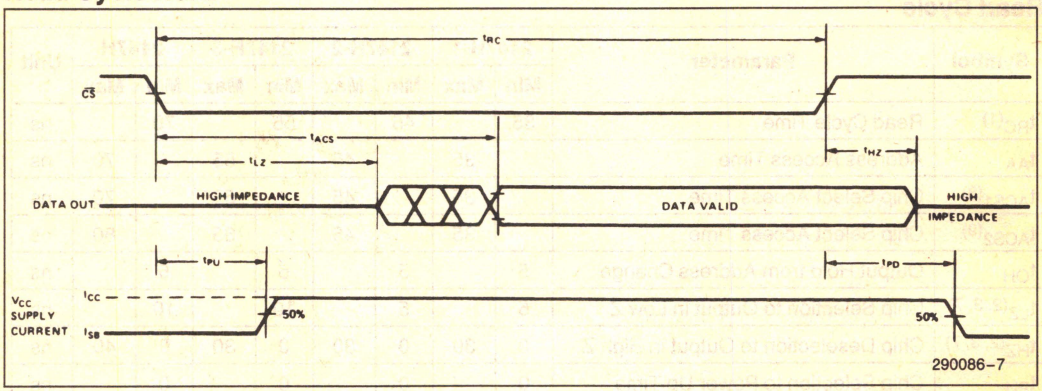
Symbol	Parameter	2147H-1		2147H-2		2147H-3		2147H		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}(1)	Read Cycle Time	35		45		55		70		ns
t_{AA}	Address Access Time		35		45		55		70	ns
t_{ACS1}(8)	Chip Select Access Time		35		45		55		70	ns
t_{ACS2}(9)	Chip Select Access Time		35		45		65		80	ns
t_{OH}	Output Hold from Address Change	5		5		5		5		ns
t_{LZ}(2, 3, 7)	Chip Selection to Output in Low Z	5		5		10		10		ns
t_{HZ}(2, 3, 7)	Chip Deselection to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		20		20		30	ns

WAVEFORMS

Read Cycle No. 1(4, 5)



Read Cycle No. 2(4, 6)



NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.
8. Chip deselected for greater than 55 ns prior to selection.
9. Chip deselected for a finite time that is less than 55 ns prior to selection. If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1. Applies to 2147H, 2147H-3.

A.C. CHARACTERISTICS (Continued)

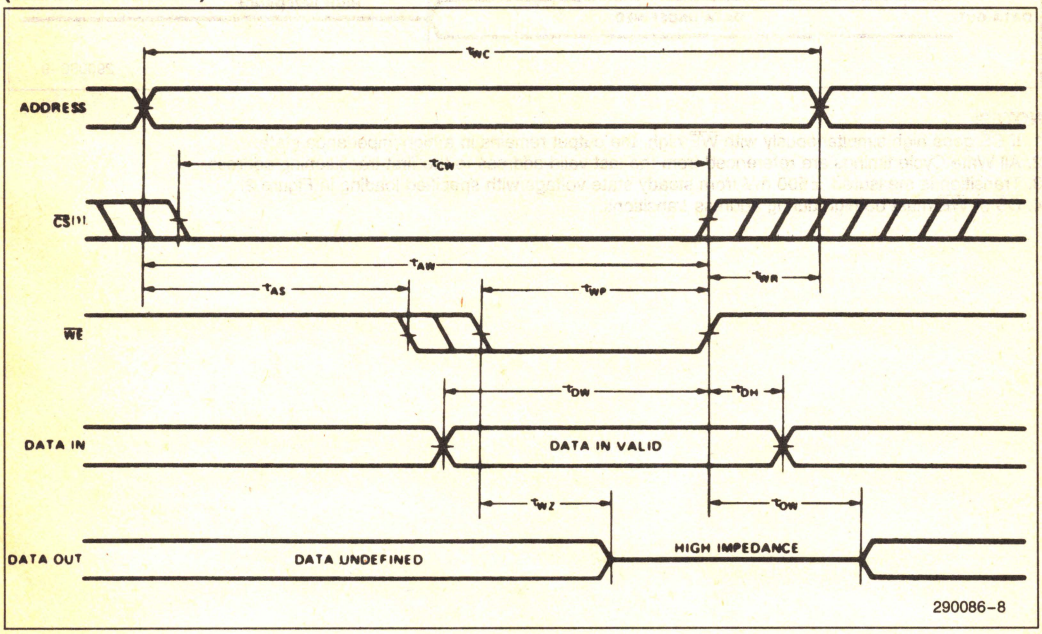
Write Cycle

Symbol	Parameter	2147H-1		2147H-2		2147H-3		2147H		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}[2]	Write Cycle Time	35		45		55		70		ns
t_{CW}	Chip Selection to End of Write	35		45		45		55		ns
t_{AW}	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	20		25		25		40		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	20		25		25		30		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}[3]	Write Enabled to Output in High Z	0	20	0	25	0	25	0	35	ns
t_{OW}[3]	Output Active from End of Write	0		0		0		0		ns

WAVEFORMS

Write Cycle No. 1

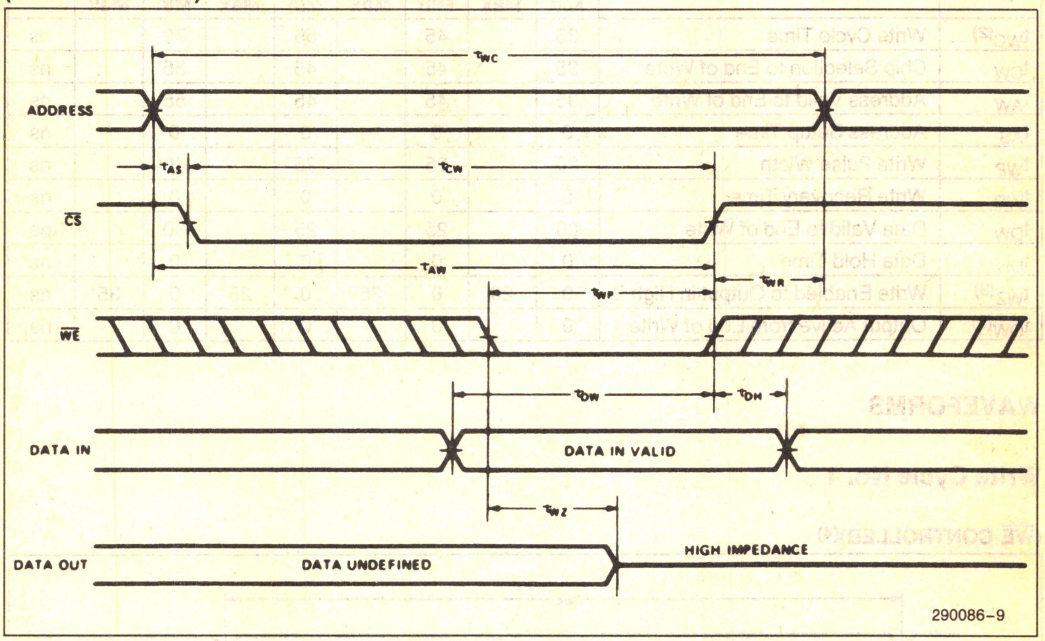
($\overline{WE}$ CONTROLLED)[4]



WAVEFORMS (Continued)

Write Cycle No. 2

($\overline{CS}$ CONTROLLED)(4)



NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

2148H FAMILY
1024 x 4 BIT STATIC RAM

	**2148H-2	2148H-3	2148H	**2148HL-3	2148HL
Max Access Time (ns)	45	55	70	55	70
Max Active Current (mA)	150	**150	**150	125	125
Max Standby Current (mA)	30	30	30	20	20

- **Improved Performance Margins**
- **Automatic Power-Down**
- **Single +5V Supply**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **HMOS* III Technology**
- **Common Data Input and Output**
- **Three-State Output**
- **High Reliability Plastic or CERDIP Package**

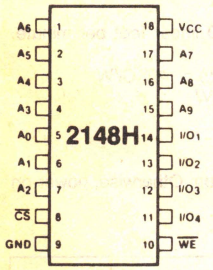
The Intel 2148H is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS III, an ultra high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—disabling the 2148H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are disabled. A non-power-down companion, the 2149H, is available to provide a fast chip select access time for speed critical applications.

The 2148H is assembled in an 18-pin plastic package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

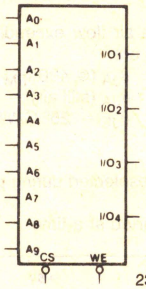
*HMOS is a patent process of Intel Corporation. **Improved performance margins.

Pin Configuration



230781-1

Logic Symbol



230781-2

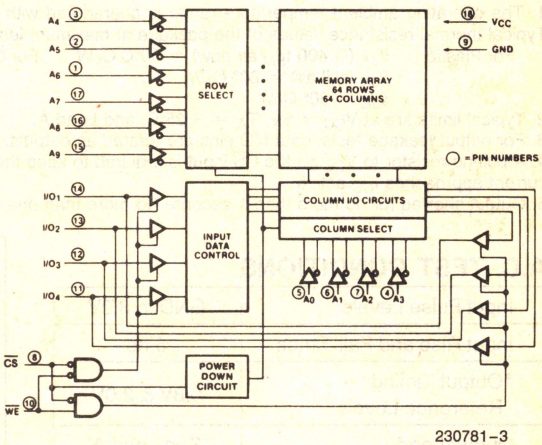
Pin Names

A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
VO_1–V_4	Data Input Output
V_{CC}	Power (+5V)
GND	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	VO	Power
H	X	Not Selected	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

Figure 1. Pin Configuration, Logic Symbol, Pin Names and Truth Table



230781-3

Figure 2. 2148H Block Diagram

November 1986
Order Number: 230781-002

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature CERDIT ... −65°C to +150°C
Storage Temperature Plastic .... −65°C to +125°C
Voltage on Any Pin with
Respect to Ground ..... −3.5V to +7V
D.C. Continuous Output Current ..... 20 mA
Power Dissipation 1.2W

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to +70°C, V_{CC} = +5V ± 10% unless otherwise noted.

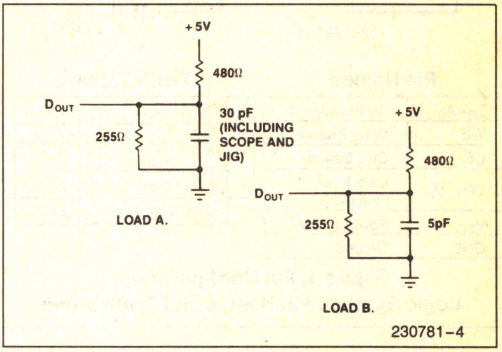
Symbol	Parameter	2148H/H-3/H-2			2148HL/HL-3			Unit	Test Conditions
		Min	Typ[2]	Max	Min	Typ[2]	Max		
*$\|I_{LI}\|$	Input Load Current (All Input Pins)		0.01	1.0		0.01	1.0	µA	V_{CC} = max, V_{IN} = GND to V_{CC}
*$\|I_{LO}\|$(3)	Output Leakage Current		0.1	10		0.1	10	µA	$\overline{CS}$ = V_{IH}, V_{CC} = max, V_{OUT} = GND to 4.5V
*I_{CC}	Operating Current		100	150		70	125	mA	V_{CC} = max, $\overline{CS}$ = V_{IL}, Outputs Open
I_{SB}	Standby Current		20	30		10	20	mA	V_{CC} = min to max, $\overline{CS}$ = V_{IH}
I_{PO}(4)	Peak Power-On Current		25	50		15	30	mA	V_{CC} = GND to V_{CC} min, $\overline{CS}$ = Lower of V_{CC} or V_{IH} min
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
*V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA
I_{OS}(5)	Output Short Circuit Current		±250	±275		±250	±275	mA	V_{OUT} = GND to V_{CC}

NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:
   For Plastic θ_{JA} (@ 400 f_{PM} air flow) = 50°C C/W
   θ_{JA} (still air) = 80° C/W
   θ_{JC} = 30° C/W
   For CERDIP θ_{JA} (@ 400 f_{PM} air flow) = 40° C/W
   θ_{JA} (still air) = 70° C/W
   θ_{JC} = 25° C/W
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and Load A.
3. For output leakage tests, data I/O pins are treated as outputs.
4. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during power-on. Otherwise, power-on current approaches I_{CC} active.
5. Output shorted for no more than 1 second. No more than one output shorted at a time.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
*Output Timing Reference Levels	0.8V & 2.0V
Output Load	See Load A

*Improved perfomance margins.



CAPACITANCE[1] $T_A = 25°C, f = 1.0\ MHz$

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	5	pF	$V_{IN} = 0V$
C_{IO}	Input/Output Capacitance	7	pF	$V_{OUT} = 0V$

NOTE:
1. This parameter is sampled and not 100% tested.

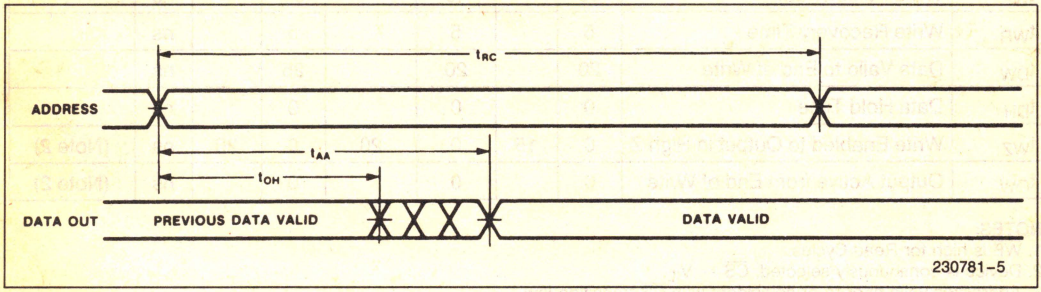
A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

Symbol	Parameter	2148H-2		2148H-3/HL-3		2148H/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
t_{ACS}	Chip Select Access Time		45		55		70	ns	
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection Output in Low Z	20		20		20		ns	(Note 4)
t_{HZ}	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns	(Note 4)
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30		30	ns	

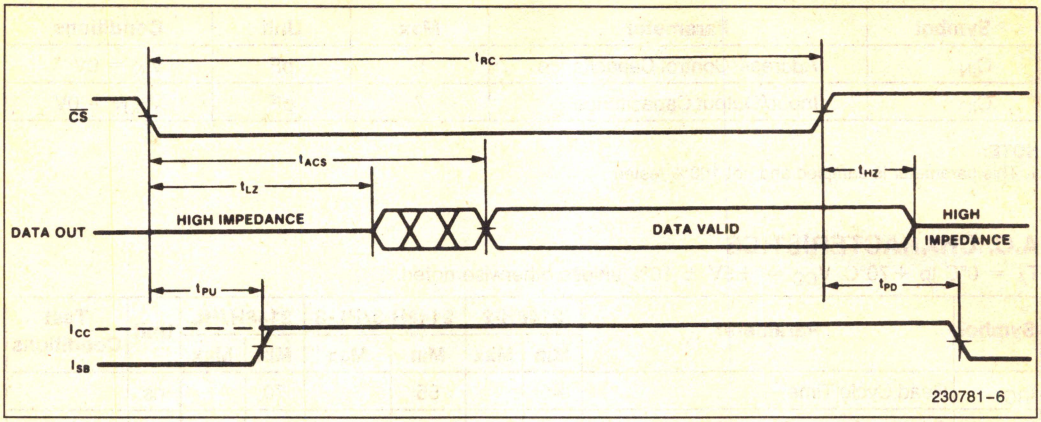
WAVEFORMS

READ CYCLE NO. 1[1,2]



NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500 mV from high impedance voltage with Load B.

READ CYCLE NO. 2(1,3)



A.C. CHARACTERISTICS (Continued)

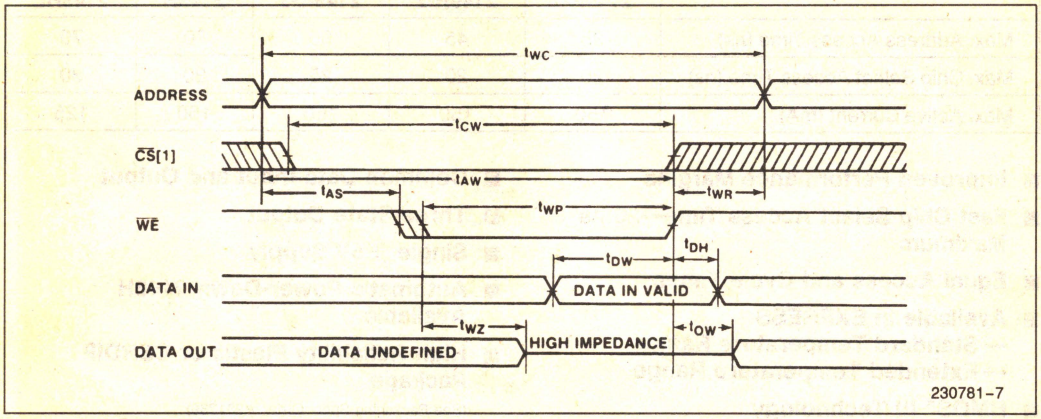
WRITE CYCLE

Symbol	Parameter	2148H-2		2148H-3/HL-3		2148/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Selection to End of Write	40		50		65		ns	
t_{AW}	Address Valid to End of Write	40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	(Note 2)
t_{OW}	Output Active from End of Write	0		0		0		ns	(Note 2)

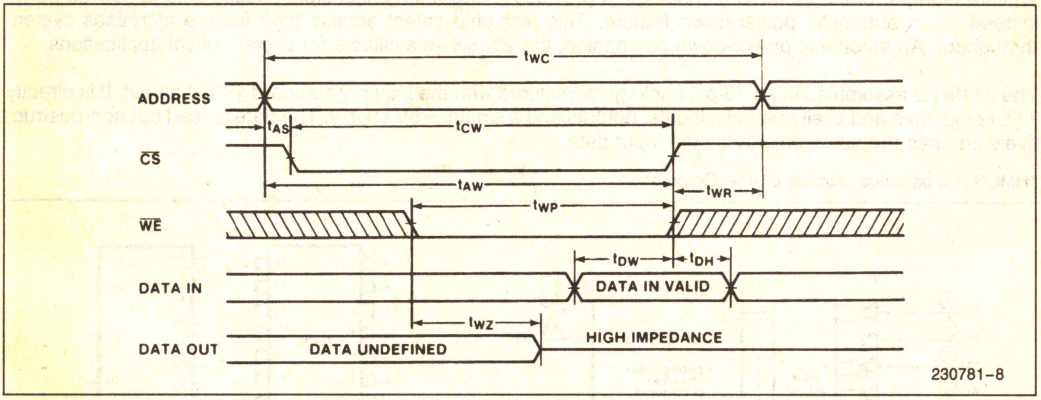
NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500 mV from high impedance voltage with Load B.

WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. Transition is measured ±500 mV from high impedance voltage with Load B.

2149H
1024 x 4-BIT STATIC RAM

	2149H-1	2149H-2	2149H-3	2149H	2149HL
Max. Address Access Time (ns)	35	45	55	70	70
Max. Chip Select Access Time (ns)	20	20	25	30	30
Max. Active Current (mA)	150	150	150	150	125

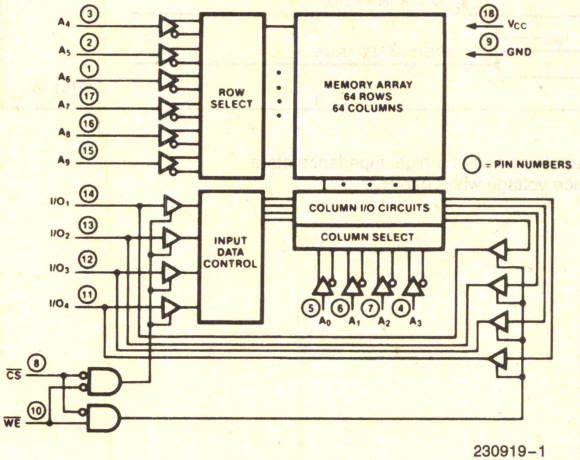
- **Improved Performance Margins**
- **Fast Chip Select Access Time—20 ns Maximum**
- **Equal Access and Cycle Times**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**
- **HMOS* III Technology**
- **Common Data Input and Output**
- **Three-State Output**
- **Single +5V Supply**
- **Automatic Power-Down 2148H Available**
- **High Reliability Plastic or CERDIP Package**

(See Packaging Spec. Order #231369)

The Intel 2149H is 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS III, an ultra high-performance MOS technology. It provides a maximum chip select access time as low as 20 ns instead of an automatic power-down feature. This fast chip select access time feature increases system throughput. An automatic power-down companion, the 2148H, is available for power critical applications.

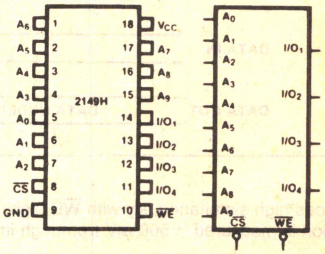
The 2149H is assembled in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible and in all respects: inputs, outputs and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data.

*HMOS is a patented process of Intel Corporation.



230919-1

Figure 1. 2149 Block Diagram



230919-2

Figure 2. 2149 Pin Diagram

Pin Names

A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1–I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O
H	X	Not Selected	HIGH-Z
L	L	Write	D_{IN}
L	H	Read	D_{OUT}

November 1986
Order Number: 230919-003

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature CERDIP ... −65°C to +150°C
Storage Temperature Plastic .... −65°C to +125°C
Voltage on Any Pin with Respect to Ground ..... −3.5V to +7V
D.C. Continuous Output Current ..... 20 mA
Power Dissipation 1.2W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to + 70°C, V_{CC} = +5V ±10% unless otherwise noted.

Symbol	Parameter	2149H/H-1/H-2/H-3			2149HL			Unit	Test Conditions
		Min	Typ(2)	Max	Min	Typ(2)	Max		
I_{LI}	Input Load Current (All Input Pins)		0.01	1.0		0.01	1.0	µA	V_{CC} = max, V_{IN} = GND to 5.5V
I_{LO}	Output Leakage Current		0.1	10		0.1	10	µA	$\overline{CS}$ = V_{IH}, V_{CC} = 5.5V V_{OUT} = GND to 5.5V
I_{CC}	Operating Current		100	150		70	125	mA	V_{CC} = max, $\overline{CS}$ = V_{IL} Outputs Open
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA
I_{OS}(4)	Output Short Circuit Current		±200	±275		±200	±275	mA	V_{OUT} = GND to V_{CC}

A.C. Test Conditions

Input pulse levels ..... GND to 3.0V
Input rise and fail times ..... 5 ns
*Output timing reference levels ..... 0.8V and 2.0V
Output load ..... See Load A.

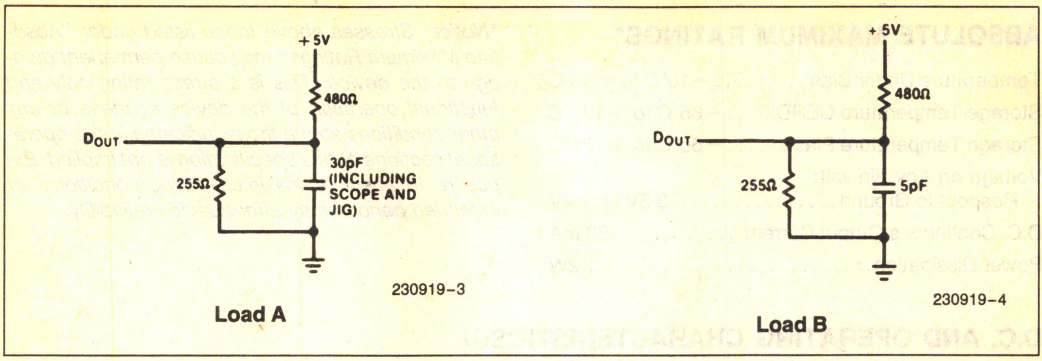
CAPACITANCE(5)

T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	5	pF	V_{IN} = 0V
C_{IO}	Input/Output Capacitance	7	pF	V_{OUT} = 0V

NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:
   For CERDIP θ_{JA}(@400 f_{PM} air flow) = 40°C/W
   θ_{JA}(still air) = 70°C/W
   θ_{JC} = 25°C/W
   For Plastic θ_{JA}(@400 f_{PM} air flow) = 50°C/W
   θ_{JA}(still air) = 80°C/W
   θ_{JC} = 30°C/W
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and Load A.
3. For Output Leakage tests, Data I/O pins are treated as outputs.
4. Outputs shorted for no more than 1 second. No more than one output shorted at a time.
5. This parameter is sampled and not 100% tested.

*improved performance margins



A.C. CHARACTERISTICS

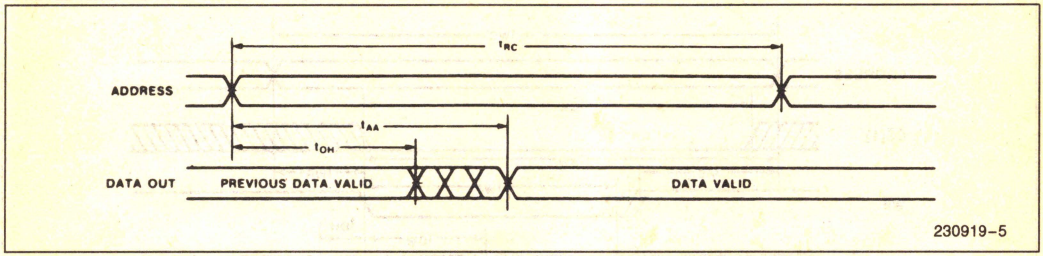
T_A = 0°C to 70°C, V_{CC} = +5V ± 10% unless otherwise noted.

READ CYCLE

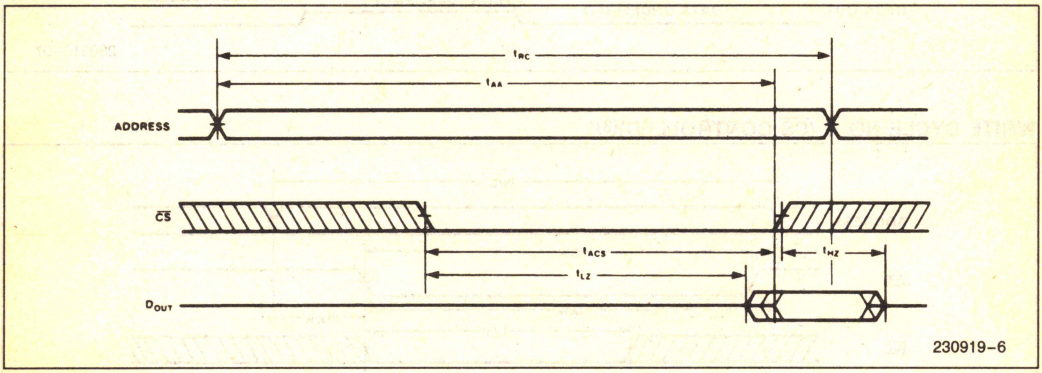
Symbol	Parameter	2149H-1		2149H-2		2149H-3		2149H/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Read Cycle Time	35		45		55		70		ns	
t_{AA}	Address Access Time		35		45		55		70	ns	
t_{ACS}	Chip Select Access Time		20		20		25		30	ns	
t_{OH}	Output Hold from Address Change	5		5		5		5		ns	
t_{LZ}	Chip Selection Output in Low Z	5		5		5		5		ns	(Notes 3, 4)
t_{HZ}	Chip Deselection to Output in High Z	0	15	0	15	0	15	0	15	ns	(Notes 3, 4)

WAVEFORMS

READ CYCLE NO. 1(1, 2)



READ CYCLE NO. 2(3)



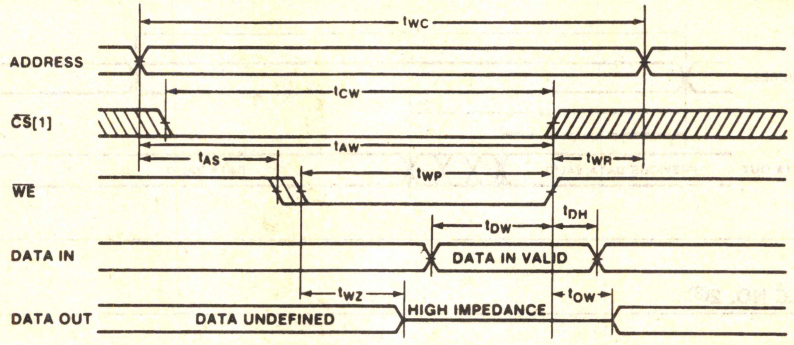
NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
4. Transition is measured ±500 mV from high impedance voltage with Load B.

WRITE CYCLE

Symbol	Parameter	2149H-1		2149H-2		2149H-3		2149H/HL		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WC}	Write Cycle Time	35		45		55		70		ns	
t_{CW}	Chip-Selection to End of Write	30		40		50		65		ns	
t_{AW}	Address Valid to End of Write	30		40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{WP}	Write Pulse Width	30		35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	15	0	20	0	25	ns	(Note 2)
t_{OW}	Output Active from End of Write	0		0		0		0		ns	(Note 2)

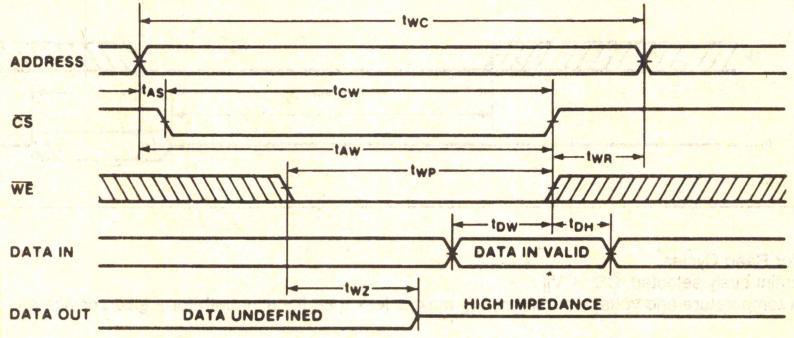
WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(3)



230919-07

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(3)



230919-08

NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. Transition is measured ±500 mV from high impedance voltage with Load B.
3. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

RAM FAMILY

EXPRESS

- **Standard Temperature Range**
- **Extended Temperature Range −40°C– +85°C Available**
- **168 (±8) Hour Burn-In Available**
- **Inspected to 0.1% AQL**

The Intel EXPRESS RAM family is a series of random-access memories which have received additional processing to enhance product operating temperature range and infant mortality. EXPRESS processing is available for several densities of RAM, allowing the choice of appropriate memory size to match system applications.

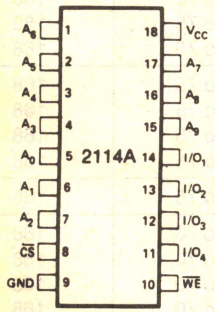
EXPRESS RAM product is available with 168 (±8) hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in.

The standard EXPRESS RAM operating temperature range is 0°C to 70 or 75°C. Extended operating temperature range (−40°C to +85°) EXPRESS product is available. EXPRESS products plus military grade RAMs (−55°C to +125°C) provide the most complete choice of standard and extended temperature range RAMs available.

Like all Intel RAMs, the EXPRESS RAM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

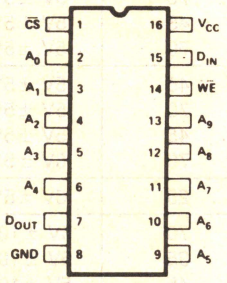
Detailed individual product electrical specifications are available separately in Intel's respective commercial and industrial grade product data sheets.

2114A



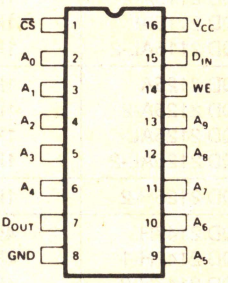
210347-1

2115A, 2125A



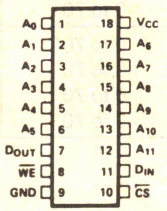
210347-2

2125H



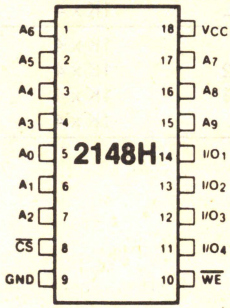
210347-3

2147H



210347-4

2148H, 2149H



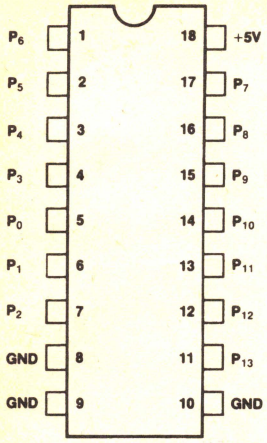
210347-5

Pin Configuration

September 1987
Order Number: 210347-002

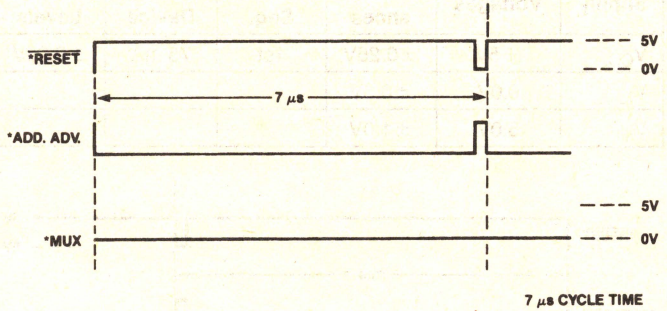
Table 1. RAM Product Family
EXPRESS

Type	Organization	Maximum Access (ns)	Power Supply	Operating Temperature (°C)	Burn-In 125°C (±8 hours)
QD 2114A-4	1K x 4	200	5V ±10%	0 to 70	168
QP 2114A-4	1K x 4	200	5V ±10%	0 to 70	168
QD 2114A-5	1K x 4	250	5V ±10%	0 to 70	168
QP 2114A-5	1K x 4	250	5V ±10%	0 to 70	168
QD 2114AL-1	1K x 4	100	5V ±10%	0 to 70	168
QP 2114AL-1	1K x 4	100	5V ±10%	0 to 70	168
QD 2114AL-2	1K x 4	120	5V ±10%	0 to 70	168
QP 2114AL-2	1K x 4	120	5V ±10%	0 to 70	168
QD 2114AL-3	1K x 4	150	5V ±10%	0 to 70	168
QP 2114AL-3	1K x 4	150	5V ±10%	0 to 70	168
QD 2114AL-4	1K x 4	200	5V ±10%	0 to 70	168
QP 2114AL-4	1K x 4	200	5V ±10%	0 to 70	168
LD 2114A-4	1K x 4	200	5V ±10%	−40 to 85	168
LD 2114A-5	1K x 4	250	5V ±10%	−40 to 85	168
LD 2114AL-3	1K x 4	150	5V ±10%	−40 to 85	168
LD 2114AL-4	1K x 4	200	5V ±10%	−40 to 85	168
TD 2114A-4	1K x 4	200	5V ±10%	−40 to 85	None
TD 2114A-5	1K x 4	250	5V ±10%	−40 to 85	None
TD 2114AL-3	1K x 4	150	5V ±10%	−40 to 85	None
QD 2115A	1K x 1	45	5V ±5%	0 to 75	168
QD 2115A-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2115AL	1K x 1	45	5V ±5%	0 to 75	168
QD 2115AL-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2125A	1K x 1	45	5V ±5%	0 to 75	168
QD 2125A-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2125AL	1K x 1	45	5V ±5%	0 to 75	168
QD 2125AL-2	1K x 1	70	5V ±5%	0 to 75	168
QD 2125H-2	1K x 1	25	5V ±5%	0 to 75	168
QD 2147H	4K x 1	70	5V ±10%	0 to 70	168
QD 2147H-1	4K x 1	35	5V ±10%	0 to 70	168
QD 2147H-2	4K x 1	45	5V ±10%	0 to 70	168
QD 2147H-3	4K x 1	55	5V ±10%	0 to 70	168
QD 2148H	1K x 4	70	5V ±10%	0 to 70	168
QD 2148H-3	1K x 4	55	5V ±10%	0 to 70	168
QD 2148HL	1K x 4	70	5V ±10%	0 to 70	168
QD2149H	1K x 4	70	5V ±10%	0 to 70	168
QD2149H-2	1K x 4	45	5V ±10%	0 to 70	168
QD2149H-3	1K x 4	55	5V ±10%	0 to 70	168
QD2149HL	1K x 4	70	5V ±10%	0 to 70	168



210347-6

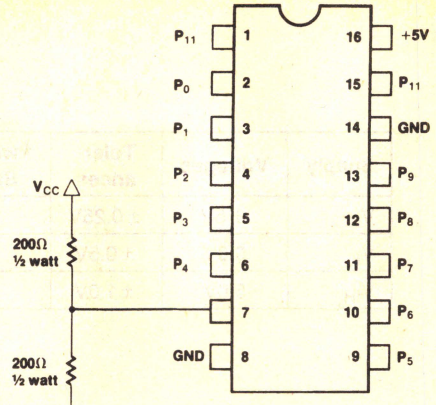
Supply	Voltages	Toler-ances	Pwr-Up Seq.	Current Device	Noise Levels
V_{CC}	+5V	±0.25V	1	70 mA	±0.25V
V_{IL}	0.0V	±0.5V			
V_{IH}	5.0V	±1.0V			



210347-7

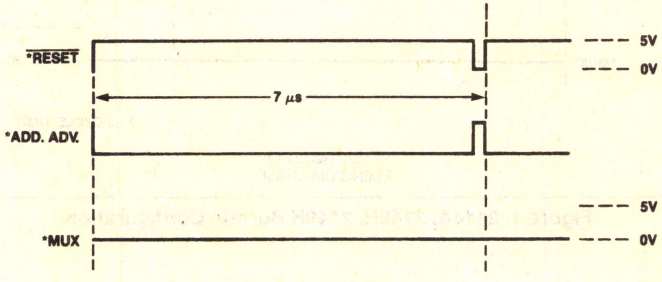
2114/2148/2149
TIMING DIAGRAM

Figure 1. 2114A, 2148H, 2149H Burn-In Configuration



210347-8

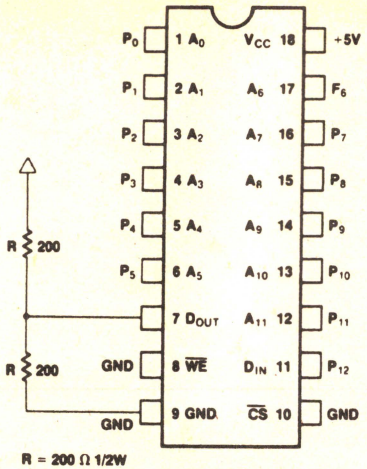
Supply	Voltages	Toler-ances	Pwr-Up Seq.	Current Device	Noise Levels
V_{CC}	+5V	±0.25V	1st	75 mA	±0.25V
V_{IL}	0.0V	±0.5V			
V_{IH}	5.0V	±1.0V			



210347-9

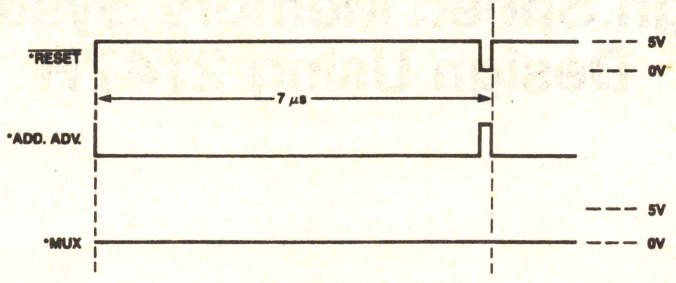
2115/2125 TIMING DIAGRAM
7 μs CYCLE TIME

Figure 2. 2115, 2125 Burn-in Configuration



210347-10

Supply	Voltages	Tolerances	Pwr-Up Seq.	Current Device	Noise Levels
V_{CC}	+5V	±0.25V	1	125 mA	±0.25V
V_{IL}	0.0V	±0.5V			
V_{IH}	5.0V	±1.0V			



210347-11

2147H
TIMING DIAGRAM
7 μs CYCLE TIME

Figure 3. 2147H Burn-In Configuration

intel®

APPLICATION NOTE

AP-74

March 1980

High Speed Memory System Design Using 2147H

JOE ALTNETHER
APPLICATIONS ENGINEERING
INTEL CORPORATION

Order Number: 290080-001

INTRODUCTION

The Intel 2147H is a 4096-word by 1-bit Random Access Memory, fabricated using Intel's reliable HMOS II technology. HMOS II, the second generation HMOS, is Intel's high performance n-channel silicon gate technology, making simple, high speed memory systems a reality. The purpose of this application note is to describe the 2147H operation and discuss design criteria for high speed memory systems.

TECHNOLOGY

When Intel introduced the HMOS 2147, MOS static RAM performance took a quantum leap by combining scaling, internal substrate bias generation, and automatic powerdown. As a result, the 2147 has an access time of 55 ns, density of 4096 bits, and power consumption of 0.99W active and 0.165W standby.

The high performance of the 2147 is further enhanced by the 2147H using HMOS II, a scaled HMOS process increasing the speed at the same power level which involves more than scaling dimensions.

Figure 1 shows the cross section of an HMOS device and lists the parameters of scaling, one of which is high device gain. The slew rate of an amplifier or device is proportional to the gain. Because faster switching speeds occur with high gain, the gain is maximized for high speed. Device gain is inversely proportional to the oxide thickness (T_{OX}) and device length (ℓ), consequently, scaling these dimensions increases the gain.

Another factor which influences performance is unwanted capacitance which appears in two forms—diffusion and Miller. Diffusion capacitance is directly proportional to the diffusion depth (X_j) into the silicon, thus X_j must be reduced. Miller capacitance, the same phenomenon that occurs in the macro world of discrete devices, is proportional to the overlap length of the gate and the source (ℓ_D). Capacitance on the input shunts the high frequency portion of the input signal so that the device can only respond to low frequencies. Secondly, capacitance from the drain to the gate forms a feedback path creating an integrator or low pass filter which degrades the high frequency performance. This effect is minimized by reducing ℓ_D.

One of the limits on scaling is punch through voltage, which occurs when the field strength is too high, causing current to flow when the device is "turned off." Punch through voltage is a function of channel length (ℓ) and doping concentration (C_B), thus channel shortening can be compensated by increasing the doping concentration. This has the additional advantage of balancing the threshold voltage which was decreased by scaling the oxide thickness for gain.

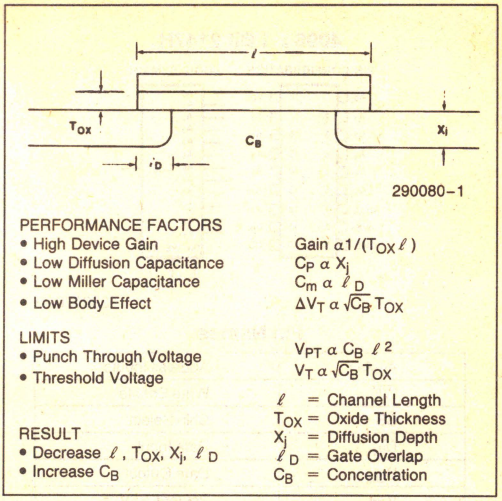


Figure 1. HMOS Scaling

Comparison

Comparing scaling theory to HMOS II scaling in Table 1, note that HMOS II agrees with scaling theory except for the supply voltage. It is left constant at +5V to maintain TTL compatibility. Had the voltage been scaled, the power would have been reduced by $1/K^3$ rather than 1/K, but the device would not have been TTL compatible.

Table 1. Scaling

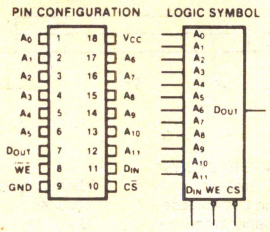
	Theory	HMOS II
Dimensions	1/K	1/K
Substrate Doping	K	K
Voltage	1/K	1
Device Current	1/K	1
Capacitance A/T	1/K	1/K
Time Delay VC/I	1/K	1/K
Power Dissipation VI	$1/K^2$	1
Power Delay Product	$1/K^3$	1/K

THE DEVICE

The 2147H is TTL compatible, operates from a single +5V supply, and is easy to use.

Figure 2 shows the pin configuration and the logic symbol. The 2147H is compatible with the 2147 allowing easy system upgrade. Contained in an industry standard 18-pin dual-in-line package the 2147H is organized as 4096 words of 1 bit. To access each of these

4096 x 1 Bit 2147H



290080-2

Pin Names

A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
GND	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

Figure 2. 2147H Logic Diagram

words, twelve address lines are required. In addition, there are two control signals: $\overline{CS}$, which activates the RAM; and $\overline{WE}$, which controls the write function. Separate data input and output are available. Logical operation of the 2147H is shown in the truth table. The output is in the high impedance or three-state mode unless the RAM is being read. Power consumption switches from standby to active under control of $\overline{CS}$.

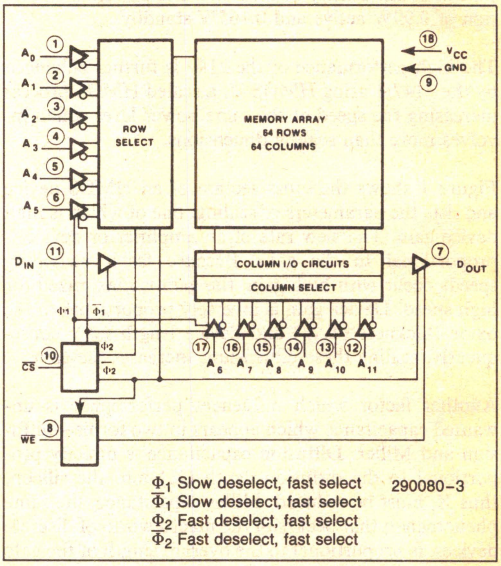
Internal structure of the 2147H is shown in the block diagram of Figure 3. The major portions of the device are: addresses, control ($\overline{CS}$ and $\overline{WE}$), the memory array and a substrate bias generator, which is not shown.

The memory is organized into a two-dimensional array of 64 rows and 64 columns of memory cells. The lower-order six addresses decode one of 64 to select the row while the upper-order six addresses decode to select one column. The intersection of the selected row and the selected column locate the desired memory cell. Additional logic in the column selection circuit controls the flow of data to the array and as stated in the truth table, $\overline{WE}$ controls the output buffer.

As shown in Figure 4, the first three stages of the address buffer are designed with an additional transistor. In each stage, the lowest transistors are the active devices, the middle transistors are load devices, while the upper transistors, controlled by Φ_1, are the key to low standby power. Forming an AND function with the active devices, the upper transistors are turned off when the 2147H is not active, minimizing power consumption. Without them, at least one stage of these cascaded amplifiers would always be consuming power.

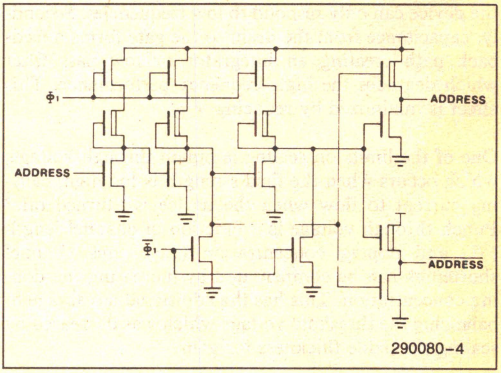
The signal Φ_1, and its inverse $\overline{\Phi}_1$, are generated from CS. They are part of an innovative design not found in the earlier 2147. Their function is to minimize the effects at short deselect times on the Chip Select access time, t_{ACS}.

For both the 2147 and the 2147H, access is delayed until the address buffers are activated by chip selection. In the standard 2147, priming during deselection compensates for this delay by speeding up the access elsewhere in the circuitry. For short deselect times, however, full compensation does not occur because priming is incomplete. The result is a pushout in t_{ACS} for short deselect times.



290080-3

Figure 3. 2147H Block Diagram



290080-4

Figure 4. Address Buffer

In the 2147H, the address buffers are controlled by Φ_1, which is shaped as shown in Figure 5. Φ_1 activates rapidly for fast select time. However, Φ_1 deactivates slowly, keeping the address buffers active during short deselect times to speed access. As shown in Figure 6, this design innovation keeps t_{ACS} pushout to less than 1 ns.

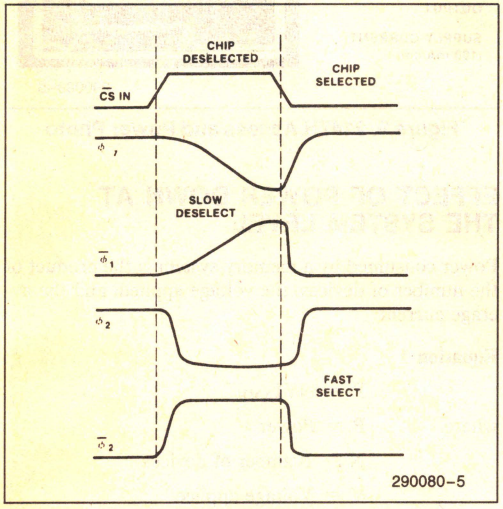


Figure 5. CS Buffer Signals

Figure 7 shows the standard six-transistor cell. Configured as a bi-stable flip-flop, the memory cell uses two transistors for loads and two for active devices so that the data is stored twice as true and compliment. The two remaining transistors enable data onto the internal I/O bus. Unlike the periphery, the cell is not powered down during deselect time to sustain data indefinitely.

The 2147H has an internal bias generator. Bias voltage allows the use of high resistivity substrate by adjusting

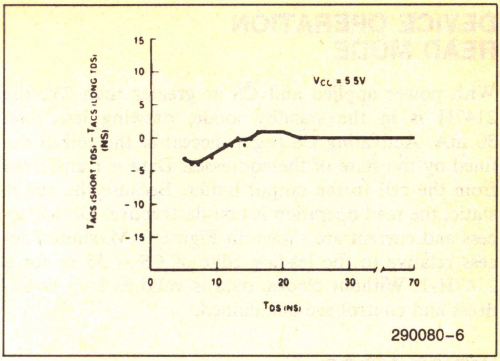


Figure 6. CS Access vs. Deselect Time

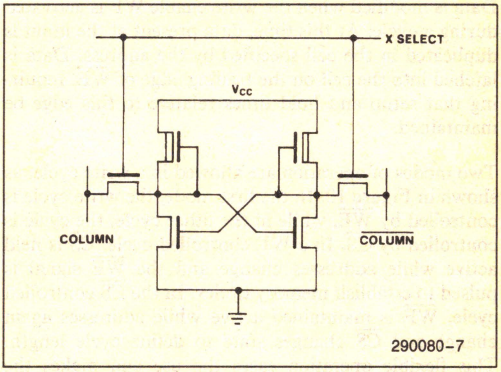


Figure 7. 2147H Memory Cell

the threshold voltages. In addition, it reduces the effect of bulk silicon capacitance. As a result, performance is enhanced. Bias voltage is generated by capacitively coupling the output of a ring oscillator to a charge pump connected to the substrate. Internally generated bias permits the 2147H to operate from a single +5V supply, maintaining TTL compatibility.

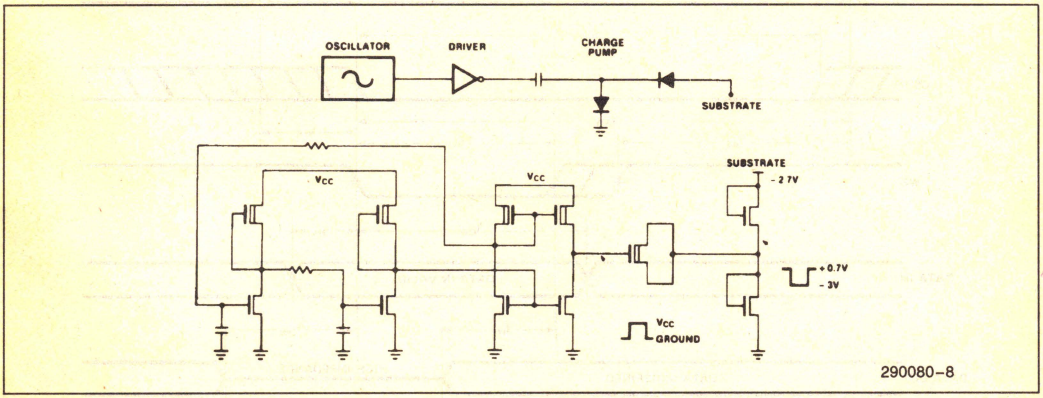


Figure 8. 2147H Substrate Bias Generator

DEVICE OPERATION
READ MODE

With power applied and $\overline{CS}$ at greater than 2V, the 2147H is in the standby mode, drawing less than 30 mA. Activating $\overline{CS}$ begins access of the cell as defined by the state of the addresses. Data is transferred from the cell to the output buffer. Because the cell is static, the read operation is non-destructive. Device access and current are shown in Figure 9. Maximum access relative to the leading edge of $\overline{CS}$ is 35 ns for a 2147H-1. Without clocks, data is valid as long as address and control are maintained.

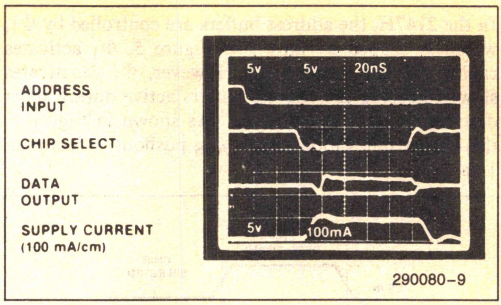


Figure 9. 2147H Access and Power Photo

WRITE MODE

Data is modified when the write enable $\overline{WE}$ is activated during a cycle. At this time, data present at the input is duplicated in the cell specified by the address. Data is latched into the cell on the trailing edge of $\overline{WE}$, requiring that setup and hold times relative to this edge be maintained.

Two modes of operation are allowed in a write cycle, as shown in Figure 10. In the first mode, the write cycle is controlled by $\overline{WE}$, while in the other cycle, the cycle is controlled by $\overline{CS}$. In a $\overline{WE}$ controlled cycle, $\overline{CS}$ is held active while addresses change and the $\overline{WE}$ signal is pulsed to establish memory cycles. In the $\overline{CS}$ controlled cycle, $\overline{WE}$ is maintained active while addresses again change and $\overline{CS}$ changes state to define cycle length. This flexible operation eases the use and makes the 2147H applicable to a wide variety of system designs.

EFFECT OF POWER DOWN AT THE SYSTEM LEVEL

Power consumed by a memory system is the product of the number of devices, the voltage applied, and the average current:

Equation 1

$$P = NVI_{AVE}$$

where:
- P = Power
- N = Number of devices
- V = Voltage applied
- I_{AVE} = Average current/device

Without power down, the average current is approximately the operating current. System power increases

WAVEFORMS

WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED)

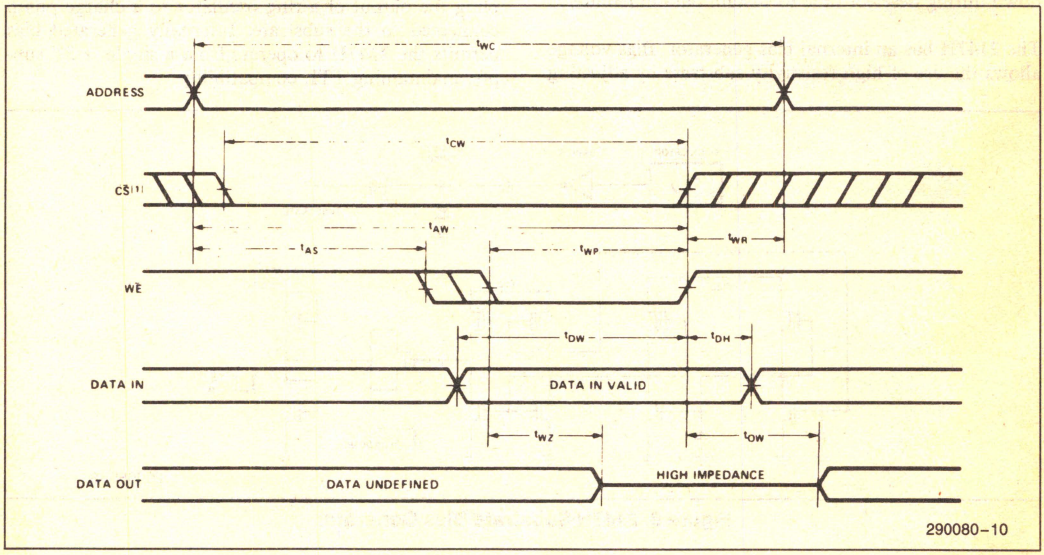
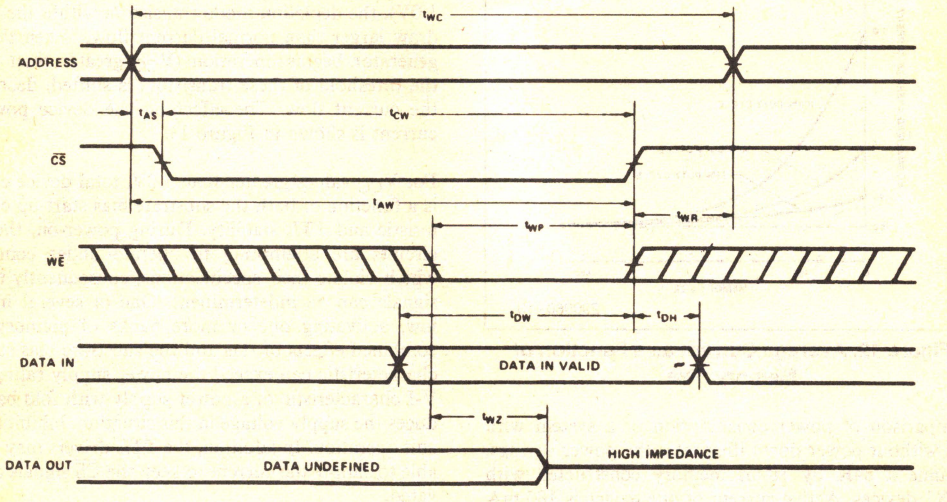


Figure 10. Write Cycle Modes of Operation

WAVEFORMS (Continued)

WRITE CYCLE #2 ($\overline{CS}$ CONTROLLED)



NOTE:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Figure 10. Write Cycle Modes of Operation (Continued)

linearly with the number of devices. With power down, power consumption increases in proportion to the standby current with increasing number of memory devices. Curves in Figure 11 illustrate the difference which results from the majority of devices being in standby with a very small portion of the devices active or being accessed. For a system with power down, the average current of a device in the system is the sum of total active current and the total standby current divided by the number of devices in the system. For an X1 memory such as the 2147H, the number of active devices in most systems will be equal to the number of bits/word, m. Therefore, the number of devices in standby is the difference between N and M. I_{AVE} is expressed mathematically:

Equation 2

$$I_{AVE} = \frac{mI_{ACT} + (N - m)\, I_{SB}}{N}$$

where: m = Number of active devices

I_{ACT} = Active current

I_{SB} = Standby current

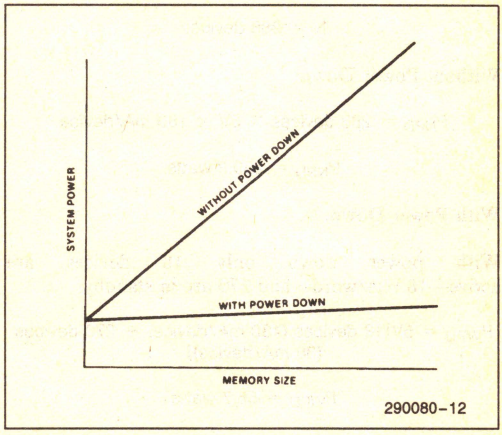


Figure 11. Effect of Power Down at the System

The graph of Figure 12 shows the relation between average device current and memory size for automatic power down. For large memories the average device current approaches the standby current. Total system power usage, P, is calculated by substituting Equation 2 into Equation 1.

$$P = V[mI_{ACT} + (N - m)\, I_{SB}]$$

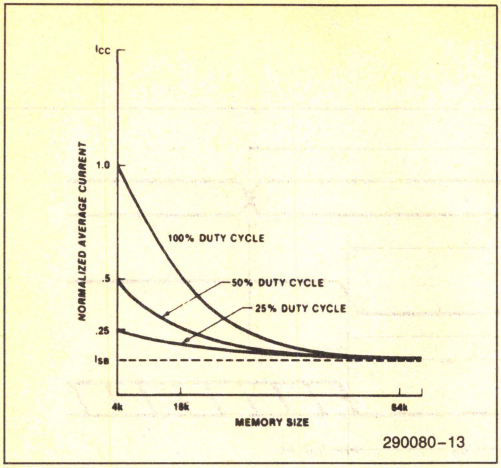


Figure 12. Average Current as a Function of Memory Size

Comparison of power consumption of a system with and without power down illustrates the power savings. Assume a 64K by 18-bit memory constructed with 4KX1 devices. Active current of one device is 180 mA and standby current is 30 mA. Duty cycle is assumed to be 100% and voltage is 5V. The number of devices in the system is:

$$N = \frac{\text{64K words} \times \text{18 bits/word}}{\text{4K bit/device}}$$

$$N = 288 \text{ devices}$$

Without Power Down:

$$P_{NPD} = 288 \text{ devices} \times 5V \times 180 \text{ mA/device}$$

$$P_{NPD} = 259.2 \text{ watts}$$

With Power Down:

With power down only 18 devices are active—18 bits/word—and 270 are in standby.

$$P_{WPD} = 5V[18 \text{ devices (180 mA/device)} + 270 \text{ devices (30 mA/device)}]$$

$$P_{WPD} = 56.7 \text{ watts}$$

The system with power down devices uses only 22% of the power required by a non-powerdown memory system.

POWER-ON

When power is applied, two events occur that must be considered: substrate bias start up and TTL instability. Without the bias generator functioning (V_{CC} less than 1.0V), the depletion mode transistors within the device draw larger than normal current flow. When the bias generator begins operation (V_{CC} greater than 1.0V), the threshold of these transistors is shifted, decreasing the current flow. The effect on the device power-on current is shown in Figure 13.

For V_{CC} values greater than 1.0V, total device current is a function of both the substrate bias start-up characteristic and TTL stability. During power-on, the TTL circuits are attempting to operate under conditions which violate their specifications; consequently the $\overline{CS}$ signals can be indeterminent. One of several may be low, activating one or more banks of memory. The combined effects of this and the substrate bias start-up characteristic can exceed the power supply rating. The V-I characteristic of a power supply with fold back reduces the supply voltage in this situation, inhibiting circuit operation. In addition, the TTL drivers may not be able to supply the current to keep the $\overline{CS}$ signals deactivated.

One of several design techniques available to eliminate the power-on problem is power supply sequencing. Memory supply voltage and TTL supply voltage are separated, allowing the TTL supply to be activated first. When all the $\overline{CS}$ signals have stabilized at 2.0V or greater, the memory supply is activated. In this mode the memory power-on current follows the curve marked $\overline{CS} = V_{CC}$ in Figure 13.

If power sequencing is not practical, an equally effective method is to connect the $\overline{CS}$ signal to V_{CC} through a 1 KΩ resistor. Although this does not guarantee a 2.0V $\overline{CS}$ input; empirical studies indicate that the effect is the same.

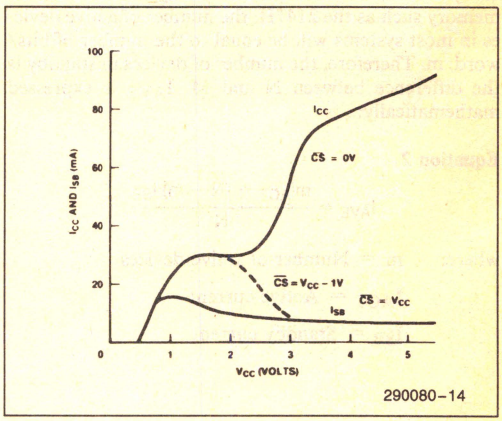


Figure 13. 2147H Power Up Characteristic

ARRAY CHARACTERISTICS

When two or more RAMs are combined, an array is formed. Arrays and their characteristics are controlled by the printed circuit card which is the next most important component after the memory device itself. In addition to physically locating the RAMs, the PC board must route power and signals to and from the RAMs.

GRIDDING

A power distribution network must provide required voltage, which from the 2147H data sheet is 5.0V ±10% to all the RAMs. A printed circuit trace, being an extremely low DC resistance, should easily route ±5V DC to all devices. But as the RAMs are operating, micro circuits within the RAMs are switching micro currents on and off, creating high frequency current transients on the distribution network. Because the transients are high frequency, the network no longer appears as a "pure" low resistance element but as a transmission line. The RAMs and the lumped equivalent circuits of the transmission line are drawn in Figure 14. Each RAM is separated by a small section of transmission line both on the +voltage and the −voltage. Associated with the transmission lines is a voltage attenuation factor. In terms of AC circuits, the voltage across the inductor is the change in current—switching transient—multiplied by the inductance.

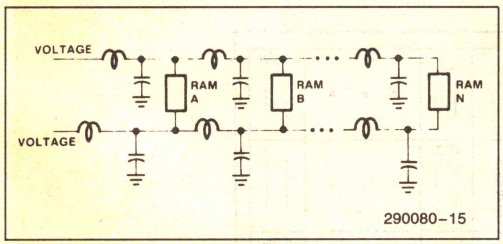


Figure 14. Equivalent Circuit for Distribution

Assuming all RAMs act similarly, the first inductor will see N current transients and the inductor at RAM B sees N-1 transients. The total differential is:

$$\Delta V = \sum_{n=1}^{N} n L \frac{di_n}{dt}$$

That voltage tolerance of ±10% could easily be exceeded with excursions of ±1V not uncommon. Measures must be taken to prevent this. The characteristic impedance of a transmission line is shown in Figure 15A.

Connecting two transmission lines in parallel will halve the characteristic impedance. The result is shown in Figure 15B.

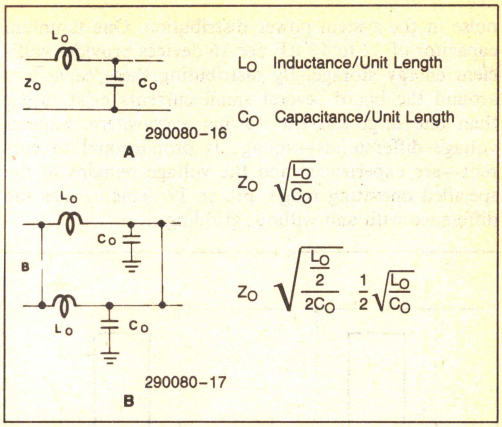


Figure 15. Transmission Line Characteristic Impedance

Paralleling N traces will reduce the impedance to Z_O/N. Extrapolation of this concept to its limit will result in an infinite number of parallel traces such that they are physically touching, forming an extremely wide, low impedance trace, called a plane. Distribution of power (+ voltage) and ground (− voltage) via separate planes provides the best distribution.

PC boards with planes are manufactured as multilayer boards sandwiching the power and ground planes internally. Characteristics of a multilayer board can be cost effectively approximated by gridding the power and ground distribution. Gridding surrounds each device with a ring of power and ground distribution forming many parallel paths with a corresponding reduction of impedance. Gridding is easily accomplished by placing horizontal traces of power (and ground) on one side of the PC board and vertical traces on the other, connected by plated through holes to form a grid.

Viewed from the top of the PC board, the gridding as in Figure 16 surrounds each device. Pseudo-gridding techniques such as serpentine or interdigitated distribution, as in Figure 17, are not effective because there are no parallel paths to minimize the impedance.

DECOUPLING

One final aspect of power/ground distribution must be considered—decoupling.

Decoupling provides localized charge to minimize instantaneous voltage changes on the power grid due to current changes. These transient current changes are local and high frequency as devices are selected and deselected. Adequate decoupling for the 2147H is accomplished by placing a 0.1 μf ceramic capacitor at every other device as shown in Figure 18. Bulk decoupling is included on the board to filter low frequency

noise in the system power distribution. One tantalum capacitor of 22 to 47 μF per 16 devices provides sufficient energy storage. By distributing these capacitors around the board several small currents exist rather than one large current flowing everywhere. Smaller voltage differentials—voltage is proportional to current—are experienced and the voltage remains in the specified operating range. Figure 19 demonstrates the difference with and without gridding.

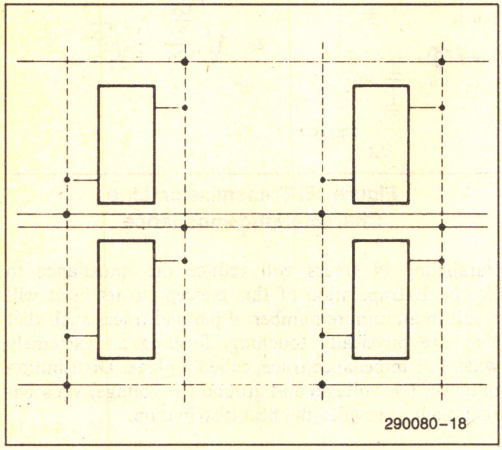


Figure 16. Gridding Plan

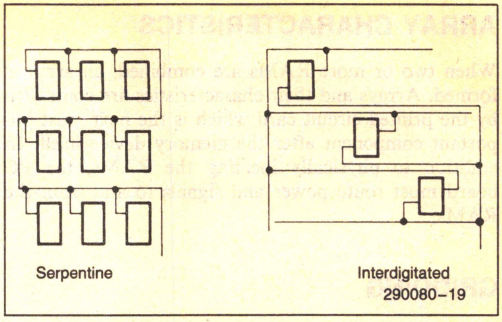


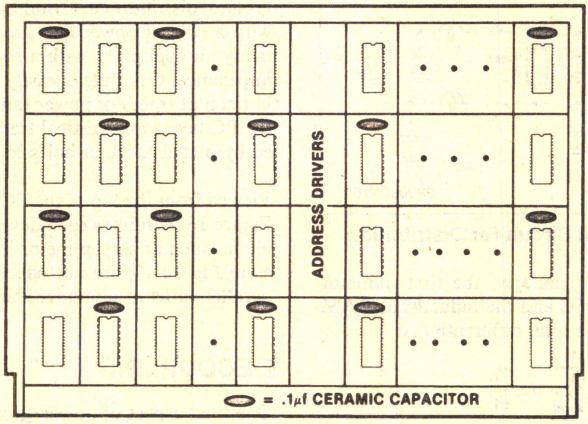
Figure 17. Pseudo-Gridding Techniques

TERMINATION

Similar reasoning is applied to the AC signals: address, control, and data. While they are not gridded or decoupled, they must be kept short and terminated. Similar to the power trace, the signal trace will have transmission line characteristics. A simplified circuit is shown in Figure 20.

MOS RAM input is essentially capacitive. Simplifying the capacitance and writing the differential equation.

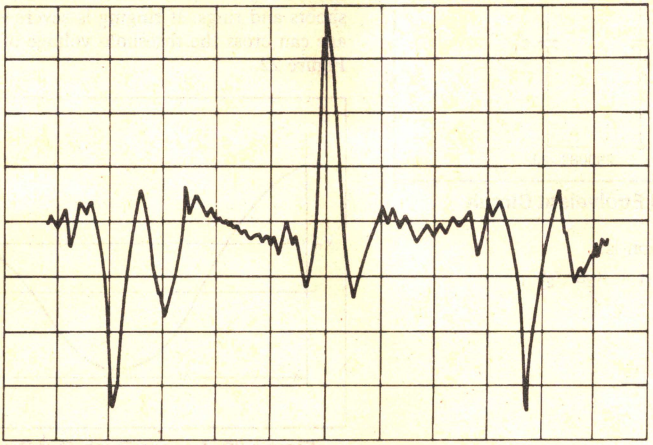
$$\partial = \frac{Ldi}{dt} + \frac{1}{C}\int idt$$



290080-20

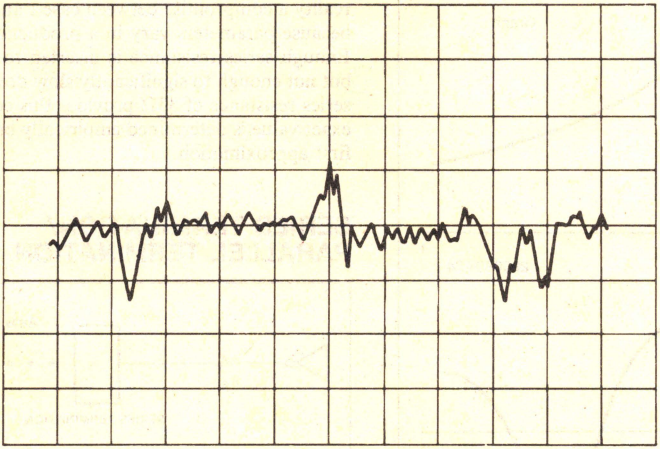
Figure 18. Decoupling

V_{CC} Noise Without Gridding and One Decoupling Capacitor Per 4 RAMs



290080-21

V_{CC} Noise With Gridding and One Decoupling Capacitor Per 2 RAMs



290080-22

Figure 19. V_{CC} Noise With and Without Gridding

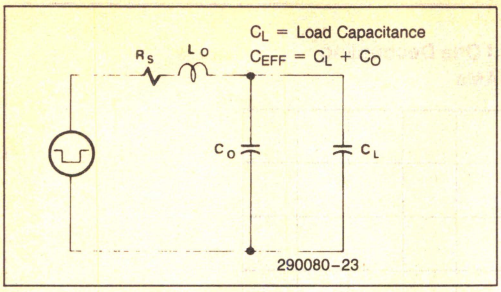


Figure 20. Signal Equivalent Circuit

The solution of this equation is:

$$i = K_1 e^{-r_1 t} + K_2 e^{-r_2 t}$$

where:

$$r_1 = \frac{R}{2L} + \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}$$

$$r_2 = \frac{R}{2L} - \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}}$$

K_1 = constant

K_2 = constant

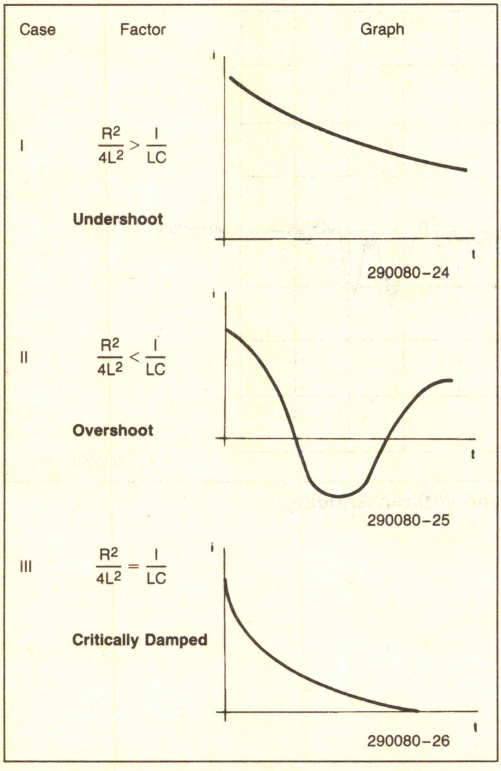


Figure 21. Three Cases of Equation Solution

Dependent on the values of R, L and C, there are three cases shown in Figure 21. In case I, rise and fall times are excessively long. In case III, the current smoothly and clearly changes, while in case II, the current overshoots and rings. If ringing is severe enough, the voltage can cross the threshold voltage of the device as in Figure 22.

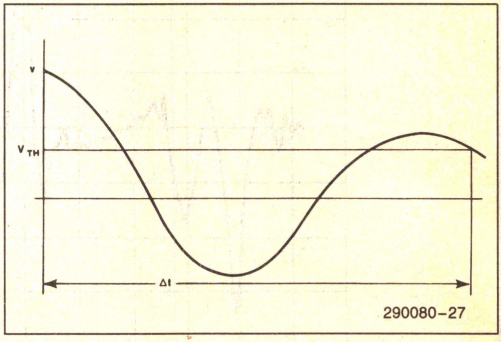


Figure 22. Access Push-Out Due to Ringing

Effective access is stretched out until the wave form settles. System access is the settling time (Δt) plus the specified device access. Case III is the ideal case but in reality a compromise between case I and case II is used because parameters vary in a production environment. Enough series resistance is inserted to prevent ringing but not enough to significantly slow down the access. A series resistance of 33Ω provides this compromise. The exact value is determined empirically but 33Ω is a good first approximation.

SERIES TERMINATION/ PARALLEL TERMINATION

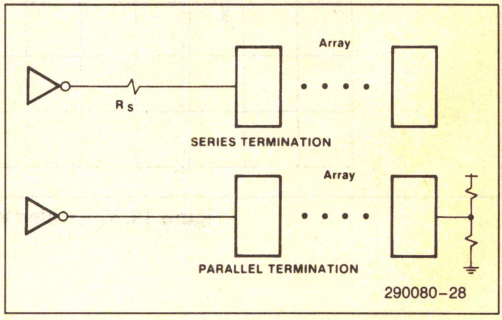


Figure 23. Series and Parallel Termination

Series termination uses one resistor and consumes little power. Current through the resistor creates a voltage differential shifting the levels of input voltage to the devices slightly. This shift is usually insignificant because the 2147H has an extremely high input impedance.

Termination could also be accomplished by a parallel termination as shown in Figure 23. Parallel termination has the advantage of faster rise and fall times but the disadvantage of higher power consumption and increased board space usage.

SYSTEM DELAYS

RAMs are connected to the system through an interface, comprised of address, data and control signals. Inherent in the interface is propagation delay. Added to the RAM access time, propagation delay lengthens system access time and hence system cycle time. Expressed as an equation:

$$t_{sa} = t_{da} + t_{pd}$$

where: t_{sa} = system access time
t_{da} = device access time
t_{pd} = propagation delay

Device access is a fixed value, guaranteed by the data sheet. System efficiency then, is a function of system access and can be expressed as:

$$Eff = t_{da}/t_{sa}$$

where: Eff = System Efficiency

This can be reduced by substitution for t_{sa} to:

$$Eff = 1/(1 + t_{pd}/t_{da})$$

System efficiency is maximized when propagation delay is minimized. With sub 100 ns access RAMs, efficiency can be reduced to 40–60% because delay through the signal paths is significant when compared to RAM access. Three factors contribute to the delay: logic delay, capacitive loading, and transit time.

LOGIC DELAY

The delay through a logic element is the time required for the output to switch with respect to the input. Actual delay times vary. Maximum TTL delays are specified in catalogs, while minimum delays are calculated as one-half of the typical specification. As an example, a gate with a typical delay of 6 ns has a minimum delay of 3 ns.

A signal propagating through two logically identical paths but constructed from different integrated circuits will have two different propagation times. For example, in Figure 24A one path has minimum delays while the other has maximum delays. Path A-B has a delay of 3.5 ns while A-B[1] has a delay of 11 ns. The time difference between these two signals is skew, which will be important later in the system design. Figure 24B shows skew values for several TTL devices.

CAPACITIVE LOADING

Delay time is also affected by the capacitive load on the device. Typical delay as a function of capacitive load is shown in Figure 25. TTL data sheets specify the delay for a particular capacitive load (typically 15 pF or 50 pF). Loads greater than specified will slow the device; similarly, loads less than specified will speed up the device.

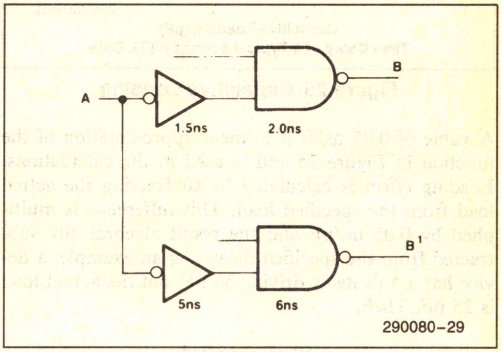


Figure 24A

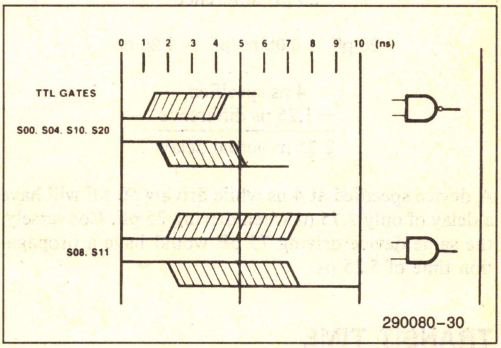


Figure 24B. Skew

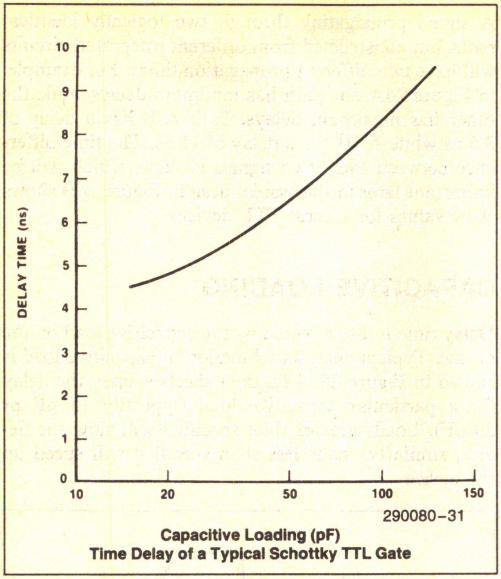


Figure 25. Capacitive Loading

A value of 0.05 ns/ft is a linear approximation of the function in Figure 25 and is used in the calculations. Loading effect is calculated by subtracting the actual load from the specified load. This difference is multiplied by 0.05 ns/pF and the result algebraically subtracted from the specified delay. As an example, a device has a 4 ns delay driving 50 pF, but the actual load is 25 pF. Then,

$$\begin{array}{r} 50 \text{ pF specified} \\ -25 \text{ pF actual} \\ \hline 25 \text{ pF difference} \end{array}$$

$$25 \text{ pF} \times 0.05 \text{ ns/pF} = 1.25 \text{ ns}$$

$$\begin{array}{r} 4 \text{ ns specified} \\ -1.25 \text{ ns difference} \\ \hline 2.75 \text{ ns actual delay} \end{array}$$

A device specified at 4 ns while driving 50 pF will have a delay of only 2.75 ns when driving 25 pF. Conversely, the same device driving 75 pF would have a propagation time of 5.25 ns.

TRANSIT TIME

Signal transit time, the time required for the signal to travel down the PC trace, must also be considered. As was shown in Figure 19, these traces are transmission lines. Classical transmission line theory can be used to calculate the delay:

$$t_p = \sqrt{LC}$$

where: t_p = Travel Time
L = Inductance/unit length of trace
C = Capacitance/unit length of trace

The capacitance term in the equation is modified to include the sum of the trace capacitance and the device capacitance. This equation approximates in the worst case direction; a signal will never "see" all the load capacitance simultaneously, it is distributed along the trace at the devices.

Substituting into the equation:

$$tp^1 = \sqrt{L(C + C_L)}$$

where: tp^1 = Modified delay
C_L = Load capacitance

Algebraically:

$$tp^1 = \sqrt{LC(1 + C_L/C)}$$

$$tp^1 = \sqrt{LC}\sqrt{1 + CL/C}$$

and

$$tp^1 = tp\sqrt{1 + CL/C}$$

Empirically, tp is 1.8 ns/ft for G-10 epoxy and C is 1.5 pF/in. For a 5-in. trace and a 40 pF load, the delay is calculated to be 4.5 ns. Because this is worst case, an approximated 2 ns/ft can be used. In the following sections, however, the equation will be used. Total delay is the summation of all the delays. Adding the device access, TTL delays and the trace delays result in the system access.

BOARD LAYOUT

The preceding section discussed the effects of trace length and capacitive loading. Proper board layout minimizes these effects.

As shown in Figure 26, address and control lines are split into a right and left hand configuration with these signals driving horizontally. This configuration minimizes propagation delay. Splitting the data lines is not necessary, as the data loads are not as great nor are their traces as long as address and control lines. Control and timing fills the remaining space.

Two benefits are derived from this layout. First, the address and control lines are perpendicular to the data lines which minimizes crosstalk. Second, troubleshooting is simplified. A failing row of devices indicates a defective address or control driver; whereas a failing column indicates a faulty data driver.

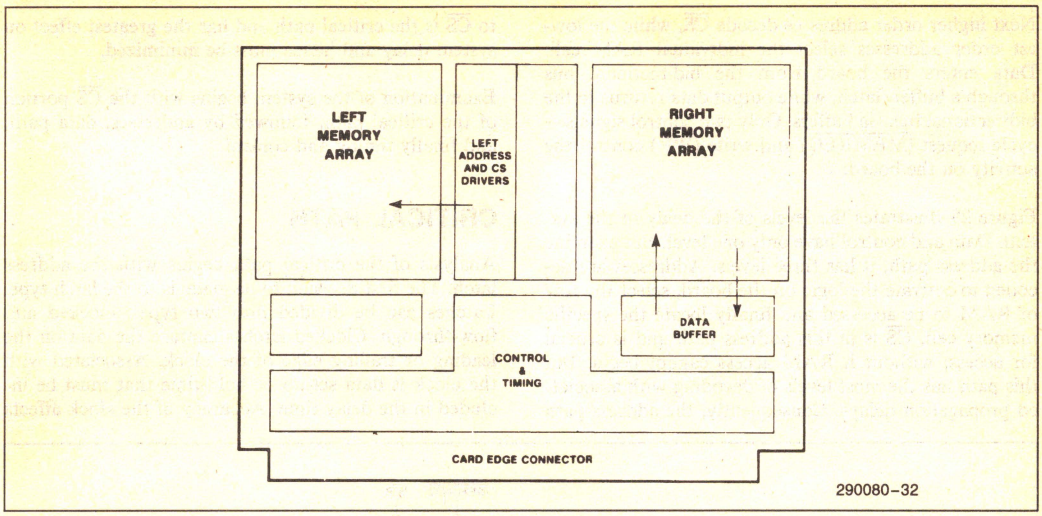


Figure 26. Board Layout

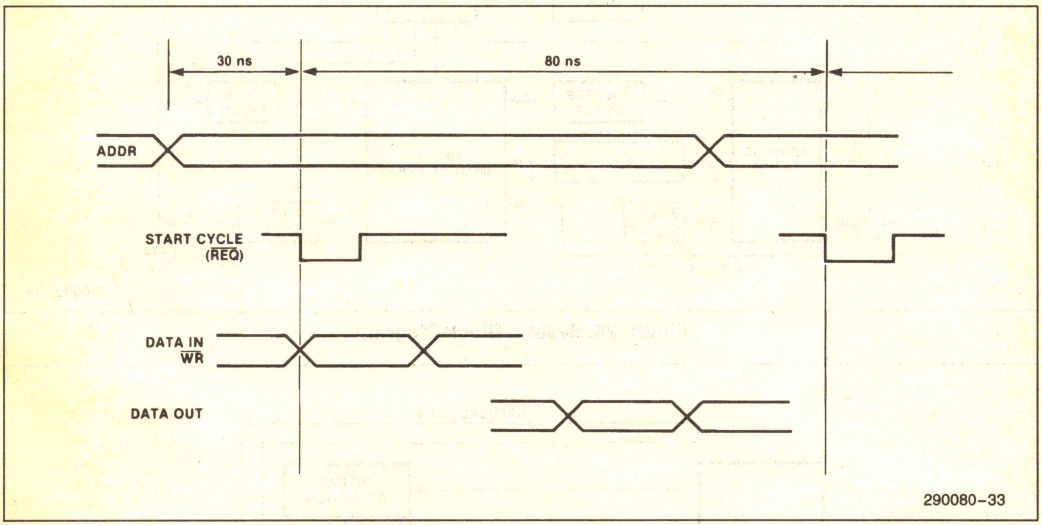


Figure 27. System Timing

SYSTEM DESIGN

Using previously discussed rules and guidelines, the design of a typical high speed memory will be reviewed to illustrate these techniques. Configuration of the system is a series of identical memory cards containing 16K words of 16 bits. Timing and control logic is contained on each board. System timing requires an 80 ns cycle as shown in Figure 27. Cycle operation begins when data and control signals arrive at the board. In this design, addresses are shifted 30 ns to be valid before the start of the cycle so that address, data, and control arrive at the memory device at the same time for maximum performance. Data and control signals are coincident with the start of the cycle. Access is not yet specified because it is affected by device access and the unknown propagation delay. Access will be determined in the design.

Figure 28 illustrates the elements of the system in block diagram form. Addresses are buffered and latched at the input to the printed circuit card. Once through the latch, the addresses split to perform three functions: board selection, chip select ($\overline{CS}$) generation, and RAM addressing. Highest order addresses decode the board select, which enables all of the board logic including $\overline{CS}$.

Next higher order addresses decode $\overline{CS}$, while the lowest order addresses select the individual RAM cell. Data enters the board from the bidirectional bus through a buffer/latch, while output data returns to the bidirectional bus via buffers. Only two control signals—cycle request ($\overline{MEMREQ}$) and write ($\overline{WR}$) control the activity on the board.

Figure 29 illustrates the levels of the delay in the system. Data and control have only one level. But examine the address path, it has three levels. Addresses are decoded to activate the logic on the board, select the row of RAM to be accessed and finally locate the specific memory cell. $\overline{CS}$ is in this address path and is crucial for access; without it RAM access cannot begin. But this path has the most levels of decoding with associated propagation delays. Consequently, the address path to $\overline{CS}$ is the critical path and has the greatest effect on system delay and hence must be minimized.

Examination of the system begins with the $\overline{CS}$ portion of the critical path, followed by addresses, data path, and finally timing and control.

CRITICAL PATH

Analysis of the critical path begins with the address latch. The first decision to be made is to the latch type. Latches can be divided into two types: clocked and flow-through. Clocked latches capture the data on the leading or trailing edge of the clock. Associated with the clock is data set-up or hold-time that must be included in the delay time. Accuracy of the clock affects

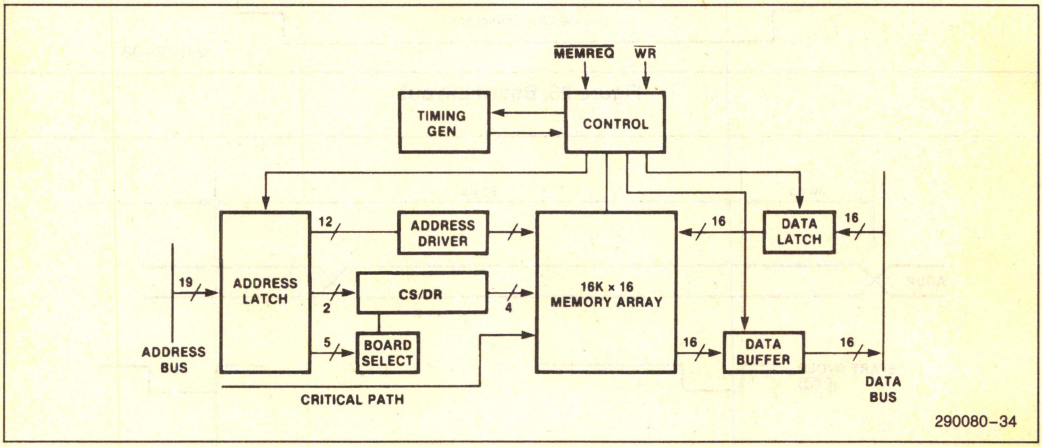


Figure 28. System Block Diagram

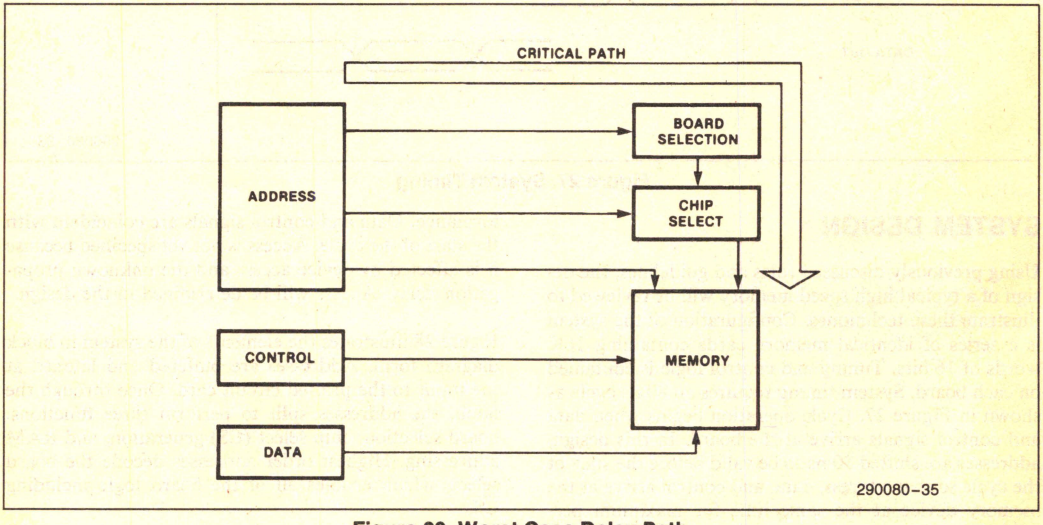


Figure 29. Worst Case Delay Path

the transit time of the signal because any skew in the clock adds to the delay time. As an example, a typical 74S173 latch has a data set-up time of 5 ns and a maximum propagation delay time from the clock of 17 ns. Total delay time is 22 ns, excluding any clock skew.

Flow-through latches have an enable rather than clock. The enable opens the address window and allows addresses to pass independent of any clock. Delay time is measured from the signal rather than a clock. The Intel 3404 is a high speed, 6-bit latch operating in a flow-through mode with 12 ns delay. This is acceptable but a faster latch can be fashioned using a 2-to-1 line multiplexer, either a 74S157 or a 74S158. The slower of the two is the 74S157 with 7.5 ns delay. Although the 74S158 is faster with 6 ns delay, it requires an extra inverter in the feedback path as shown in Figure 30. Between the 74S157 and the 74S158 latches, the trade off is speed against board space and power. Individual designers will choose to optimize their designs.

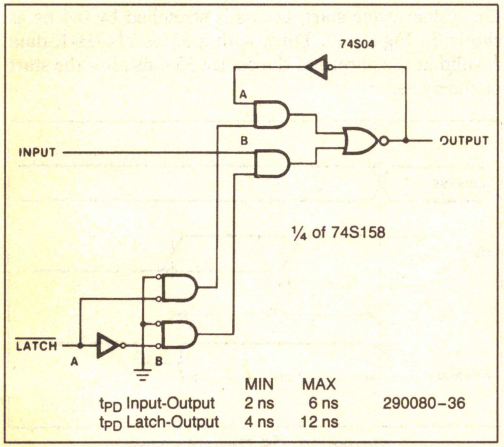


Figure 30. Fast Latch

In either case, care must be exercised in constructing the latch. Output data must be fed back to the input having the shortest internal path—the A input. If the latch is constructed with the output strapped to the B input, the input could be deselected and the feedback loop not yet selected because of the delay through the internal inverter. In this situation data would be lost. Additional delay through the external inverter (74S04) aids in preventing data loss. Inverting addresses has no system effect—except that it's faster than the non-inverting latch. During a write cycle, data will be stored at the compliment of the system address. When this data is to be retrieved, the same address will be complimented, fetching the correct word.

The remaining elements in the critical path to be designed are board selection and $\overline{CS}$ decoding. To minimize the $\overline{CS}$, decode path, the easiest method is to work backwards from $\overline{CS}$. In this manner input signals to a stage are determined and the output from the preceding stage is defined. This saves inserting an inverter at the cost of 5 ns to generate the proper input to a stage.

Starting with the $\overline{CS}$ driver, the design analyzes several approaches to select the fastest one. With four rows of devices, there are four $\overline{CS}$ signals to be generated. A 2-to-4 line decoder like the 74S138 is a possible solution. It is compact, but has two detriments: long propagation delay and insufficient drive capability. Propagation delay from enable is 11 ns. Enable is driven by board selection which arrives later than the binary inputs. Splitting the RAMs into two 4 x 8 arrays eases the drive requirement but the demultiplexer must still drive eight devices at 5 pF each—or 40 pF total—which adds 1.75 ns to the delay. More importantly, signal drive is required to switch cleanly and maintain levels in spite of crosstalk and reflections. A 74S240 buffer will solve this but in the process consumes an additional 9 ns.

A second and preferred approach is to use a discrete decoder to decode and Drive the $\overline{CS}$ signals. Four input NAND buffers—74S40—fulfill this function. Addresses A_{12} and A_{13} are inverted via 74S04, providing true and compliment signals to the buffer for decoding. As shown in Figure 31, the delay is 11.5 ns. Propagation delay for the 74S40 is specified into a 50 pF load, eliminating the additional loading delay. Left and right drivers—CSXL and CSXR—are in the same package to minimize skew between left and right bytes of data. All of the decoders are enabled by Board Select to prevent rows of devices on several boards from being simultaneously active. Board Select is a true input, defining the output from the Board Select decoder.

In the Board Select decoder, the high order addresses are matched to hard-wired logic levels generated with switches for flexibility. Changing a switch setting shifts the 16K range of the board. Comparison of the switch setting and the address can be accomplished with an exclusive-OR, a 74S86. NANDing all the exclusive-OR outputs will generate a Board Select signal. Unfortunately, this signal is active-low, requiring an additional inverter as in Figure 32A, and it also consumes 22.5 ns to decode. An MSI solution to board selection is a 4-bit comparator—74S85—which consumes less board area and propagation delay is improved at 16.5 ns.

The best solution is attained by inverting the high order addresses to generate true and compliment signals. The appropriate signal is connected into a 74S260, 5-input NOR. With an active-high output, maximum delay is 11 ns as in Figure 32B.

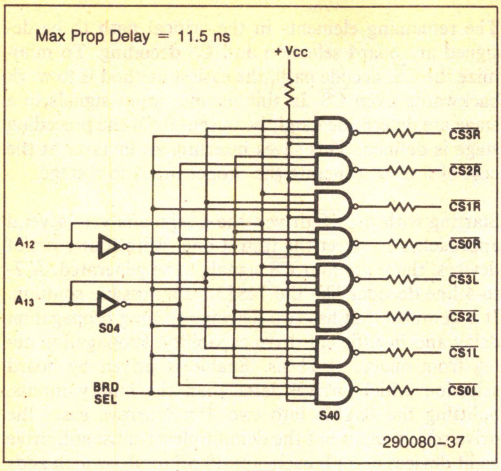


Figure 31. $\overline{CS}$ Decode

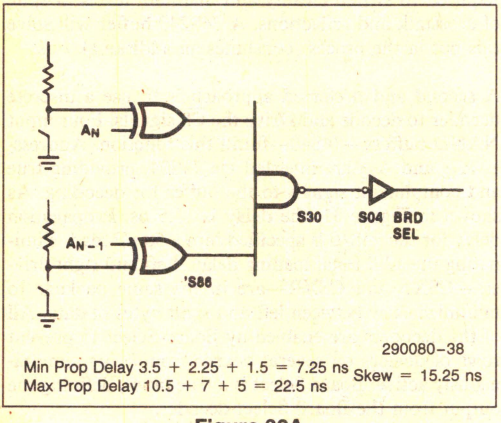


Figure 32A

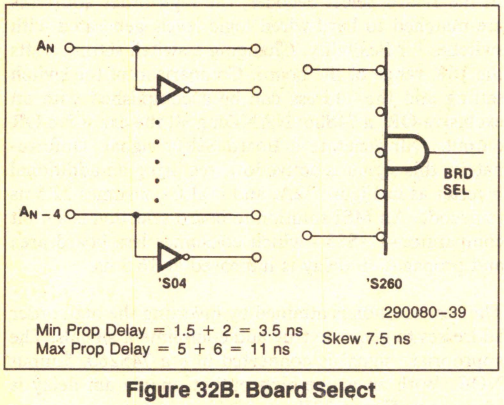


Figure 32B. Board Select

Critical path timing is the sum of the latch, Board Select, and $\overline{CS}$ delay times. In this example, latch delay is 6 ns, Board Select is 11 ns and $\overline{CS}$ decode is 11.5 ns for a total of 28.5 ns. One additional delay—trace delay—must be included for a complete solution. Each 74S40 drives eight MOS inputs having 5 pF/device for a load of 40 pF. Trace capacitance is calculated on 5 in. of trace. At 1.5 pF/in., trace capacitance is 7.5 pF. Trace delay calculated from equation 3 is 1.9 ns.

$$tp1 = \frac{1.8\text{ ns}}{\text{ft}} \times \frac{5\text{ in.}}{12\text{ in./ft}} \sqrt{1 + \frac{40\text{ pF}}{7.5\text{ pF}}}$$

$$tp1 = 1.9\text{ ns}$$

Total worst case maximum critical path delay has been calculated to be 30.4 ns (28.5 ns + 1.9 ns). With the addresses shifted in time by an amount equal to the worst case delay, device and system cycle start are coincident. Start of system access and device access differ only 0.4 ns when the addresses are shifted 30 ns. From the system cycle start, access is stretched by 0.4 ns as shown in Figure 33. Thus, with a 35 ns 2147H-1, data is valid at the output of the device 35.4 ns after the start of the cycle.

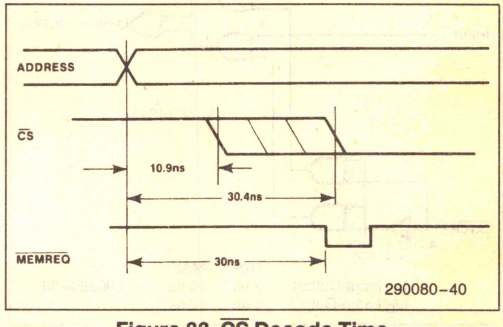


Figure 33. $\overline{CS}$ Decode Time

The minimum delay also must be calculated. With addresses valid prior to the start of the cycle, $\overline{CS}$ decoding can start in the previous cycle. If it occurs too soon, the previous cycle will not be properly completed. Minimum delay time is the sum of the minimum propagation delays plus capacitive loading delay plus trace delay. Capacitive loading delay is less than 0.4 ns and ignored. Minimum delay through the TTL is 9 ns, and added to trace delay results in a total of 10.9 ns.

From address change, the maximum delay in the critical path is 30.4 ns while the minimum is 10.9 ns. The difference between these two times is skew and will be important in later calculations.

ADDRESSES

Lower order addresses (A_0–A_{11}) arrive at the devices earlier than $\overline{CS}$ because they are not decoded. Consequently, the address drivers do not have a critical speed requirement. Once through the 6 ns latch, addresses have 24 ns to arrive at the devices.

While speed is not the primary prerequisite, drive capability is. Address drivers are located in the center of the board, dividing the array into two sections of 32 devices each. For the moment, assume one driver drives 32 devices as in Figure 34A. Each device is rated at 5 pF/input, resulting in a load of 160 pF. In addition, there are four 5-in. traces—one for each row. Twenty inches of trace equates to 30 pF. Total capacitive load is 190 pF. A 74S04 is specified at 5 ns delay into 15 pF. The increased capacitive load is 175 pF, which at 0.05 ns/pF increases the delay by 8.75 ns. Under these conditions the worst case driver relay is 5 ns plus 8.75 ns, totaling 13.75 ns. It is 10 ns earlier than the 24 ns available.

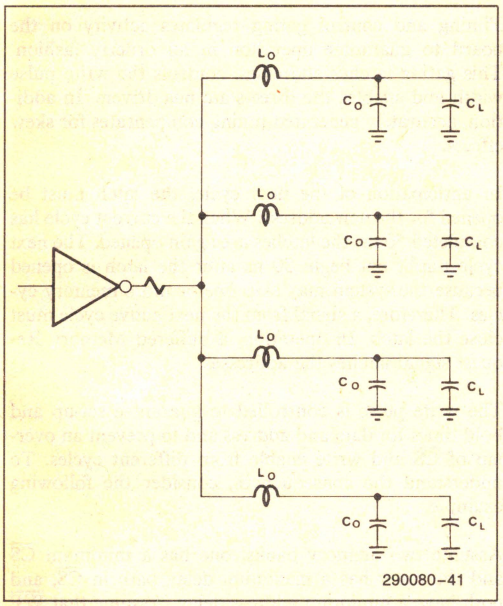


Figure 34A. Address Driver

The first impression is that this is sufficient, but the effect of crosstalk must be considered. For example, as shown in Figure 35, each trace has inductance, and parallel traces take on the characteristics of transformers. When a signal switches from a one level to a zero level, its driver can sink 20 mA, inducing a transient in an adjacent trace. If the adjacent signal is switching to a one level, only 400 μA of a source current from the driver is available. The induced current will generate a

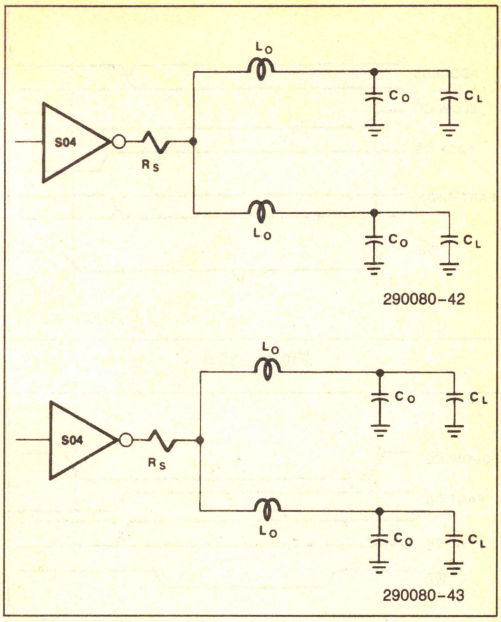


Figure 34B. Address Drivers

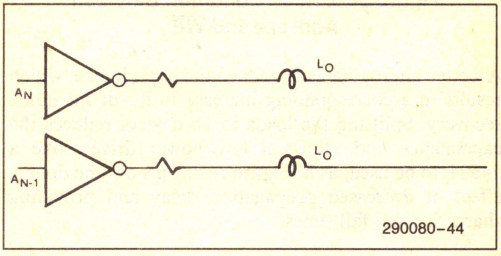


Figure 35. Cross Talk

negative spike, driving the signal at a one level negative. Additional time of 10 ns to 15 ns is required to recover and re-establish a stable one level. This may prevent stable address at the start of the cycle. Recall:

$$i = C\frac{dv}{dt} \text{ or } dt = C\frac{dv}{i}$$

where: i = instantaneous current
C = capacitance
$\frac{dv}{dt}$ = voltage time rate of change

The term dv/dt can be maximized by increasing i or decreasing C. Current can be doubled by using a driver like a 74S240, but it draws 150 mA supply current. In a large system the increased power is a disadvantage because it requires a larger power supply and additional cooling.

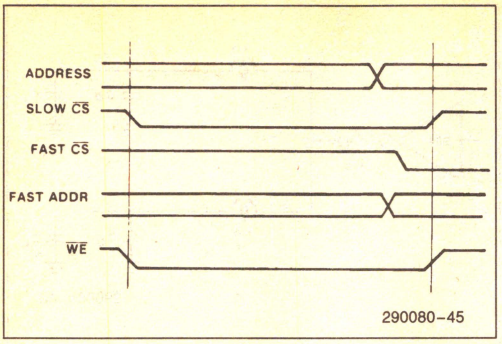


Figure 36A

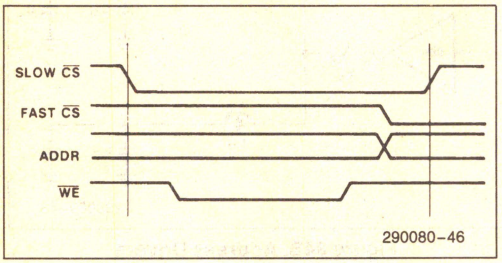


Figure 36B. Race Condition Between Address and $\overline{WE}$

A better alternative is to reduce the capacitance, which results in a corresponding increase in dv/dt for quick recovery. Splitting the loads to 16 devices reduces the capacitance and allows a low power driver, like a 74S04, to be used, as in Figure 34B. This has the double effect of decreased propagation delay and providing sharp rise and fall times.

Now, there are only 10 in. of trace or 15 pF load and 16 devices, representing 80 pF for a total of 95 pF. Again, the S04 delay is 5 ns into 15 pF, but the stretched delay due to 80 pF is only 4.0 ns for a total of 9.0 ns. Stable addresses are guaranteed at the start of the cycle.

DATA PATH

Next in line for analysis is the data path. Reference to the system block diagram shows that the data is latched into the board on a write cycle and buffered out during a read cycle. Data latches are constructed from 74S158 quad two-input multiplexers. Because the data bus is bidirectional, 74S240 three-state drivers are used for output buffers.

All that remains to complete the board access computation is the calculation of the output propagation delay. Output delay of the active RAM is caused by the capacitance loading of its own output plus the three idle RAMs, the input capacitance of the 74S240 bus driver and trace capacitance. Output capacitance of the 2147Hs is 6 pF/device for a subtotal of 24 pF; input capacitance of the 74S240 is 3 pF and trace capacitance of a 5-in. trace is 7.5 pF. Total load capacitance is 34.5 pF, and access time of the 2147H is specified driving a 30 pF load. Calculated loading is close enough to the specified loading to eliminate any significant effect on the access calculations. Had there been a difference, the effect would have been included in the calculation. As previously calculated, transit time of the trace is 1.6 ns. Adding this to the 7 ns delay through the 74S240 bus driver results in an 8.6 ns output propagation delay from the RAM output to the bus.

Total access is 35.4 ns plus 8.6 ns output delay for a total access of 44 ns. The efficiency of this system is:

$$\text{Eff} = \frac{35}{44} \text{ or } 80\%$$

TIMING AND CONTROL

Timing and control gating regulates activity on the board to guarantee operation in an orderly fashion. This gating latches addresses, controls the write pulse width and enables the three-state bus drivers. In addition, accurately generated timing compensates for skew effects.

In anticipation of the next cycle, the latch must be opened for the new address. When the current cycle has completed 50 ns, the latches are again opened. The next cycle might not begin 30 ns after the latch is opened because the system may skip one or more memory cycles. Therefore, a signal from the next active cycle must close the latch. In operation, a buffered Memory Request signal latches the addresses.

The write pulse is controlled to guarantee set-up and hold times for data and address and to prevent an overlap of $\overline{CS}$ and write enable from different cycles. To understand the consequences, consider the following example.

Assume two memory banks, one has a minimum $\overline{CS}$ and the other has a maximum delay path in $\overline{CS}$, and both have a minimum address delay. Assume that $\overline{WE}$ is a level generated from a write command as shown in Figure 36A. The operation under examination is a write cycle into the bank with fast $\overline{CS}$ followed by a read cycle into the bank with slow $\overline{CS}$.

Both the write cycle and the read cycle have device specification violations. In the write cycle, the addresses change prior to $\overline{CS}$ and $\overline{WE}$ becoming inactive; that new address location may be written into. In the read cycle, the address change is correct but $\overline{WE}$ is still active and the fast $\overline{CS}$ begins too soon, performing a nonexistent write cycle. Clearly, controlling the width of $\overline{WE}$ will solve the problems.

Figure 36B shows the proper operation controlled with timing.

Finally, the data output buffers, controlled by timing signals are enabled only during a read cycle while the board is selected preventing bus contention with two or more boards in the system. More importantly, timing disables the output prior to the start of the next cycle, allowing input data to be stabilized on the bidirectional data bus in preparation for a write cycle.

TIMING GENERATION

Having discussed the philosophy of timing and control, we can now focus on the specifics of address latching, write pulse generation and output-enable timing. To perform these functions timing can be generated from one of three sources: clock and shift register, monostable multivibrator, or delay line.

CLOCKED SHIFT REGISTER

A clocked shift register circuit is shown in Figure 37 consisting of a D-type flip-flop and an 8-bit shift register.

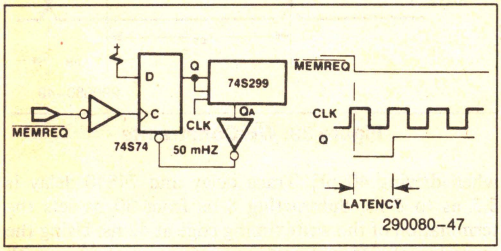


Figure 37. Flip-Flop and Shift Register

On the leading edge of $\overline{\text{MEMREQ}}$, the Q output of the D flip-flop is clocked to a one state, enabling a "one" to be propagated through the shift register. The one is clocked into the first stage of the shift register on the first clock edge after the A and B inputs are "ones." After the clock, the output Q_A goes true which subsequently clears the D flip-flop, clocking zeroes into the register to create a pulse one clock period wide.

The accuracy and repeatability depends primarily on the accuracy and stability of the clock. Crystal clocks can be built with +0.005% tolerance and less than 1% variation due to temperature.

An inherent difficulty is the synchronization of Memory Request and the clock. At times there will be a latency of one clock cycle between Memory Request and the actual start of the cycle when Memory Request becomes active just after the clock edge. Assuming an 80 ns cycle and 20 ns clock, the latency can be 20 ns or 25% of a cycle stretching both access and cycle accordingly. A second difficulty of this circuit is caused by the asynchronous nature of the clock and the Memory Request. The request becomes active just prior to the clock and the set-up time of the latch is violated, the output Q_A "hangs" in a quasi-digital state and could double or produce an invalid pulse width; this and the latency hinder effective use in high speed design.

MONOSTABLE MULTIVIBRATOR

The second possible timing generator is a series of monostable multivibrators, using a device such as the AMD Am 26S02 multivibrator. It has a maximum delay from input to output of 20 ns and an approximate minimum of 6 ns. However, with a delay of 20 ns, the monostable multivibrator offers no advantage over the clocked generator. Having a minimum pulse width of 28 ns, the one-shot offers no improvement over the 50 MHz clock, but in fact the performance is worse because it is more temperature and voltage sensitive. The pulse width is dependent on the RC network composed of resistors and capacitors that are temperature sensitive. Consequently, repeatability leaves something to be desired.

DELAY LINE

The third and best choice is a delay line. This design uses STTLDM-406 delay lines from EC[2] with tapped outputs at 5 ns increments. In operation, Memory Request activates an R-S flip-flop fabricated from cross-coupled NAND gates. The output of this circuit starts the memory cycle. Consequently, the cycle starts 5 ns after Memory Request compared to 20 ns for the other two timing generators. The leading edge travels down the delay lines. When the edge reaches the 25 ns tap, the output is inverted and fed back to the R input of the R-S flip-flop, shaping the pulse to width to 25 ns. Twenty-five nanoseconds was chosen to match as close as possible the write pulse width. A 25 ns pulse limits the Memory Request signal width to less than 25 ns to insure proper operation. Otherwise, the R-S flip-flop will not clear until Memory Request returns to a one level. As the pulse travels down the delay lines, it acquires additional skew of ±1 ns per delay line package for a total of 6 ns overall. Figure 38 shows several timing pulses and the uncertainty of each edge calculated by worst case timing analysis. The remaining problem is selection of timing edges to operate the device. Now that the timing chain is completely defined, specific details of the address latch, write pulse and output enable can be completed.

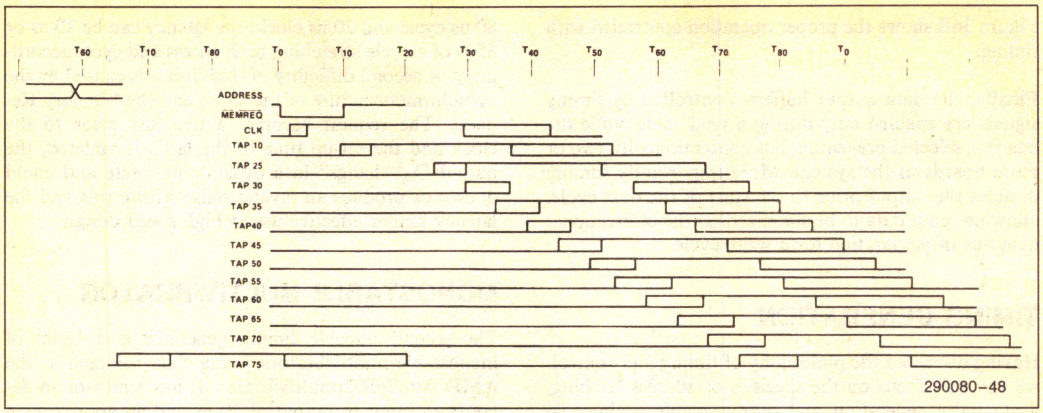


Figure 38. Timing Chain

ADDRESS LATCH TIMING

An R-S flip-flop activated by MEMREQ latches the addresses. A second signal which we will now calculate is used to open the latch. This signal has two boundaries. If the latch opens too late, the access of the cycle will be extended; if it opens too soon, the current cycle will be aborted. Skew through the R-S flip-flop is 1.75 ns to 5.5 ns and skew in the latch from enable to output is 4 ns to 12 ns for a total skew of 6 ns to 17.5 ns. With this skew added to the 30 ns address set-up time, the latch opening signal must be valid at 36 ns best case or 47.5 ns worst case prior to the start of the memory cycle. Each cycle is 80 ns long, therefore, the latch opening signal must begin 44 ns or 32.5 ns, respectively, in the preceding cycle. From the delay line timing diagram, T35 will satisfy the worst case requirements for opening the latch and T25 best case. In production, each board is tuned by selecting T25, T30, or T35 to open the latch, guaranteeing it opens between 35 ns and 30 ns prior to the start of the cycle.

WRITE PULSE TIMING

The next timing to be calculated is the write pulse. Figure 39 shows the three parameters which define the write pulse timing: data set-up time, write pulse width and write recovery time. Data set-up is assured by having data valid through the entire cycle.

Placement of $\overline{WE}$ in the cycle is controlled by address change to comply with t_{WR}. From previous calculations the earliest addresses can change is 50 ns, which defines the end of the $\overline{WE}$ signal. Our calculations begin at the device and work back to the timing edge. Eight devices constitute a 40 pF load and a 74S40 is specified for a 50 pF load, reducing delay by 0.5 ns

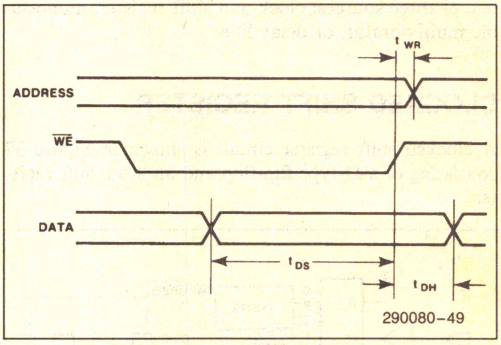


Figure 39. $\overline{WE}$ Constraints

when driving 40 pF. Trace delay and 74S40 delay is 3.5 ns to 8 ns. Subtracting 8 ns from 50 ns sets the termination of the write timing edge at 42 ns. Using the inversion of T25 will end the write pulse at 43 ns with 7 ns to spare.

Data set-up time is guaranteed because data is valid 6 ns (the worst case delay through the latch) after the start of $\overline{MEMREQ}$.

OUTPUT ENABLE TIMING

There is a 5.5 ns delay through the address driver providing minimum device cycle of 50 ns. As a result the earliest data can disappear from the bus is at 54 ns because of delay through the output circuit. To select the timing tap for the output enable, the skew of the enable circuit is subtracted from the system access time.

Subtracting the 28 ns skew of the buffer enable circuit from the 44 ns access time of the system shows that the latest the timing edge can occur is 16 ns, which is satisfied by edge T10. The trailing edge, however, ends at 37 ns and with minimum propagation delays the bus

would become three-stated at 44 ns, coincident with data becoming valid. ORing T20 with T10 will guarantee the output is valid until 54 ns, minimum. Selecting a timing gap between T35 and T50, depending on the propagation delay in the enable circuit, disables the output at 70 ns, allowing input data to be valid for 10 ns prior to start of cycle. The complete schematic is shown in Figure 40.

SUMMARY

The 2147H is an easy-to-use, high speed RAM. The problems in a memory system design are the result of inherent limitations in interfacing. Largest of these is skew, which the designer must strive to minimize. In this example, skew consumed 45 ns of an 80 ns cycle while device access time was extended by only 10 ns, resulting in an 80% efficiency.

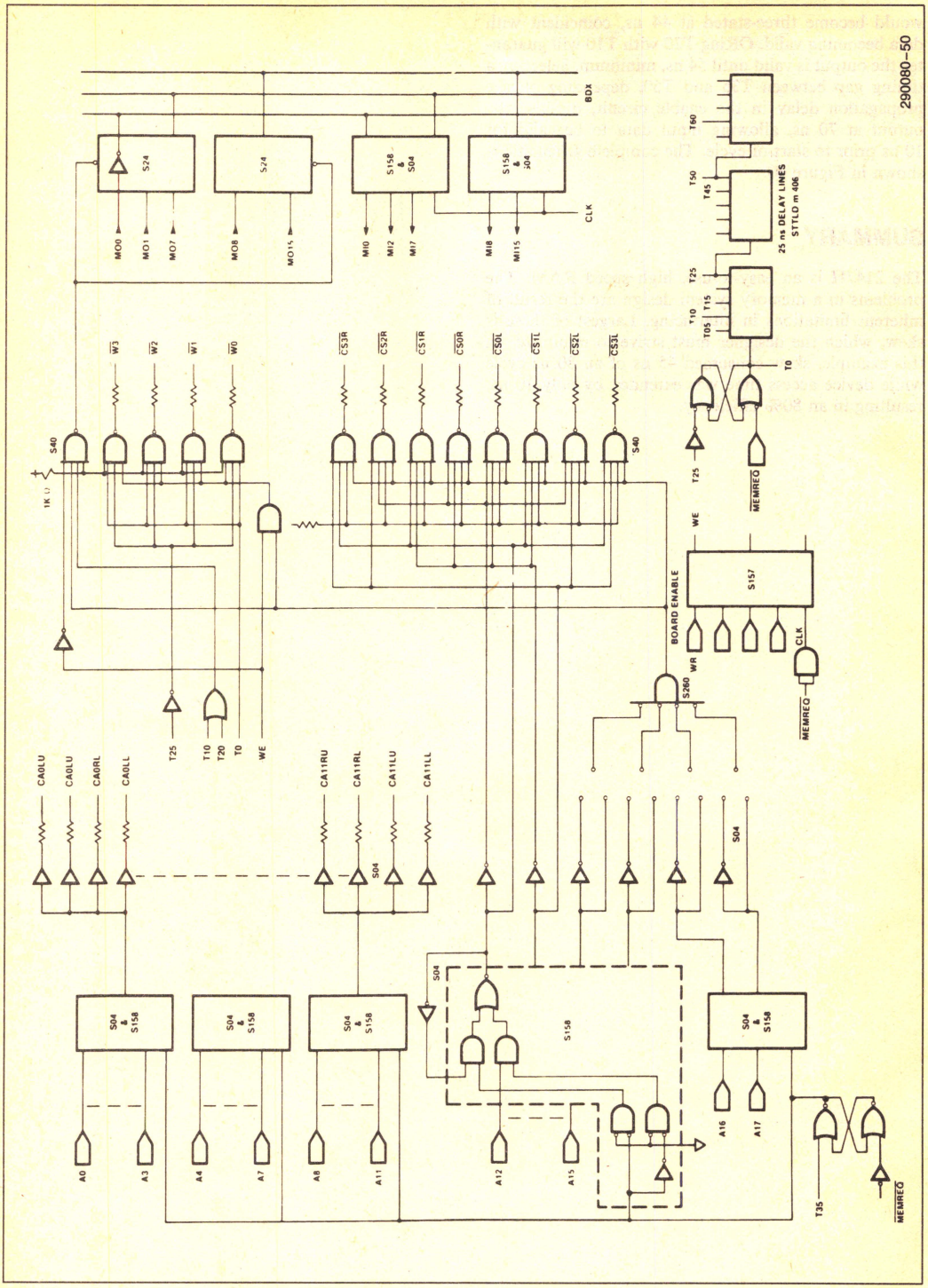


Figure 40. 16K x 16-Bit High Speed Static Memory

intel®

APPLICATION NOTE

AP-238

March 1985

Memory Design For The Low Power Microsystem Environment

DENNIS KNUDSON
MEMORY COMPONENTS

Order Number: 280103-001

1.0 INTRODUCTION

1.1 The Low Power Environment

The low power environment, as discussed in this document, refers to microsystems that have low power as a major feature of the design. The purpose here is to provide some guidelines for designing such systems—particularly the memory subsystems. The topics covered include descriptions and trade-offs of various types of memory components, system design examples and discussions of batteries and power switching circuitry.

1.2 Elements

Generally, the low power environment has two basic elements: active and standby power. With respect to memories, another element—the data retention power—is equally important. As discussed in this document, active power is simply the power required during an access to memory. Standby power is that required while the memory is between accesses. Data retention power is the minimum power required to maintain data in the memory.

1.3 Applications

Low power applications in general are divided into those using AC line power and those using batteries either as primary power or as backup power for memory maintenance and/or memory protection. Active or primary power for systems is fairly simple and can be provided by either the AC line or batteries. Back-up power subsystems consists of circuitry supported by batteries only during the absence of regular power. It includes the system memory, batteries and power switching circuits. When in the backup power mode, the batteries provide power to the memory and the support circuits necessary to maintain the stored information. When power fails, the power switching circuits must shut down all of the system except the memory and its support circuits. In so doing, they must provide a clean, glitch-free and orderly transition from line power to battery power. When line power returns, they must transfer control from the battery powered circuits back to line powered circuits, again in an orderly, glitch-free manner.

In the backup power applications, only those components required to maintain volatile memory data when power is removed, or those required to protect the data when power fails need to be low power devices. Some examples are systems requiring fast, non-volatile storage (RAMs) or power failure protection for on-line memory. They include, but are not limited to battery powered systems. For example, when used for storage such as solid state disks, CHMOS DRAMs allow the user to operate directly out of mass memory but they require battery backup to maintain the data whenever the system is powered down.

In battery powered systems or subsystems, all components are battery supported and as such must consume little power. Such systems must be able to run on each set of batteries for an acceptable period defined by the application. When using re-chargeable batteries, the system should run on each charge for the longest likely continuous use in the specific application and recharge time should be acceptable for the probable frequency of use. Obviously, the more power drawn by the compoments of the system, the bigger the battery required or the shorter the operating time. Above all, a battery powered system design should avoid components or sub-systems that will require special cooling accommodations (i.e. fans).

1.4 Design Considerations

When designing low power memory systems with standard TTL drivers, standby power can be as little as two percent of the active power. To achieve the low standby power possible with CMOS memories, pull-up resistors must be used on all critical control lines and the TTL must be powered down. This requires special considerations. A more effective method is to use CMOS logic.

Newer CMOS products are ideal for these types of applications because they provide the speed required when the system is operating, and dissipate very little heat in the process when compared to NMOS products. When in backup or data retention mode, they require about two tenths of one percent of their active power to maintain information. CMOS drivers for the memory system reduce standby power to its lowest level—lower, typically by a factor of 40, than TTL standby power consumption. The implications to the system designer are lower cooling requirements and smaller power supplies of batteries(1).

2.0 MEMORY OPTIONS FOR LOW POWER OR NON-VOLATILE STORAGE

In this section we will look at various types of memory suitable for low power applications. Typically, memories used in this type of system are CMOS RAMs for their low power and high speed features. Bubble memories are useful here for mass storage if the application requires long term storage without power. For relatively short term storage, power consumption for the bubble can be reduced by power switching(2). E^2PROMs and CMOS EPROMs, also non-volatile, can be used for small, permanent or semi-permanent software storage such as firmware and operating system kernels.

NVRAMs would be useful for buffer storage on a communications data link or in small, fast local memory requiring data retention without power. In 1972, Signetics introduced the 25120 write only memory (WOM) but no lasting applications have developed so it will not be covered here.

2.1 Magnetic Bubble Memory

The bubble memory is a rugged, non-volatile, serial-in/serial-out storage medium. Both the one megabit (7110) and the four megabit (7114) operate at 50 KHz. Briefly, the MBM operates by rotating an external magnetic field to propel a cylindrical magnetic domain (bubble) through a film or magnetic material. Externally, it handles data in a serial fashion similar to magnetic disc or drum storage systems but, without the noise or moving parts, it is faster, more reliable and uses much less power.

Magnetic bubble memory is smaller than any other memory storage system and cost/bit is second only to the dynamic RAM. It is the slowest and has the highest operating and standby power requirements of all solid state memories but it can retain data indefinitely when power is removed.

A complete bubble memory kit consists of the bubble memory, controller, current pulse generator, formatter, coil pre-driver and drive transistors. The kit requires two voltages and dissipates about 1.5 watts in standby and 3.5 watts active per bubble component. Rugged and truly non-volatile, it has many applications including robotics, oil exploration, aircraft navigation and test equipment.

2.2 EPROMs

Non-volatile read-only-memories, EPROMS are erased under ultraviolet light and then re-programmed electrically. They are programmed by injecting "hot" electrons (typically created by a 12.5 volt Vpp) into the floating (isolated) gate of the transistor. Capacitively coupled to the select gate of the transistor, this charge adds to the select gate charge, altering the threshold voltage of the transistor. They are erased by ultraviolet light which induces enough energy into the floating gate to cause the excess electrons to overcome the energy barrier between the floating gate and the insulator surrounding it. Thus, the electrons are dissipated into the select gate and substrate of the transistor.

EPROMs must be removed from the circuit to be erased and re-programmed. In addition, they must first be completely erased before they can be re-programmed. Typical erasure times are 15 to 20 minutes. Program time is typically 5 minutes (27256 with Int$_e$ligent^{TM} programming) and access times of less than 250 nS are available. Through they do not have the flexibility of reading and writing data in real time, they are close to the dynamic RAM in density and they do not lose data when power is removed.

Some typical applications of EPROMs are firmware, operating system kernels, computer boot programs, communications, portable instruments, office equipment and commercial appliances. CHMOS EPROMs are faster and, with 25% of the active and 0.4% of the standby current of their NMOS counterparts, are well suited for storing initialization programs in low power systems.

2.3 E^{2}PROMs

Electrically erasable (E^2) PROMs use the same "floating gate" technology as EPROMs. The difference is that the charge is added or removed via a tunnel oxide in a phenomenon known as Fowler-Nordheim tunneling. At an energy level referred to as the "forbidden" band, the electrons are able to penetrate the oxide without ever reaching the energy level that standard mechanics would predict as being necessary to overcome the barrier[3]. This allows them to be erased and programmed IN-CIRCUIT and it permits individual byte programmability.

Active power is equivalent to that of static RAM but standby power is much higher, second only to magnetic bubble memory. It has the highest cost/bit and lowest density of the solid state memories except for Non-Volatile RAMs. Non-volatile and in-circuit reprogrammable, it is versatile in control functions and in data acquistion and communication systems requiring frequent system reconfiguration.

2.4 NVRAMs

Each cell of the Non-Volatile RAM consists of two memory cells, one static RAM and the other E^{2}PROM. Consequently, it is the least dense of all solid state memories. It functions as a static RAM during operation but provides non-volatile storage of data when powered off. A signal from the power supply indicating that power is being removed (or lost) causes the NVRAM to move the data from the SRAM cell into the E^{2}PROM cell. Thus, data that can be operated on at microprocessor speeds is automatically saved in non-volatile memory, combining the flexibility of SRAM with the long-term, power free storage of E^{2}PROM. Power and cost/bit are roughly equivalent to E^{2}PROMs.

2.5 SRAMs

Static Random Access Memories latch data into either four transistor (4T, for cost) or six transistor (6T, for low power) memory cells. Consequently, they do not need to be refreshed and access time is, essentially, cycle time. These features have historically contributed to the speed advantage of SRAMs over other memory types as well as to simple interface design. However, they also contribute to the density and power disadvantages of the SRAM. As data are gated out by addresses, they do not require clocks but may use one of two signals to control system interface. A chip enable $\overline{(CE)}$ may be used to provide a standby mode with reduced power and an output enable $\overline{(OE)}$ may be provided to release the data bus.

SRAMs are always one density generation behind dynamic RAMs because of the number of transistors per cell. The new CMOS SRAMs actually enjoy a power advantage over NMOS dynamic RAMs but the advantage is lost once again to dynamic RAMs on the CMOS process. Like dynamic RAMs, SRAMs are volatile memory, losing data when power is lost.

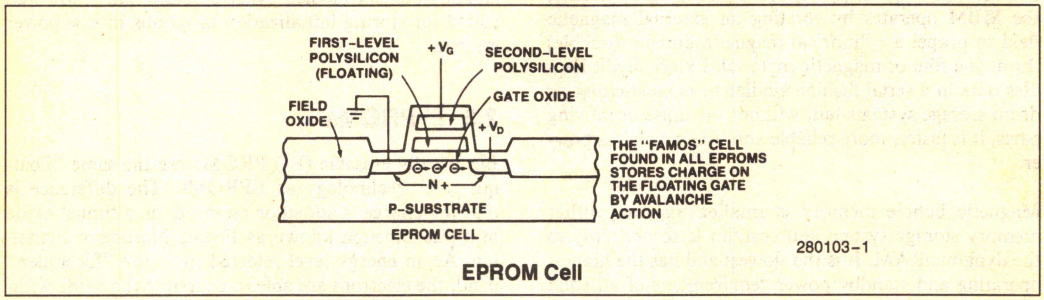


Figure 1. EPROM Cell

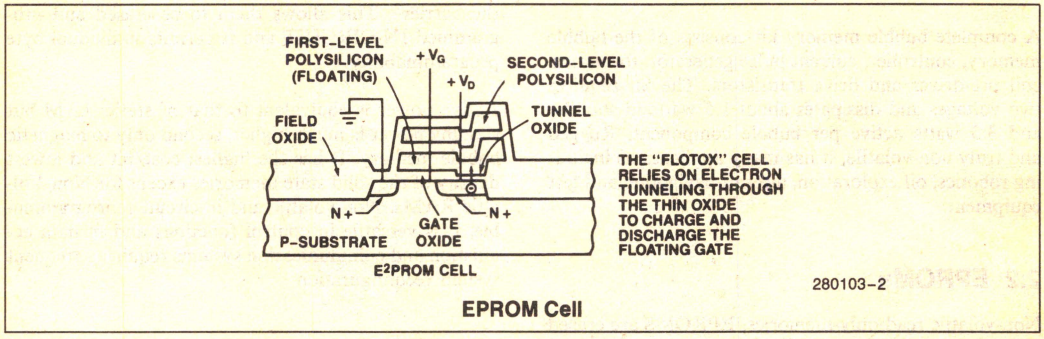


Figure 2. E²PROM Cell

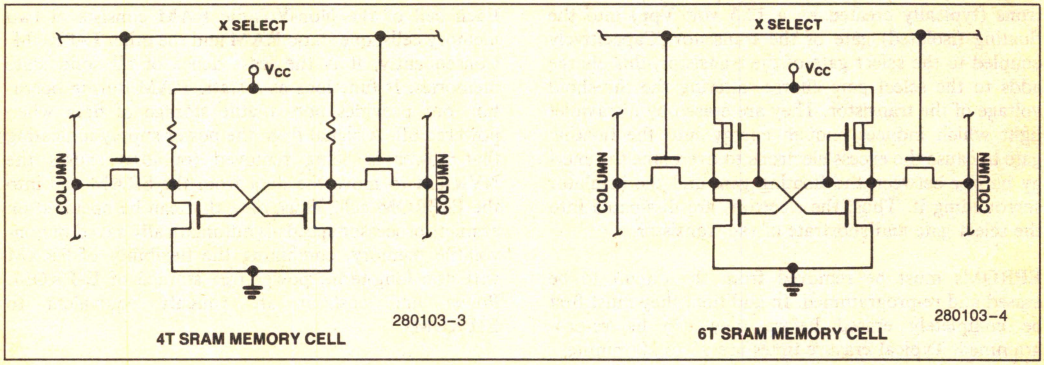
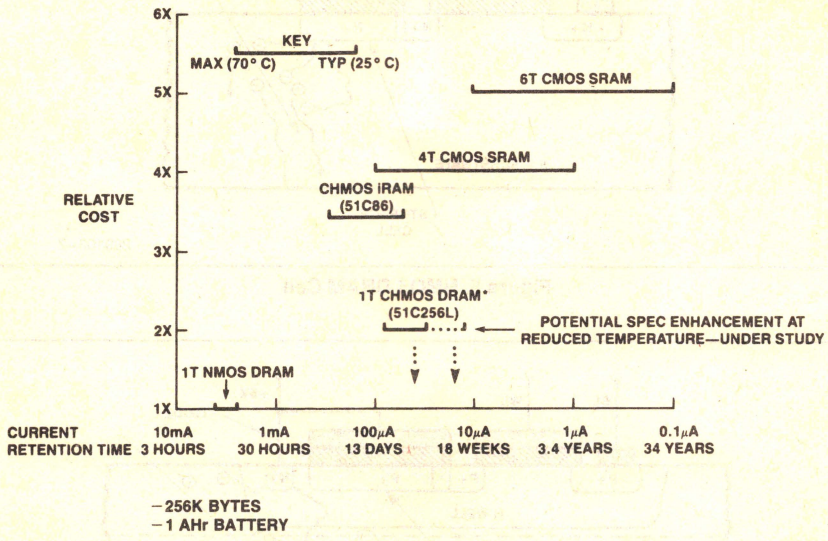


Figure 3. SRAM 4T and 6T Cells

MEMORY COST vs DATA RETENTION CURRENT/TIME (64K BIT EQUIVALENT)



NOTE:
*Includes controller and assumes extended refresh. See bibliography, Item 4

Chart 1

Some typical applications of SRAMs are in cache memories, bit slice processors, local microprocessor memory (less than 64K), video graphics and (with CMOS SRAMs) battery backup and battery powered systems.

2.6 iRAMs

The integrated RAM works like an SRAM but costs less. It is a dynamic RAM with an on-chip refresh circuitry and it is generally available in two versions, synchronously or asynchronously refreshing. The synchronous version has an on-chip refresh address generator and a "Refresh" input that allows the user to control the refresh occurrence.

The asynchronous version has a timer, refresh address generator, access arbiter and a "Ready" output. When a refresh request occurs coincident with an access request the arbiter resolves which will take precedence. Whenever an access request is held up by refresh, "Ready" goes low, causing the processor to insert WAIT states. With these features, the iRAM provides SRAM characteristics at lower cost per bit and lower power requirements (within like technologies). The iRAM is a volatile memory, particularly well suited to microcontroller memory (up to 64K bytes) and local memory (up to 128K bytes) for microprocessors.

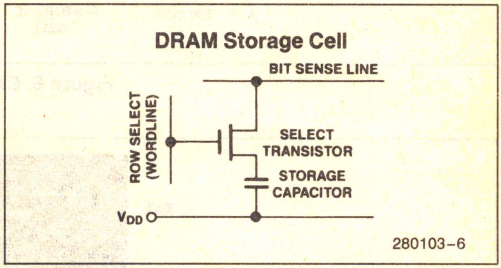


Figure 4. DRAM Storage Cell

2.7 DRAMs

The Dynamic RAM stores data on a capacitor in a single transistor cell. This allows the highest density and lowest power per bit of all random access memories, but, because of charge leakage from the storage capacitor, they have to be refreshed periodically. DRAMs are volatile memory and, as such, lose data whenever power is removed or lost.

The primary DRAM application has been, historically, large main memories (greater than 64K) for mainframe, mini and personal computers. The introduction of CHMOS DRAMs has further reduced the power requirements[4] and added new high bandwidth fea-

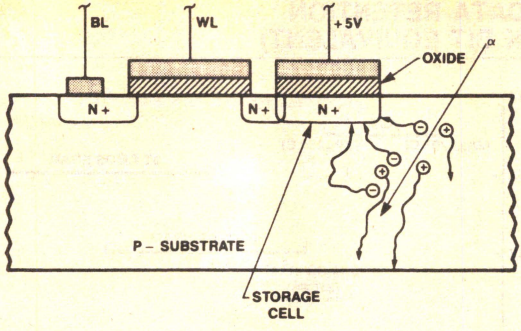


Figure 5. NMOS DRAM Cell

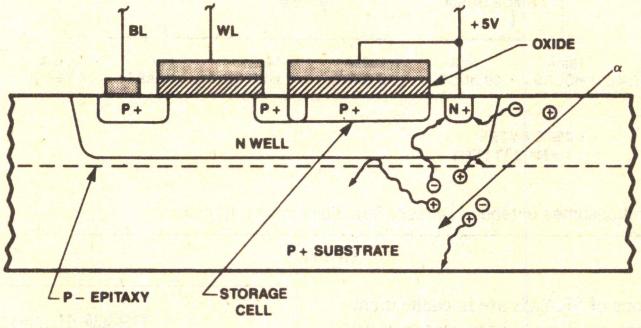
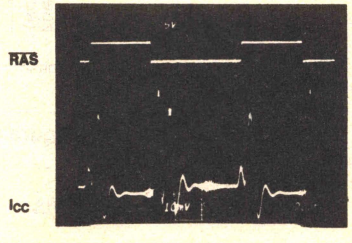


Figure 6. CMOS DRAM Cell



51C259L CURRENT
20 mA/DIVISION
I_{CC} DURING $\overline{RAS}$ LOW TIME BETWEEN
T_{RAC} AND T_{RP} IS 5 mA

Figure 7. 51C259 Current

tures such as Ripplemode™ and Static Column Decode[5]. The features of CHMOS allow DRAMs to move into non-volatile solid state disks (which will permit the user to execute directly from mass storage), battery powered (portable) computers, battery back-up systems and traditionsl SRAM speed applications such as video graphics[6].

DRAMs on the CHMOS process reduce the standby current by about a factor of forty. The data retention power requirement of the DRAM is further reduced by the extended refresh feature. When operating in the data retention mode, refresh can be extended to 32 ms for the 51C256L, 64 ms for the 51C64L.

Because a small capacitor is the storage mechanism for DRAMs, they have been susceptible to "soft errors". When an alpha particle strikes the die, it generates ions which collect at the capacitor, changing the stored charge[7]. The cell is not damaged but the information it contains can be changed (Figure 5). If it is, a "soft" error has occurred. The CMOS process has changed this by allowing the storage capacitor to be placed in an "n" well which absorbs the ions generated by the stray particle[8] (Figure 6). Consequently, 64K CHMOS DRAMs, at a 1μS cycle rate, have soft error rates of 10 fits*. At the 256K level, the soft error rate will be less than 400 fits, and typically 40 fits. Furthermore, since the soft error rate is directly related to cycle rate , during the low power data retention mode (i.e. 32 ms refresh) the soft error rate goes to:

1 μs = 40 fits, then for the 256K devices the extended refresh soft error rate is:

32 ms/256 refresh rows = 125 μs

1 μs/125 μs −40 fits = **0.32 fits** per device

*failures in time = number of failures in $10^{(9)}$ device hours (or 114 years).

3.0 SYSTEM DESIGN USING CHMOS DRAMs

3.1 Active Low Power Design Description

CHMOS DRAMs permit the building of larger and lower powered systems than have previously been possible. As an illustration, a low power, general purpose microcomputer system design will be discussed using all CMOS products. An 80C88 operating in max mode has 256K bytes of DRAM (expandable to 960 Kb) with a DMA controller to handle refresh during normal operation. A standby mode of operation is provided to reduce the power usage during periods of no activity. During standby the memory refresh is extended to 32 ms which reduces the data retention power.

To minimize the transient effects of current, it is recommended that a 0.1 μF bypass capacitor be provided for each memory device. High speed (low inductance) capacitors are preferred. Most CMOS devices require less than 0.1 μF. The actual decoupling capacitance required can be calculated for specific devices using the formula:

$$C_{BYPASS} = di^{*}dt/dV$$

where; di = change in current

dt = spike duration or 1 μs*, whichever is faster

dV = allowable voltage droop

For example, Figure 7 shows the current requirement for the 51C259. The peak current is 95.63mA so the decoupling requirement is:

$$C = 96\ mA \times 40\ ns/100\ mV = 0.04\ \mu F$$

In this case 0.1 μF for every other device would be sufficient.

***NOTE:**
Assume 1 μs respond time of bulk capacitance, typical of tantalum.

3.1.1 SYSTEM DESIGN EXAMPLE

Referring to Figure 8, during normal ooeration the 80C88 controls the bus through the 82C88 bus controller. During interrupt requests the 82C59A interrupt controller takes control of the bus long enough to send a vector address to the microprocessor, and to refresh the DRAM array, the DMA controller requests the bus and then executes a single (distributed) refresh cycle to all four banks of memory. The DRAM $\overline{RAS}$ signals and the EPROM $\overline{CE}$ are decoded by the higher order addresses A16, A17, A18 and A19 in a 4-to-16 line decoder. The decoder divides the address field into 64K blocks, convenient for the particular DRAM components used here. One output of the decoder is used as Chip Enable for the 16K bytes of EPROM shown here at address FC000H to FFFFFH. The EPROM is located here because the system reset vectors the 80C88 to address FFFF0H to access initialization routines. The EPROM can be expanded downward in the address field to 64K bytes beginning at F0000H, or further still by using another of the 4-to-16 line decoder outputs. Four outputs from the decoder are used as $\overline{RAS}$'s each to a bank of DRAM, totalling 256K bytes at addresses 00000 to 3FFFFH. Using the other outputs to provide $\overline{RAS}$ to eleven more banks would increase the total DRAM by 704K, to 960K bytes.

The reset initialization routines are located in EPROM and, for this system, will include programming routines

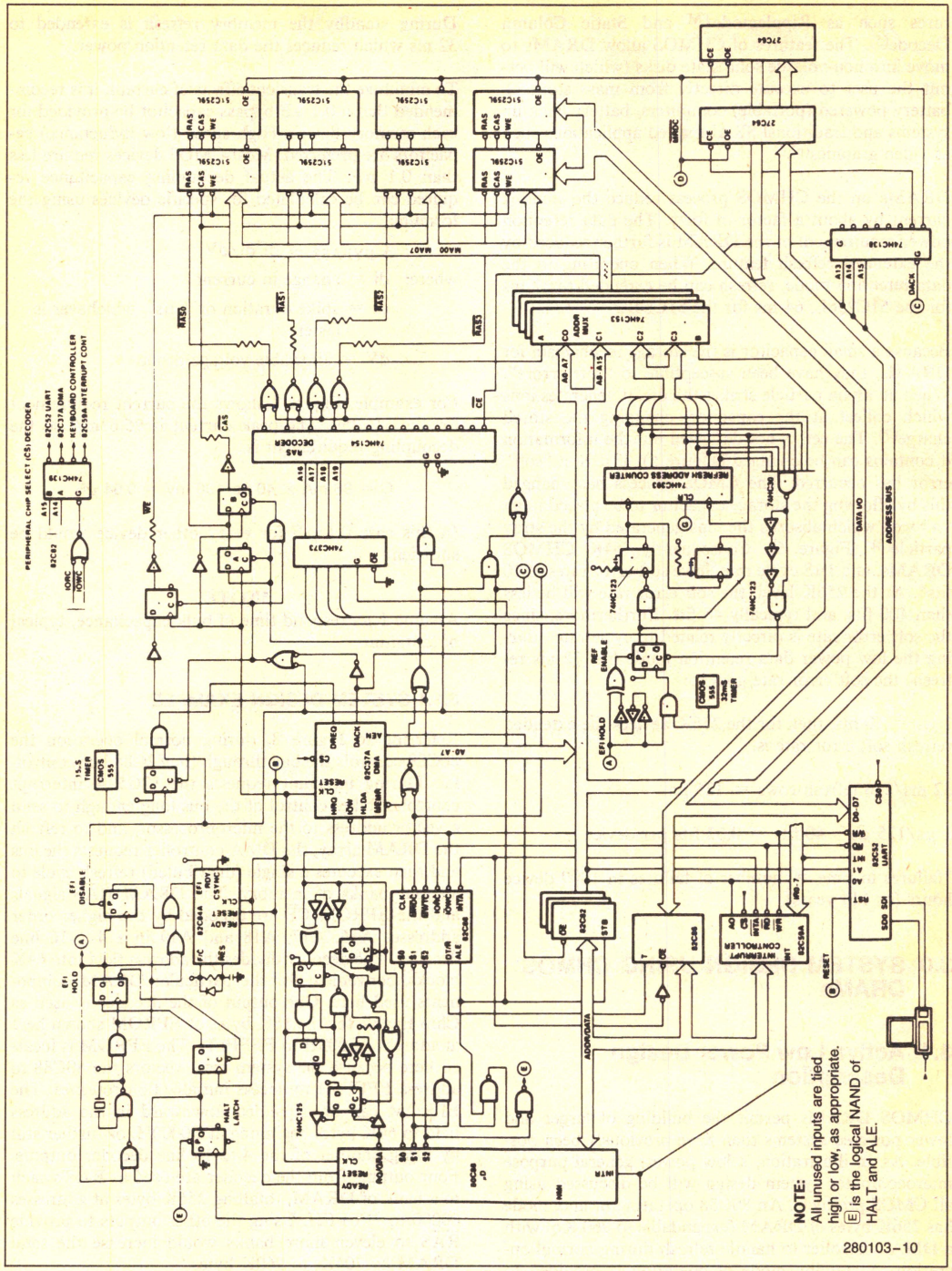


Figure 8. Low Power System Design

for the DMA controller, the interrupt controller and the UART. Following initialization, the DMA will begin its distributed refresh routine and the operating system software can be loaded through one of the I/O ports.

Write enable ($\overline{WE}$) to the DRAM is generated by the memory write command ($\overline{MWTC}$) from the 82C88 bus controller and the system clock. Column address strobe ($\overline{CAS}$) is generated by $\overline{MWTC}$ or $\overline{MRDC}$ (memory read command) and the system clock. The rising edge of the clock sets the latch (A) which switches the address multiplexer from the row address to the column address. The falling edge of the clock then sets the second latch (B) which sends $\overline{CAS}$ to the memory. During the DMA refresh cycles, the acknowledge signal (DACK) holds CAS and $\overline{WE}$ high and clears the DMA request (DRQ). Note that the $\overline{CAS}$ and $\overline{WE}$ latches are buffered to the array. This is done because reflections from the line stubbing of the memory array back into the outputs of the latches could cause the latches to toggle, glitching the signals. Also, series terminators ($\sim 33\Omega$) are shown in the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address lines. These terminators improve the impedance match of the driver to the line, reducing reflections. For best results, they should be located electrically less than one inch from the driver output.

3.1.2 MEMORY

The 51C259L devices used here are low power 256k bit memory devices organized as 64K x 4. This organization helps keep active power low by enabling only two devices during a memory access. If 256K×1 devices were used, all eight would be turned on, drawing about four times the current.

The EPROMs shown are CHMOS 8K x 8's, containing a boot loader and programming instructions for the DMA, the interrupt controller and the UART. The EPROM capacity could be increased to 64K bytes using the rest of the outputs of the 74HC138 decoder.

In max mode, the 80C88 provides two common I/O request/grant ($\overline{RQ}/\overline{GRA}$) lines to co-processors for bus access, one of which is used here for the DMA (Figure 9). This pin requires a low-active pulse in to request the bus, then sends a low-active pulse out to release (grant) the bus. The processor then waits for another low-active pulse in to indicate that the co-processor is through with the bus. The DMA has separate Hold Request (HRQ) and Hold Acknowledge (HLDA) pins which use active-high levels. Consequently, it is necessary to convert both the high-going and low-going edges of HRQ to low-active pulses. In the period between these pulses, the $\overline{RQ}/\overline{GRA}$ pin must be released for the 80C88 output "Grant" pulse. The Grant pulse presets a latch for the DMA Hold Acknowledge and returns the $\overline{RQ}/\overline{GRA}$ pin to the input circuit to wait for the end-of-hold pulse.

3.1.3 STANDBY MODE

One nice feature of the CMOS process is that the system can be put into a very low power standby mode by bringing the system clock to a complete stop. To do this, the external frequency in (EFI) on the 82C84A is used and the EFI clock is stopped, in this case, by a HALT instruction from the 80C88 (Figure 10). The HALT instruction first stops the EFI clock without any glitches and it then stops the oscillator itself, both at a high level. The timing through the 82C84A at this frequency stops the clock output low. Any interrupt (such as a key pressed) will cause the system to exit the standby mode and return to normal operation. The interrupt clears the halt latch which allows the oscillator to begin again. Because the oscillator was stopped at a high level, it will begin by transitioning low. Then, on the high transition, it will clock the EFI hold latch thus clearing it. The following low transition will get through the first stage OR gate. When the burst refresh initiated by clearing the EFI hold latch (see below) is completed, the oscillator will clock the EFI disable latch low and then the oscillator will be enabled through to the EFI input of the 82C84A. The burst

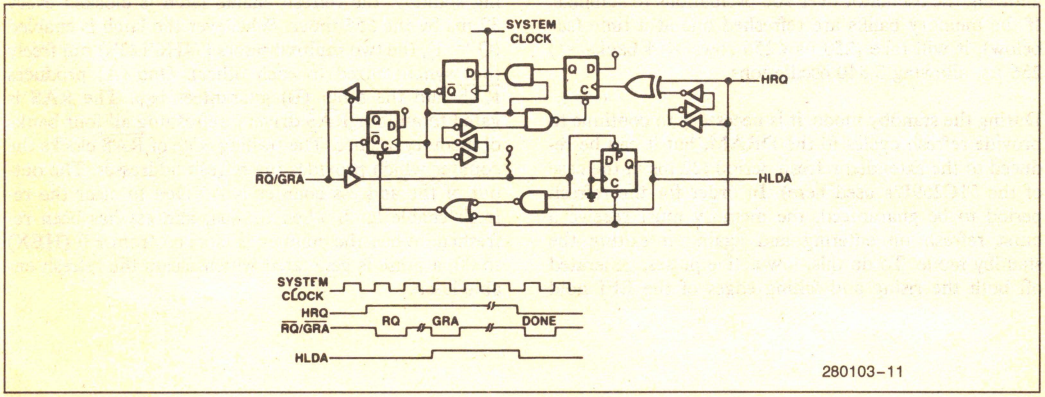


Figure 9. Bus Request Circuit

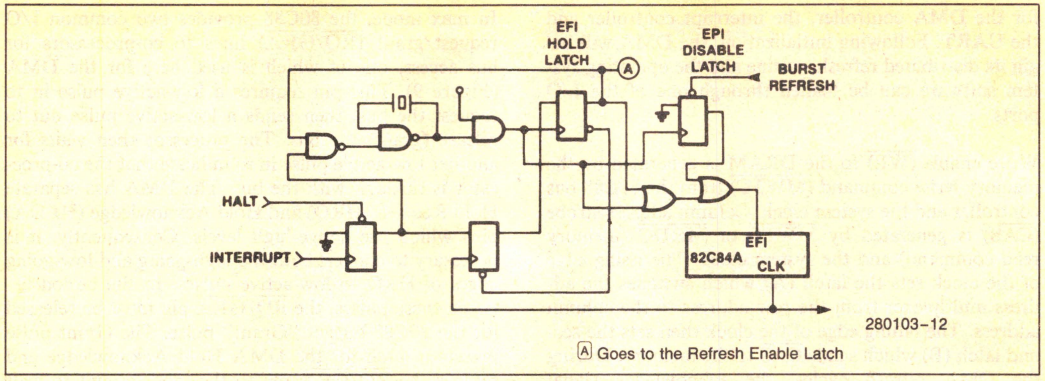


Figure 10. Clock Circuit

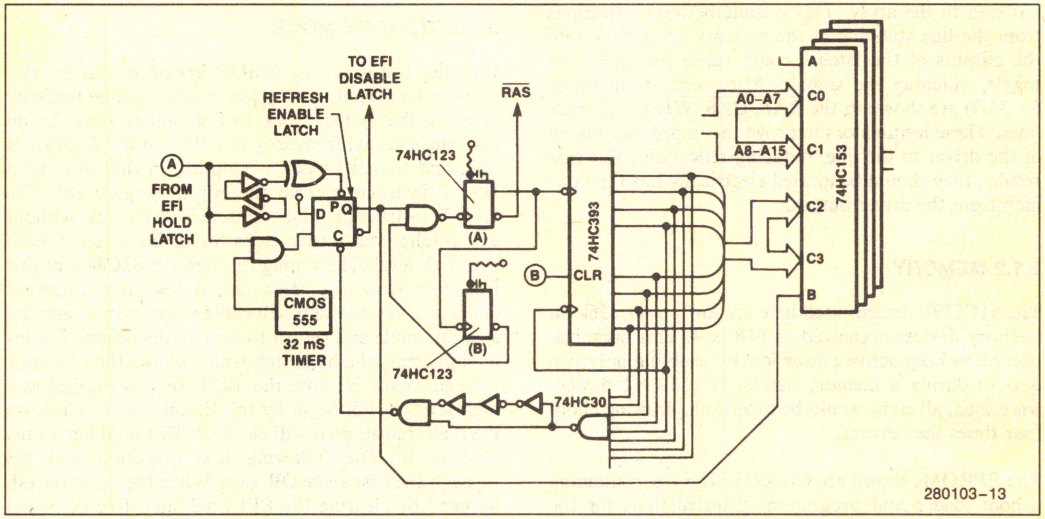


Figure 11. Refresh Circuit

refresh will take about (250 ns × 256 rows =) 64 μs, allowing the oscillator over 900 oscillations to stabilize. If the memory banks are refreshed one at a time (see below), it will take (250 ns×256 rows × 4 banks =) 256 μs, allowing 3,840 oscillations.

During the standby mode, it is necessary to continue to provide refresh cycles to the DRAM, but it can be reduced to the extended refresh period (32 ms in the case of the 51C259L's used here). In order for the refresh period to be guaranteed, the memory must receive a burst refresh on entering and again on exiting the standby mode. To do this, low-active pulses, generated off both the rising and falling edges of the EFI hold latch, preset the refresh enable latch (Figure 11). During standby, the refresh enable latch is clocked every 32 ms by the 555 timer. Whenever the latch is enabled (Q = 1), the two multivibrators (74HC123's) run freely (but synchronized to each other). One (A) produces $\overline{RAS}$ and the other (B) guarantees t_{RP}. The RAS is gated to all four $\overline{RAS}$ drivers, refreshing all four banks of memory at once. The trailing edge of $\overline{RAS}$ clocks the counter which provides the refresh addresses. The output of the address counter is ANDed to clear the refresh enable latch when the last address has been refreshed. When the counter is clocked from FF (HEX) to 00, a pulse is generated which clears the refresh enable latch.

While refreshing all four banks at once, as is shown here, does not use any more average power, refreshing one row at a time would reduce the peak power requirement during standby by a factor of four (see Figure 14 and the Data Retention design for power calculations, later in this section).

When exiting the standby mode, it is necessary to keep the 80C88 and the DMA off the bus until the last burst refresh has been completed. To do this, (Figure 10) the refresh enable latch presets the EFI disable latch in the clock hold circuitry, blocking the oscillator from the EFI input of the 82C84A and holding the system clock off. At the same time, it disables the DREQ input to the DMA and, for additional security, holds $\overline{CAS}$ and $\overline{WE}$ off. When the burst refresh is complete, the oscillator clears the EFI disable latch, releasing the oscillator to the 82C84A.

3.1.4 POWER ANALYSIS

The system shown (Figure 8) contains ten VLSI devices[9], ten memory devices, thirty logic devices and two timers. To calculate the power consumption, some assumptions are made:

— where not given, typical values are 40% of the maximum value (rule of thumb)

— some values are estimates as final data sheets are not yet available.

— typical values are used as they should average out over a system.

— during normal operation, the memory receives a 15 μs distributed refresh

— The 80C88 can access the memory at 5 MHz/4 = 1.25 MHz max.(one bus cycle takes four T-states)

— The DRAM memory is capable of operating at (1/245 ns =) 4.082 MHz.

— System duty cycle is 2% (most of the system time is spent waiting for instructions such as keyboard entries)

— The speed/power curve is approximately linear

74HC logic current requirement (@25°C):
536 μA (logic) + 144 μA (timers) = 0.68 mA

Eight 51C259L-15 DRAMs, 100% (4.082 MHz) duty cycle, I_{CC} (typ):

— operating = 45 mA each

— standby = 0.01 mA each (CMOS drivers)

Two 27C64 CMOS EPROM, I_{CC} (typ):

— operating = 20 mA × 0.4 = 8 mA each

— standby = 100 μA × 0.4 = 0.04 mA each

During constant DRAM memory accesses, memory activity is:

active: 1.25 MHz/4.082 MHz = 30.6%

refresh: 245 ns/15 μs = 1.7%

standby: 100% − (30.6 + 1.7) = 67.7%

Memory Current is:

active: [2(45 mA) + 6(0.01 mA)] 30.6% = 27.56 mA

refresh: [8(45 mA)] 1.7% = 6.12 mA

standby: [8(0.01 mA)] 67.7% = 0.054 mA

continuous memory access total current = 33.73 mA

At 2% system duty cycle, memory current is:

$(I_{oper} \times 2\%) + I_{ref} + [I_{stby} \times (100\% - (2 + 1.7)\%)] =$
(27.56 mA × 2%) + 6.12 mA + [8(0.01 mA)] 96.3% =
6.597 mA

EPROM Current is:

continuous active	16.0 mA
continuous standby	0.08 mA

Table 1 shows the typical current required for the VLSI:

Table 1

Device	Active	Standby
80C88	20.0 mA	0.2 mA
82C84A	6.0 mA	6.0 mA
82C37A	0.4 mA	0.004 mA
82C88	2.0 mA	0.004 mA
82C82 (3 each)	1.5 mA	0.012 mA
82C86	0.5 mA	0.004 mA
82C59A	0.4 mA	0.004 mA
82C52	1.0 mA (est)	0.004 mA
TOTAL	**31.8 mA**	**6.232 mA**

Rounding the DMA duty cycle up to 2% (from 1.7%) for simplicity, the current requirement for the VLSI at a 2% duty cycle is:

(31.8 mA × 2%) + (6.232 mA) × 98%) = 6.743 mA

Therefore, total current for the system during normal operation at the 2% duty cycle (DRAM accesses only) is:

logic + DRAM + EPROM + VLSI
0.68 mA + 6.597 mA + 0.08 mA + 6.743 mA = **14.1 mA**

During a RESET operation, for a period of less than 1 ms, current will be:

DRAM stby + refresh + EPROM + logic +
[8(0.01 mA)]98.3% + 6.12 mA + 16 mA + 0.68 mA +

μP + clk + DMA + bus + addr +
20 mA + 6 mA + 0.0107 mA + 2.0 mA + 1.5 mA

data + int + UART =
+0.5 mA + 0.004 mA + 0.004 mA = **52.9 mA**

Power Supply

Using the formula: $C = di*dt/dV$;

$$(52.9\ mA - 14.1\ mA)1\ ms/200\ mV = 194\ \mu F$$

200 μF of storage capacitance will support V_{CC} during reset to no more than 200 mV of droop. This means the power supply need only be sized for normal operation. Normal operation should not exceed 70% of the power supply capacity (ye olde rule of thumb) so:

$$0.7\ I_{ps} = 14.1\ mA$$
$$I_{ps} = 20.14\ mA$$

a 20 mA supply would suffice and, incidentally, would reduce the maximum droop voltage during reset to:

$$(52.9\ mA - 20\ mA)1\ ms/200\ \mu F = 164.5\ mV$$

3.2 Data Retention Design

A system with data retention can, but need not necessarily be a low power design. The main prerequisite is that that portion of the system to be supported by the battery in the absence of line power must be low power. The elements to be discussed here include:

— saving information in use by the processor

— ensuring refresh for the DRAM

— protecting the memory from false signals:
  a. during back-up
  b. at power up

— minimizing power dissipation during back-up

3.2.1 SAVING INFORMATION

When power fails, the processor will "lose its place", or forget the operations it was actively executing. To prevent this, one can, when the power sense signal occurs, interrupt the processor using the non-maskable interrupt. The NMI would send the processor to a routine causing it to store, in a fixed area of memory, the pointers, stack counter and program counter and then to set a flag. The area of memory used can be anywhere, but it should either be dedicated to this task or it should be a rarely used section such as the bottom of the stack. When power returns, following system initialization, the processor checks the flag and, if set retrieves the saved information and continues from where it was interrupted.

3.2.2 SYSTEM DESIGN EXAMPLE

For the sake of simplicity, we will use the low power design already discussed, modifying it for battery back-up. In Figure 12, power fail circuitry is ORed with the EFI hold signal into the data retention refresh circuitry. A binary counter enabled by 'power sense' counts $\overline{RAS}$ pulses to the memory, allowing, in this case, fifteen memory accesses (including refresh) to store pointers, etc., and set a flag. It then starts the backup refresh circuitry. The maximum time before starting data retention refreshing would occur when all accesses counted are normal refresh cycles:

$$15\ \mu s \times 15\ cycles = 225\ \mu s$$

This period is easily supported by the capacity of the power supply and V_{DD} grid, but it does limit the number of memory accesses and the time in which to do

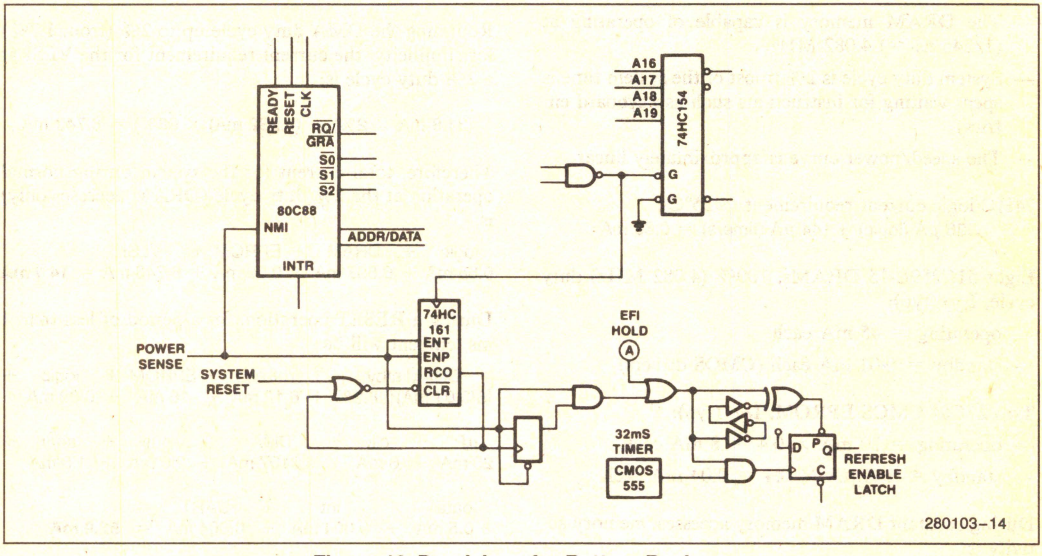


Figure 12. Provisions for Battery Back-up

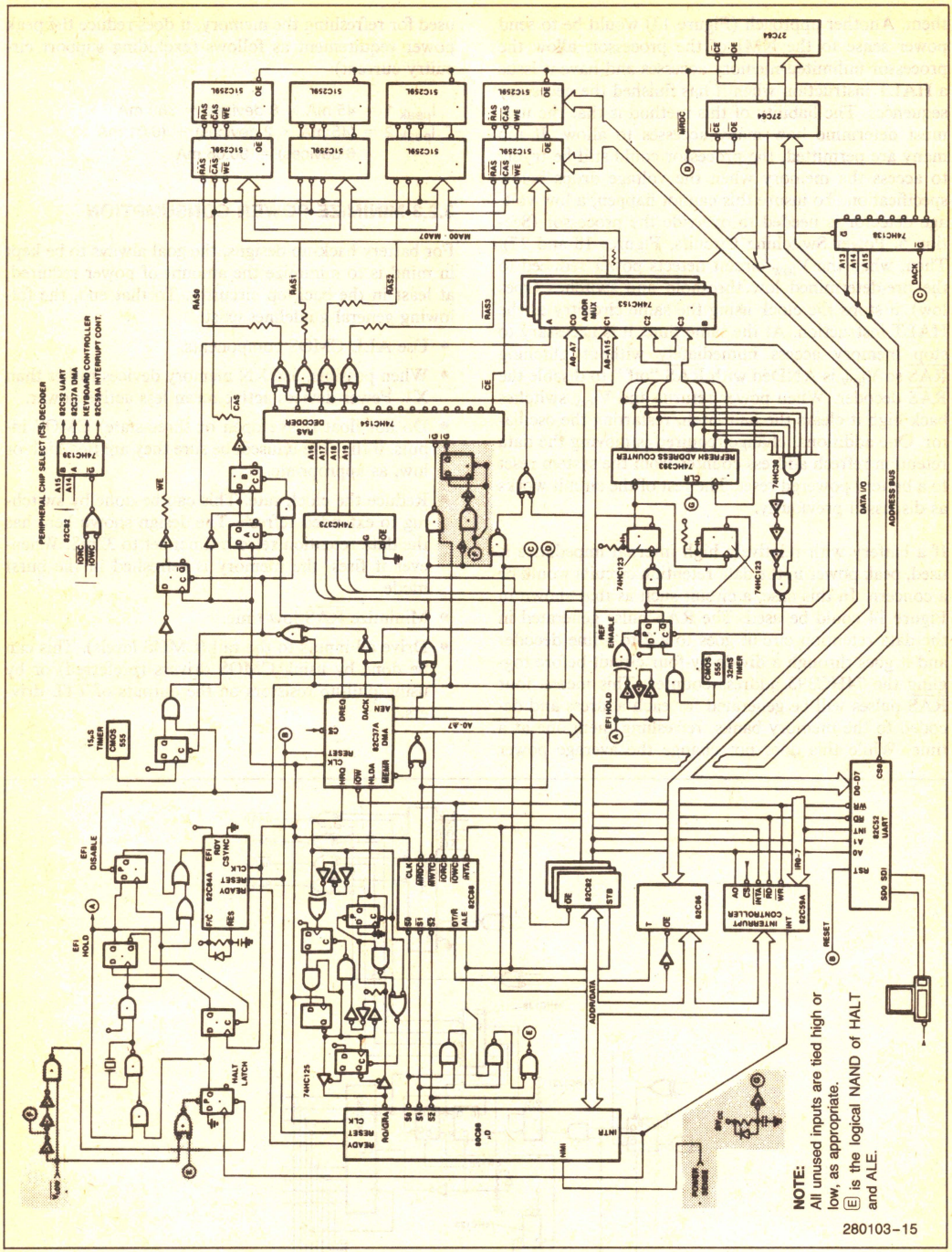


Figure 13. Battery Back-up Design

them. Another approach (Figure 13) would be to send power sense to the NMI of the processor, allow the processor unlimited memory accesses and have it issue a HALT instruction when it has finished the necessary sequences. The liability of this method is that the user must determine how many accesses to allow. If too many are permitted, the processor could still be trying to access the memory when the voltage drops below specification. To insure this cannot happen, a low voltage detector is needed to override the processor (Section 5, Power Switching Circuits, Figures 18 and 27). Then, when the V_{low} circuit detects power reduced to the pre-determined low threshold and switches (goes low), it stops the clock using the same circuitry as the HALT instruction. At the same time, it is necessary to stop memory access immediately without glitching $\overline{RAS}$ so V_{low} is ANDed with $\overline{RAS}$ "off" to disable the $\overline{RAS}$ decoder. When power returns and V_{low} switches back high it clears the halt latch, restarting the oscillator. One additional change required is moving the data retention refresh address counter from the system reset to a battery powered reset. The rest of the circuit works as discussed previously.

If a battery with relatively high internal impedance is used, peak power in the data retention circuits would be a concern. In this case, a circuit such as that shown in Figure 14 could be used. The $\overline{RAS}$ pulse generated in the data retention circuit goes to a 2-to-4 line decoder and it goes through a divide-by-four circuit before toggling the 74HC393 address counter. This means four $\overline{RAS}$ pulses will be generated for each address and decoded to the memory banks, refreshing them one at a time. While this does not change the average power used for refreshing the memory, it does reduce the peak power requirement as follows (excluding support circuitry current):

$I_{peak}\ 1 = 45\ mA \times 8\ devices = 360\ mA$

$I_{peak}\ 2 = (45\ mA \times 2\ devices) + (0.01\ mA \times 6\ devices) = 90.06\ mA$

3.2.3 MINIMIZE POWER CONSUMPTION

For battery back-up designs, the goal always to be kept in mind is to minimize the amount of power required, at least in the back-up circuitry. To that end, the following general guidelines exist:

- Use ALL CMOS components.
- When possible, use XN memory devices rather than X1. Fewer devices active mean less active power.
- Do not float (leave open or three-state) CMOS inputs. if they are unused, be sure they are tied high or low, as appropriate.
- Reduce the clock rate. This can be done by switching to extended refresh. The design shown here has the data retention refresh timer set to 32mS. Whenever it fires, the memory is refreshed in the burst mode.
- Minimize $\overline{RAS}$ low time.
- Drive all inputs to the rail (CMOS levels). This can be done by using CMOS drivers (preferred) or by using pull-up resistors on the outputs of TTL drivers.

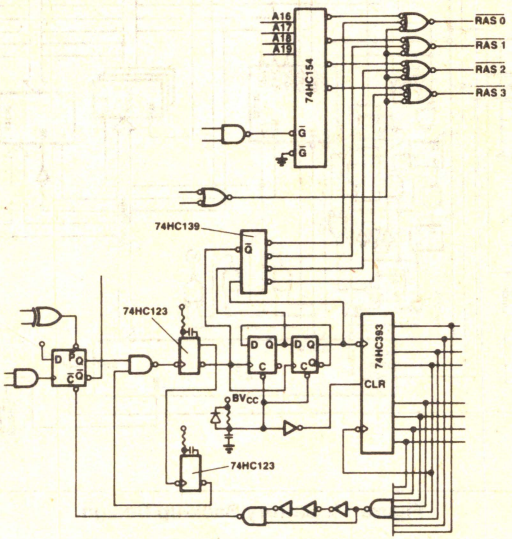


Figure 14. Distributed Refresh Reduces Peak Current

- Minimize the number of pull-up resistors by using CMOS drivers wherever possible.
- Ensure bypass capacitors have low inductance paths across the device (Figure 15).
- Use good design practices. Reduce the load capacitances by keeping related sections physically close.

Control input transitions. When too slow ($\geq$25 ns), excess current will flow. When too fast (<5 ns), the increased frequency increases the current requirement. When possible, distribute the power used over time to control peak currents. Figure 14 alternates the refresh to each bank of memory, reducing the peak power requirement.

(For more design guidelines, see #10 in the bibliography)

3.2.4 POWER ANALYSIS

For this example, the power requirements of just the battery back-up section will be analyzed. As shown in Figure 13, those elements identified by an asterisk (*) would be powered by the battery in data retention mode. To determine battery size, typical values may be used, but the application, particularly the ambient temperature should also be considered. The lesser values will be used here.

The current requirements are:

Memory (/dev.):	Logic (total,TYP.)
typical operating = 45 mA	464 μA
maximum operating = 65 mA	
typical standby = 0.01 mA	
maximum standby = 0.1 mA	

When supported by the battery, the memory is refreshed every 32 ms. Refresh cycle time is 250 ns and each device has 256 rows to be refreshed (the cycle time can be extended a little to provide margin for component tolerances but extend t_{RP} because as $\overline{RAS}$ low time is extended, power increases). Total current required will be determined by the amount of time spent in each of refresh and standby.

256 rows × 250 ns = 64 μs to refresh
64 μs/32 ms × 100 = 0.2%
8(45 mA) × 0.002 = 720 μA (active)
8(0.01 mA) × 0.998 = 79.84 μA (standby)
720 μA + 79.84 μA = 799.8 μA (averaged over refresh period)

Therefore, the total average current drawn by the battery back-up section of this design, at 25°C, is:

799.8 μA + 464 μA = 1.264 mA

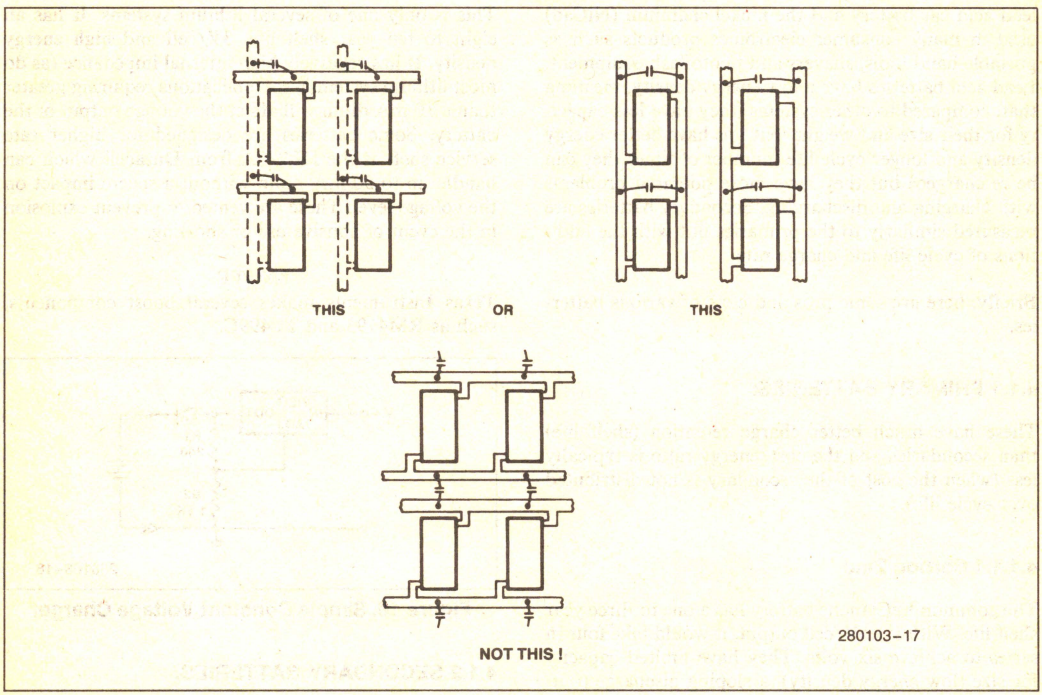


Figure 15. Effective Capacitive Decoupling

With this information, a reasonable choice of battery type can be made (see Section 4, Batteries).

4.0 BATTERIES

4.1 Battery Types

Batteries are divided into two basic types, primary and secondary. Primary batteries cannot, reasonably, be recharged. Secondary batteries are those that can be recharged. (For a comprehensive reference on batteries, see #12 in the bibliography.)

Primary batteries are created around a chemical reaction that, for all practical purposes, cannot be reversed. Consequently, when their charge is depleted they must be replaced. Some common examples are the zinc chloride, silver oxide and lithium batteries. They come in various sizes and most are in one of two styles, cylindrical or coin shaped. There are many electrochemical systems under the primary heading, each varying from the others in some unit of measure such as voltage, energy, energy density or cost. These variations can make them more or less suited for various applications (see chart 2)[11].

Secondary batteries use a reversible chemical reaction. Some common examples of secondary batteries are the lead acid car battery and the nickel-cadmium (NiCad) used in many consumer electronics products such as portable hand tools, shavers and photoflash equipment. Lead acid batteries have a low energy density, meaning that, compared to other systems, they have less capacity for their size and weight. NiCads have better energy density and longer cycle life (number of times they can be re-charged) but they have more potential problems with charging and discharging. Secondary batteries are measured similarly to the primaries but with the additions of cycle life and charge rate.

Briefly, here are some pros and cons of various batteries.

4.1.1 PRIMARY BATTERIES:

These have much better charge retention (shelf life) than secondaries and the cost/energy ratio is typically less (when the cost of the secondary is not distributed over cycle life).

4.1.1.1 Carbon Zinc

The common LeClanche battery has a one to three year shelf life. With a 1.5V/cell output, it would take four in series to achieve six volts. They have limited capacity for size (low energy density), a sloping discharge (output voltage decreases continuously over the period of the discharge), low cost and excellent availability in a wide variety of package sizes and capacities.

4.1.1.2 Alkaline Manganese

Similar to the carbon zinc, the alkaline battery has a two to five year shelf life, 1.5V/cell, limited capacity for size and a sloping discharge. It has higher energy density but higher cost than LeClanche and it is widely available in a variety of sizes and capacities.

4.1.1.3 Silver Oxide

This battery has a two to five year shelf life. It has a high energy density but, with 1.5V/cell, it would require four in series of a boost circuit* to achieve six volts. It has a flat discharge curve, relatively high cost and limited package configurations.

4.1.1.4 Mercuric Oxide

Similar to the silver oxide, the mercuric oxide battery has only 1.35V/cell. It has a flat discharge curve, higher cost and a potential ecological problem with the disposal of spent cells.

4.1.1.5 Lithium Manganese

This is only one of several lithium systems. It has an eight to ten year shelf life, 3V/cell and high energy density. It has relatively high internal impedance (as do most lithium systems), so applications requiring greater than a 10 mA drain will affect the voltage output of the battery. Some batteries are designed for higher rate service such as the DL2/3A from Duracell which can handle up to 50 mA drain without a severe impact on the voltage level. These are vented to prevent explosion in the event of abusive use or shorting.

*NOTE:
Texas Instruments makes several boost components, such as RM4193 and TL499C.

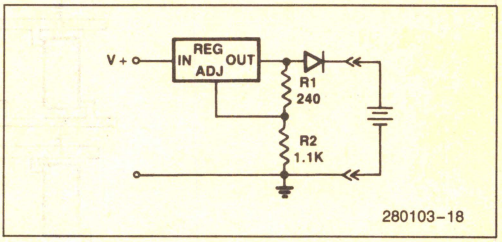


Figure 16. Simple Constant Voltage Charger

4.1.2 SECONDARY BATTERIES:

Because of self-discharge, these batteries have a relatively short shelf life but, with some means of charge

Chart 2. Eight Principal Battery Systems and Average Characteristics

Usual Name*	Carbon Zinc*	Zinc Chloride Super Heavy Duty*	Alkaline-Manganese Dioxide (MnO_2)	Mercuric Oxide*
Electrochemical System	Zinc-Manganese Dioxide (often called Leclanche)	Zinc-Manganese Dioxide	Zinc-Alkaline Manganese Dioxide	Zinc-Mercuric Oxide
Voltage Per Cell	1.5	1.5	1.5	1.35
Negative Electrode	Zinc	Zinc	Zinc	Zinc
Positive Electrode	Manganese Dioxide	Manganese Dioxide	Manganese Dioxide	Mercuric Oxide
Electrolyte	Aqueous solution of ammonium chloride and zinc chloride	Aqueous solution of zinc chloride (may contain some ammonium chloride)	Aqueous solution of potassium hydroxide	Aqueous solution of potassium hydroxide or sodium hydroxide
Type	Primary	Primary	Primary	Primary
Rechargeability	Not Recommended	Not Recommended	Not Recommended	Not Recommended
Number of Cycles				
Input if Rechargeable				
Overall Equations of Reaction	$2MnO_2 + NH_4Cl + Zn \rightarrow ZnCl_2 + 2NH_3 + H_2O + Mn_2O_3$	$8MnO_2 + 4Zn + ZnCl_2 + 9H_2O \rightarrow 8MnOOH + ZnCl_2 \cdot 4ZnO \cdot 5H_2O$	$2Zn + 2KOH + 3MnO_2 \rightarrow 2ZnO + 2KOH + Mn_3O_4$	$Zn + HgO + KOH \rightarrow ZnO + Hg + KOH$
Typical Commercial Service Capacities	60 mAh to 30 Ah	Several hundred mAh to 18 Ah	30 mAh to 45 Ah	45 mAh to 14 Ah
Energy Density (Commercial) Watt-hour/Lb	20	40	20–45	50
Energy Density (Commercial) Watt-hour/Cubic Inch	2	3	2–5	8
Practical Current Drain Rates Pulse	Yes	Yes	Yes	Yes
Practical Current Drain Rates High (More Than 50 mA)	100 mA/square inch of zinc area ("D" cell)	150 mA/square inch of zinc area ("D" cell)	200 mA/square inch of separator area ("D" cell)	No
Practical Current Drain Rates Low (Less Than 50 mA)	Yes	Yes	Yes	Yes
Discharge Curve (Shape)	Sloping	Sloping	Sloping	Flat
Temperature Range: Storage	−40°F to 120°F (−40°C to 48.9°C)	−40°F to 120°F (−40°C to 48.9°C)	−40°F to 120°F (−40°C to 48.9°C)	−40°F to 140°F (−40°C to 60°C)
Temperature Range: Operating	20°F to 130°F (−6°C to 54.4°C)	0°F to 130°F (−17.8°C to 54.4°C	−20°F to 130°F (−28.9°C to 54.4°C)	14°F to 130°F (−10°C to 54.4°C)
Effect of Temperature on Service Capacity	Poor low temperature	Good low temperature relative to carbon-zinc	Good low temperature	Good high temperature, low temperature depends upon construction
Impedance	Mode	Low	Very low	Low
Leakage	Low???Under Abusive conditions	Low	Rare	Some salting
Gassing	Medium	Higher than carbon-zinc	Low	Very low
Reliability (Lack of Duds: 95% Confidence Level)	99% at 2 years	99% at 2 years	99% at 2 years	99% at 2 years
Shock resistance	Fair to Good	Good	Good	Good
Cost Initial	Low	Low to Medium	Medium Plus	High
Cost Operating	Low	Low to Medium	Medium to high at high power requirements	High

***NOTE:**
Portions of this chart reprinted here courtesy of Union Carbide Corp. Eveready.

Chart 2. Eight Principal Battery Systems and Average Characteristics (Continued)

Usual Name*	Silver Oxide*	Nickel-Cadmium*	Lithium	Lead Acid
Electrochemical System	Zinc-Silver Oxide	Nickel-Cadmium	Lithium-Manganese Dioxide	Lead
Voltage Per Cell	1.5 (monovalent)	1.2	3	2
Negative Electrode	Zinc	Cadmium	Lithium	Lead
Positive Electrode	Monovalent Silver Oxide	Nickelic Hydroxide	Manganese Dioxide	Lead Dioxide
Electrolyte	Aqueous solution of potassium hydroxide or sodium hydroxide	Aqueous solution of potassium hydroxide	Non-aqueous mix propylene carbonate dimethoxy ethane	Sulfuric Acid
Type	Primary	Secondary	Primary	Secondary
Rechargeability	Not Recommended	Yes	Not Recommended	Yes
Number of Cycles		300 to 1,000		
Input if Rechargeable		Minimum of 140% of energy withdrawn		160% of energy withdrawn
Overall Equations of Reaction	$Zn + Ag_2O + KOH \rightarrow ZnO + 2Ag + KOH$	$Cd + 2NiOOH + KOH + 2H_2O \rightleftarrows Cd(OH)_2 + 2Ni(OH)_2 + KOH$	$2Li + 2MnO_2 \rightarrow Li_2O + Mn_2O_3$	$PbO_2 + Pb + 2H_2SO_4 \rightleftarrows 2PbSO_4 + 2H_2O$
Typical Commercial Service Capacities	15 mAh to 210 mAh	150 mAh to 4 Ah	35 mAh to 1100 mAh	1.5 Ah to 400 Ah
Energy Density (Commercial) Watt-hour/Lb	50	12–16	100	10–100
Energy Density (Commercial) Watt-hour/Cubic Inch	8	1.2–1.5	6.6	0.8–7
Practical Current Drain Rates Pulse	Yes	Yes	Yes	Yes
Practical Current Drain Rates High (More Than 50 mA)	No	8.10A ≈ 1 amp/sq. in. of electrode	Cylindrical yes coin no	Yes
Practical Current Drain Rates Low (Less Than 50 mA)	Yes	Yes	Yes	Yes
Discharge Curve (Shape)	FLat	Flat	Flat	Sloping
Temperature Range: Storage	−40°F to 140°F (−40°C to 60°C)	−40°F to 140°F (−40°C to 60°C)	−60°C to +75°C	−60°C to 30°C
Temperature Range: Operating	14°F to 130°F (−10°C to 54.4°C)	Discharge: −4°F to 113°F (−20° to 45°C) Charge CH Types: 32°F to 113 °F (0°C to 45°C) Charge CF Type: 60°F to 113°F (15.6°C to 45°C)	−10°C to +70°C	−40°C to 60°C
Effect of Temperature on Service Capacity	Low temperature depends upon construction	Very good at low temperature	Good high temperature Low temperature depends upon construction	Low temperature depends upon construction
Impedance	Low	Very low	Medium	Low
Leakage	Some salting	No	Rare	Low to Medium. Some salting
Gassing	Very low	Low	Low	Medium
Reliability (Lack of Duds: 95% Confidence Level)	99% at 2 years	99% at 2 years		
Shock resistance	Good	Good	Good	Fair to Good
Cost Initial	High	High	High	Medium
Cost Operating	High	Low	High	Very Low

***NOTE:**
Portions of this chart reprinted here courtesy of Union Carbide Corp. Eveready.

maintenance, shelf life can be extended virtually indefinitely. For the most part, they have a better high rate performance than the primaries, an exception being lithium cells using soluble cathode materials which have comparable performance (i.e. lithium/sulfur dioxide, lithium/thionyl chloride). They can generate gasses when charging or discharging at excessively high rates. For brevity, and because they are generally the preferred design for this application, only the sealed versions will be considered here.

4.1.2.1 Lead Acid

With low energy density, these batteries are generally packaged three or six cells in series for six or twelve volts and in larger sizes for much higher capacities (i.e. 400 Amp hours). Fully charged, they contain strong sulfuric acid and shorting the outputs may cause an explosion. They self-discharge, forming lead sulfate ($PbSO_4$) crystals which can insulate the plate, reducing capacity. Lead filaments can form between the plates when charging and can short out cells. Excessive overcharging may cause venting. They can deliver large current surges and they have a sloping discharge curve which eases the task of sensing when the battery is low. They are normally charged with a constant voltage but can be charged with constant current if care is taken to avoid overcharging. They cannot be stored in a discharged state. They have a lower cycle life than NiCads but they cost less and they have no "memory" effect or thermal runaway problems. Charging circuits are discussed in more detail in the next section.

4.1.2.2 Nickel Cadmium

These batteries have low energy density and 1.2V/cell. If used in series, they should have closely matched discharge rates or the faster discharged cell can be driven to cell reversal (destroyed) when the battery is allowed to reach total discharge. NiCads are charged with constant current at a rate of 10% of capacity (0.1C) for 14 to 16 hours (standard cell) or 30% (0.3C) in 3 to 5 hours for quick charge cells. If constant voltage is used, care must be taken to limit the charge current during the final 25% of charging to prevent thermal runaway. If charged at less than a 10% rate, cell capacity will fade and a sustained overcharge will cause a lack of capacity on the first discharge. When partially discharged to the same level several times and then recharged, they develop a "memory" effect and will, thereafter, discharge no further than that level. It is a temporary effect in that forcing a deep discharge will erase the memory. They cost more than lead-acid but are more rugged, typically have a longer cycle life and they have a long shelf life in any state of charge. Normal discharge rate is fairly flat. Charging circuits are discussed in more detail in the next section.

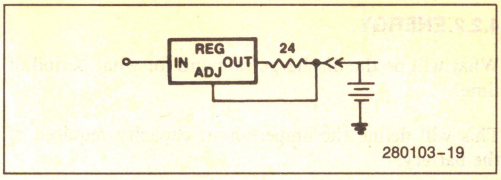


Figure 17. Simple Constant Current Charger

4.1.3 OTHER BATTERY SYSTEMS

This is by no means an exhaustive description of battery systems. Many other primaries and some additional secondaries are available and more are in development. For example, there are a number of primary lithium systems such as lithium/thionyl chloride, lithium/copper oxide, lithium/silver chromate, and so on. A silver oxide secondary is available with the highest energy and power density and best charge retention of any commercially available secondary. Its high cost and low cycle life, however, have held it to limited applications. Many more secondaries are in development, including lithium, nickel, zinc, aluminum, sodium and calcium systems[12]. The concern of this document, however, was for those systems available today and was further narrowed for this application by energy density, availability, voltage/cell, cost, and so on. The LeClanche was included in this description primarily as a commonly known system for reference.

4.2 Key Parameters For Battery Selection

In the process of selecting a particular battery, first consider the application in which it will be used. That will usually encompass many of the characteristics that will identify the battery of choice. For example, in what environment (temperature, vibration, etc.) will the battery exist? What voltage is required. And so on. If necessary, applications engineers from the battery manufacturers can help in the selection process, but here are the main parameters to be considered, in no particular order. The application will generally prioritize them.

4.2.1 VOLTAGE:

What is the voltage range within which the application will be operating?

How low a voltage can be tolerated?

This will show either that a sloping discharge curve is acceptable or it may indicate a requirement for a battery with a flat discharge curve.

4.2.2 ENERGY:

What will be the discharge rate and for what period of time?

This will define the ampere-hour capacity required of the battery.

4.2.3 ENERGY DENSITY:

How much space will be available (or perhaps weight tolerable) in the area where the battery is to be located?

It may be possible to use multiple cells in series to achieve, say, six volts, but more than two cells may be two cumbersome. It is worth noting here that re-chargeable batteries require less service than primaries which have to be replaced periodically. So, particularly in stationary systems, they could be located with the system power supply, permitting larger sizes for greater capacity.

4.2.4 ENVIRONMENT:

What are the temperatures, standby and operating, to which the battery will be subjected?

Will it have to withstand vibration?

This will define how rugged the battery must be.

4.2.5 SERVICE LIFE:

How long must the batteries last, of at least, what is an acceptable period?

This will help define the capacity required of the battery. In the case of the re-chargeables, it can also define the cycle life of the battery.

4.2.6 COST:

Of course! What is acceptable?

Higher cost for a flat discharge rate or, perhaps, for higher service?

Higher initial but lower operating (or the reverse) cost?

Depending on the priority of this issue, it may be the deciding factor between a preferred battery and one that is merely acceptable.

Other factors that may be considered include shelf life, duty cycle, safety, reliability and availability.

4.3 Choosing a Battery

Of course, the issues being considered here are low power systems and systems with battery backup. A hypothetical example of each is examined to illustrate the battery selection process.

4.3.1 EXAMPLES

The first application is a low power system. It is portable, so it must be kept both small and light. The voltage will be in the range of six volts to four-and-a-half volts, using not more than two batteries in series that together do not exceed one half inch in height. Peak current drain is 8mA and duty cycle is 1%. A sloping discharge curve will give an early "battery low" indication which will permit continued operation for a reasonable period to allow time for purchase of a replacement. So size, voltage and discharge curve are the first considerations. Within those parameters we will look for greatest capacity and lowest cost. Referring back to the chart of battery comparisons (Chart 2), the carbon zinc and alkaline manganese have limited capacity for size (energy density) and silver oxide and mercuric oxide would require four cells or a boost circuit. The lithium/manganese dioxide has relatively high energy density, sufficient voltage to achieve six volts with just two cells and an acceptable discharge curve. Both initial and operating costs are high but expense is not a high priority (in this example). Current drain is low enough that the internal impedance of the battery should not be a problem. In the re-chargeables, lead-acid has a low energy density (too big and too heavy). The NiCad has slightly better energy density, it will require four cells and a charging circuit, but has low operating cost. Therefore, it will increase the size of the system (small size was a high priority) but keep operating costs down (cost was a low priority).

The battery of choice for this system is the lithium.

The second application is battery backup. A small computer, stationary, has a four megabyte CHMOS DRAM memory (sixty-four 51C259L's) organized as 2M × 16 and serving as both main memory and as mass storage. Using the 64K × 4 51C2259L means that only four devices will be active at a time, keeping both operating and (if banks are refreshed one at a time) refresh currents low. Since the system is not portable and the battery is for backup, it can be located with the primary power supply so size is not as restricted as in the previous example. This will permit a larger, higher capacity battery to be used for the relatively large memory, but it will probably be less accessible. This implies a battery that rarely needs servicing. Since the system normally draws power from the AC line, a recharging circuit can be added to the system quite easily. Therefore, a rechargeable battery will be used, but which one? Size was not an issue so cost can be. Nickel cadmium batteries are more expensive than lead acid and require more care in charging and discharging. So the battery of choice for this system is the lead acid.

Table 2

System	# = 6V	Capacity	Size (inches)	Typical Life Cycle @ 14mA
Alkaline	4 each	1600 mAh	1.97×2.25×0.56	114.3 hours
Silver Oxide	1 each	150 nAh	0.99×0.51×0.51	10.7 hours
Mercuric Oxide	1 each	500 mAh	1.77×0.68×0.68	35.7 hours
Lithium Mang.	1 each	1200 mAh	1.41×1.37×0.76	85.7 hours
Lead Acid	1 each	6000 mAh	3.6×4.5×1.9	428.6 hours
NiCad (quick chg)	5 each	1200 mAh	1.7×4.5×0.9	85.7 hours

4.3.2 BATTERY SELECTION FOR THE LOW POWER SYSTEM

The low power system discussed in Section 3 could be powered by a secondary battery instead of the power supply. It would have to support about 14 mA during normal operation and a random pulsed high rate of 53 mA (I_{reset}). As discussed in Section 3, storage capacitance could help during the high rate, but a battery with some high rate capacity could reduce the size of the capacitance required. What remains is to determine an acceptable tradeoff between life cycle, size and cost. Beginning with primaries, Table 2 has a few randomly selected examples of battery systems to further illustrate the concept.

Either the NiCad or the lead acid would work well in this particular design. The final choice would depend on other requirements of the application such as cycle life (NiCad) or cost (lead acid).

4.3.3 BATTERY SELECTION FOR BATTERY BACK-UP SYSTEM

The battery back-up system discussed in Section 3 required 1.26 mA average drain at 6 Vdc. Most line power failures are very short, so assuming AC powers the memory at all times except failures and the longest failure might be four hours, the minimum battery capacity is:

$$1.26\ mA \times 4 = 5.04\ mAh$$

Referring to Chart 2, it can be seen that any of the battery types can easily support this requirement. Primary batteries in this system will require a battery low indicator (see Section 5, Power Switching Circuits) and regular servicing. Since AC line power is normally used, this is an excellent application for secondary batteries with a recharging circuit. As above, if the system is to be mobile, smaller NiCads might be used. If stationary or if cost is a significant factor, less expensive lead-acid might be preferred.

If the system is used eight hours a day, five days a week and the batteries are required to support the memory whenever normal power is off, the minimum capacity would have to support the weekend, so:

$$1.26\ mA \times 63\ hours = 79.4\ mAh$$

With the addition of off-hours during the week:

$$1.26\ mA \times 64\ hours = 80.6\ mAh$$

$$\text{Total: } 79.4 + 80.6 = 160\ mAh\ per\ week$$

Referring above to Table 2, the highest capacity primary would last:

$$1600\ mAh / 160\ mAh\ per\ week = 10\ weeks.$$

The secondaries would last to the extent of their cycle life, typically from one to four years at five cycles per week.

5.0 POWER SWITCHING CIRCUITS

A battery back-up system required some means to smoothly enter and exit the battery back-up mode of operation. It must, in an orderly fashion, stop the system and switch the volatile memory over to battery power before the line power is lost. It must also return the memory to line power when that power is restored and it must do it without loss of the data stored and with an orderly transfer of the bus back to the now-active system. In addition, it may be necessary to sense when the battery is in a low state of charge and flag the operator. Where appropriate, it must provide battery charging circuits.

Briefly, these are the elements to be covered in this section:

a. Power sensing
b. Switching to back-up power
c. Sensing battery low
d. Recharging

5.1 Power Sensing

The power sensing circuit is connected to the front-end of the power supply. Essentially, it must provide a look-ahead signal to tell the system that the line power is going down. The system can then invoke a predetermined series of operations that take it to back-up power quickly and in an orderly manner. The sensing circuit is powered at all times by the battery.

5.1.1 μWATTS CMOS LOW POWER DETECTOR

The first circuit shown here is a microwatt CMOS low power detector. It provides two outputs. The first tells the system that power is going down early enough that the system has time to store pointers, stack counter and program counter and shift over to battery power. The second output tells the system to stop all activities, power is gone.

5.1.2 DIFFERENTIAL COMPARATOR FOR POWER FAIL DETECTION

The second circuit uses a comparator that relies on the ripple out of the bridge rectifier. When power starts to go down, the ripple becomes more pronounced. As it fluctuates below the trigger level of the circuit, the comparator output goes high, signalling the beginning of a power loss. As the ripple swings high again (momentarily shutting the comparator off), it provides a little more boost to the regulator, keeping power up a little longer. Because of the relatively low frequency of the ripple (60 × 2 = 120 cps), this provides at least (1/120 =) 8 ms of continued power. Time for the system to shut itself down in orderly sequence.

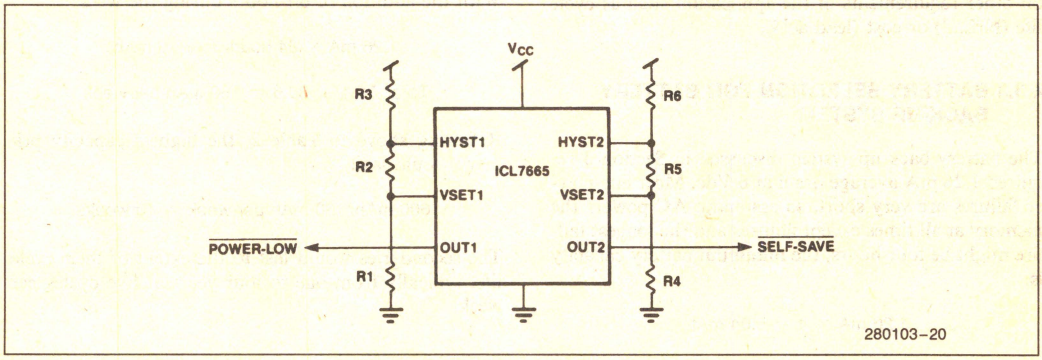


Figure 18. μWatt CMOS Low Power Detector

5.2 Power Switching Circuits

5.2.1 SIMPLE SWITCHING CIRCUIT

The first requirement of a power switching circuit is that the power for the portion of the system what will be supported by the battery when power fails (CMOS) be isolated from the power for the rest of the system (TTL).

This can be done quite simply with a low-leakage diode as shown in the simple diode switching circuit, below. A second diode is installed in the TTL line to keep the normal voltage to both circuits at the same level. V_{CC} must be higher to allow for the diode drop. The lithium battery shown also has a diode to prevent charging of the primary cell. The NiCad has a resistor both to allow charging and to limit the charge current. Battery power to the system will be lower by the voltage drop across the resistor. Relays could be used, but a capacitor would have to support the CMOS circuits during switching and is not recommended.

5.2.2 DUAL VOLTAGE SWITCH

The second switching circuit shown uses transistor isolation. This is a dual voltage circuit, providing normal voltage when the system is operating, and a lower, support voltage on battery power. The voltage drop across the transistor Q2 is small enough (100 to 200mV) that it is unnecessary to match the TTL and CMOS V_{CC} as was done in the diode circuit. During normal operation, Q1 is turned on and the power supply powers the circuit. At the same time, the battery is charged by the base current of Q1. When power goes down, Q2 turns on, Q1 turns off and the battery powers the circuit.

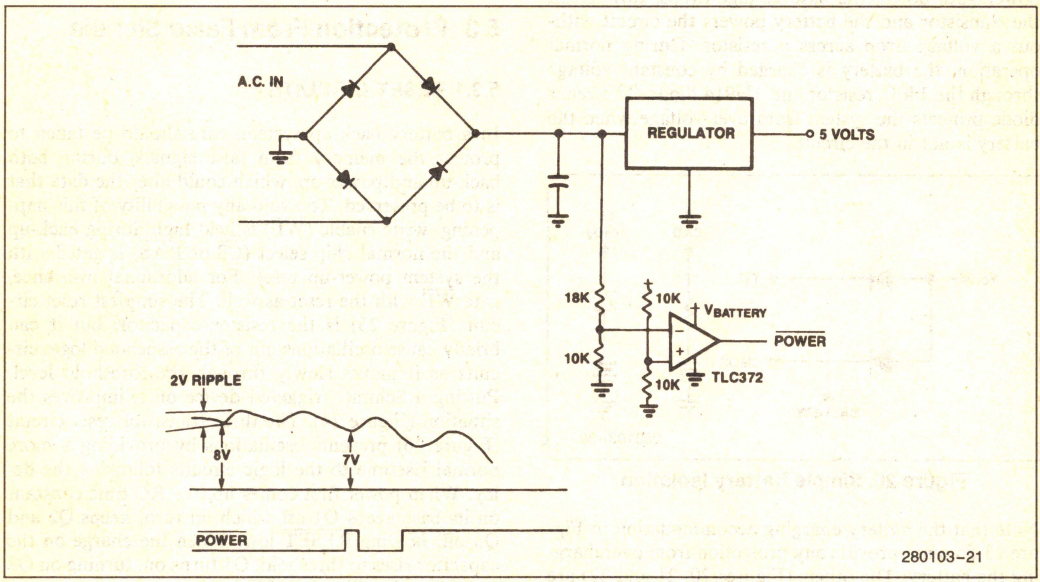


Figure 19. Power Failure Detection

5.2.3 SINGLE-BUS SWITCH

The next switching circuit is a single voltage transistor circuit for a system that has all circuits backed up by the battery. Q2 and its bias network are a regulating circuit that establishes the voltage at which the circuit switches from normal to battery power. As power goes down, that voltage turns off Q2 which, in turn, shuts off Q1 and the battery takes over. The battery is charged by constant voltage, and R_c in the NiCad circuit establishes the maximum charging current for the battery.

5.2.4 DUAL-BUS SWITCH

The last switching circuit uses diode isolation for the two circuits and a transistor switch for the battery. Normally biased off by the unregulated voltage, as power goes down, the base voltage drops, turning on the transistor and the battery powers the circuit without a voltage drop across a resistor. During normal operation, the battery is charged by constant voltage through the 140Ω resistor and 1N914 diode. The zener diode protects the system from over-voltage when the battery is not in the circuit.

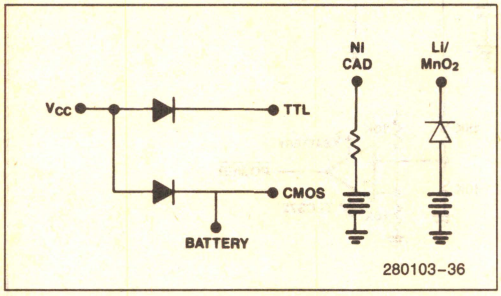


Figure 20. Simple Battery Isolation

Note that the battery charging accommodation in Figure 23 does not provide any protection from overcharging the battery. The others (Figures 20, 21 and 22) are somewhat protected by the lower input voltage used. Overcharging is addressed in the two stage battery charging circuits later in this section.

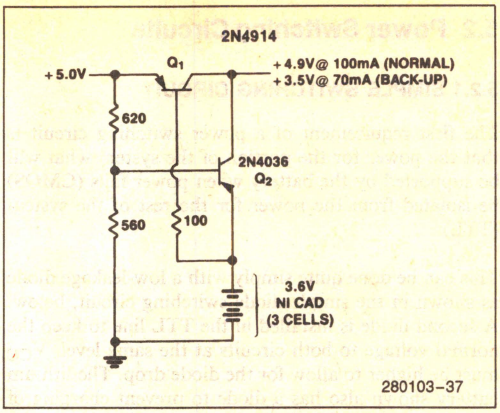


Figure 21. Dual Voltage Circuit

5.3 Protection From False Signals

5.3.1 RESET CIRCUITS

In a battery back-up system, care should be taken to protect the memory from false signals, during both back-up and power-up, which could alter the data that is to be preserved. To avoid any possibility of this happening, write enable ($\overline{WE}$) is held high during back-up and the normal chip select ($\overline{CS}$ or $\overline{RAS}$) is gated with the system power-up reset. For additional insurance, gate $\overline{WE}$ with the reset as well. The simplest reset circuit (Figure 25) is the resistor/capacitor, but it can briefly cause oscillations out of the associated logic circuits as it moves slowly through the threshold level. Putting a Schmitt triggered device on it improves the situation (Figure 24). The three transistor reset circuit (Figure 26) prevents oscillations by providing a more normal risetime to the logic circuits following the delay. When power first comes up, the RC time constant on its base keeps Q1 off which, in turn, keeps Q2 and Q3 off, holding $\overline{RESET}$ low. When the charge on the capacitor rises to threshold, Q1 turns on, turning on Q2 and Q3 and pulling $\overline{RESET}$ high.

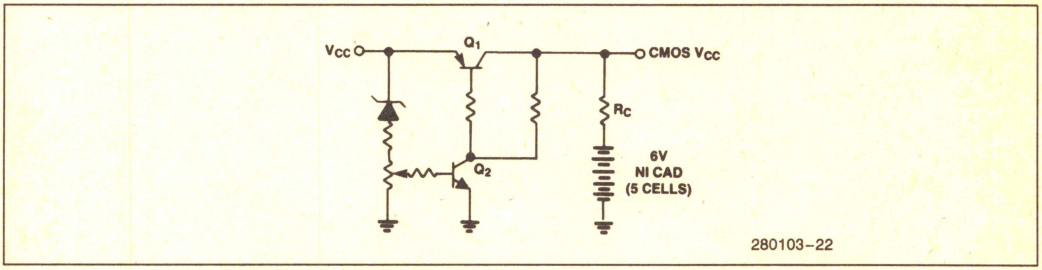


Figure 22. Transistor Isolation for Battery Back-up

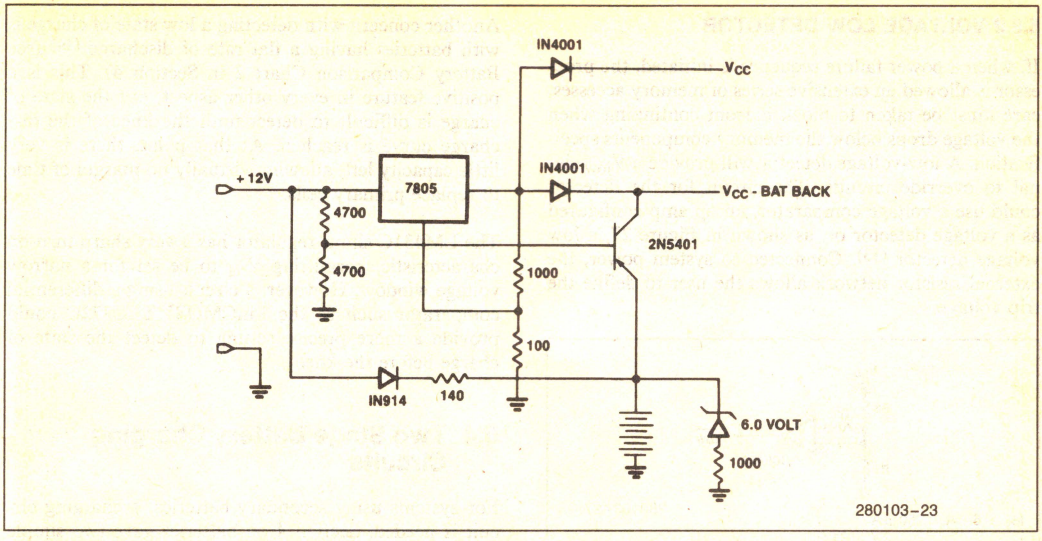


Figure 23. Transistor Switch for Battery

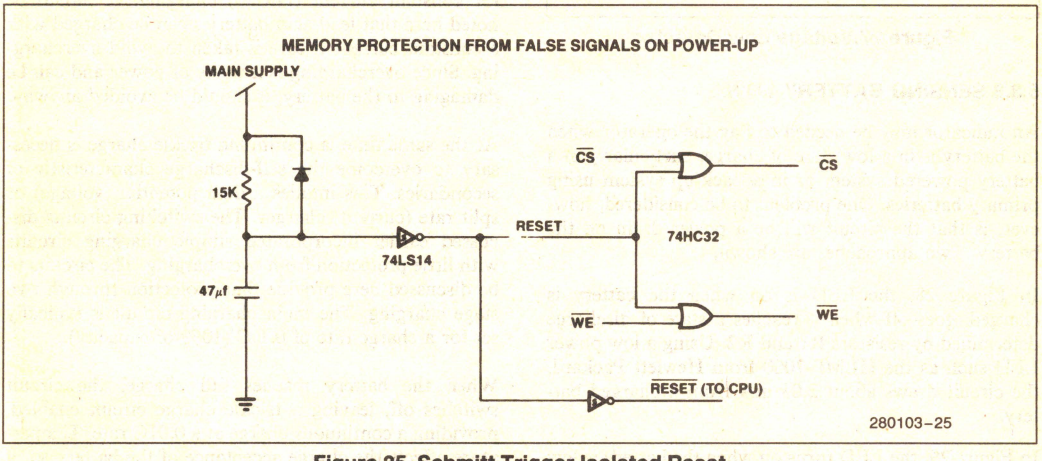


Figure 25. Schmitt Trigger Isolated Reset

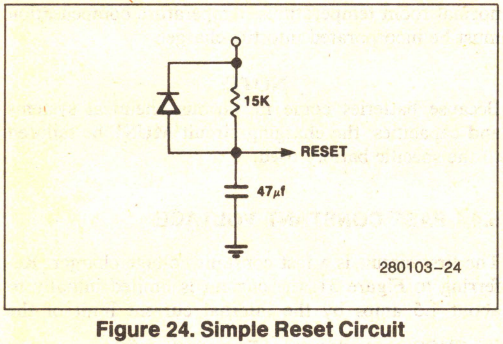


Figure 24. Simple Reset Circuit

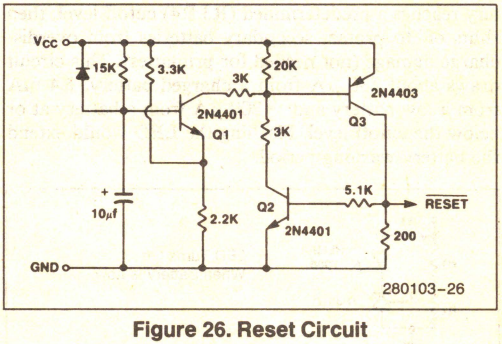
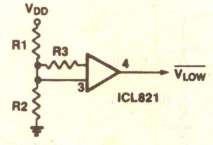


Figure 26. Reset Circuit Protects From Oscillation

5.3.2 VOLTAGE LOW DETECTOR

If, when a power failure sequence is initiated, the processor is allowed an extensive series of memory accesses, care must be taken to block it from continuing when the voltage drops below the memory components specification. A low-voltage detector will provide a V_{low} signal to override circuits. The circuit for the detector could use a voltage comparator, an op amp configured as a voltage detector or, as shown in Figure 27, a low voltage detector [13]. Connected to system power, the external resistor network allows the user to define the trip voltage.



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$I_{RI} \geq 6\ \mu A, \leq 50\ \mu A$

$$\text{Trip Voltage } V_{TR} = \left(\frac{R1\ R3}{(R1 + R3)} + R2\right) \times \frac{1}{R2} \times 1.15V$$

Figure 27. Voltage Low Detector

5.3.3 SENSING BATTERY LOW

An indicator may be needed to flag the operator when the battery is in a low state of charge, particularly in a battery powered system or in a back-up system using primary batteries. One problem to be considered, however, is that the circuit will be a power drain on the battery. Two approaches are shown.

In Figure 28, the LED is on when the battery is charged, goes off when it reaches a state of discharge determined by resistors R1 and R2. Using a low power LED such as the HLMP-7000 from Hewlett Packard, the circuit draws about 2.03 mA from a charged battery.

In Figure 29, the LED turns on when the battery is low (determined by R1 and R2). It stays on until the battery reaches a predetermined (R3,R4) cutoff level, then shuts off to protect secondary batteries from overdischarge damage (not needed for primaries). This circuit draws about 430 μA from a charged battery, 2.4 mA from a low battery and ~200 μA from a battery at or below the cutoff level. Flashing the LED would extend the battery warning period.

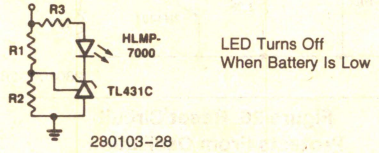

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Figure 28. Battery Low Indicator #1

Another concern with detecting a low state of charge is with batteries having a flat rate of discharge [14] (see Battery Comparison Chart 2 in Section 4). This is a positive feature in every other aspect, but the state of charge is difficult to detect until the knee of the discharge curve is reached. At that point, there is very little capacity left, allowing virtually no margin of time to replace primary cells.

The LM431C shunt regulator has a very sharp turn-on characteristic, permitting V_{ref} to be set for a narrow voltage window. However, a circuit using a differential comparator such as the LinCMOS* TLC372C could provide a more precise setting to detect the state of charge before the knee.

5.4 Two Stage Battery Charging Circuits

For systems using secondary batteries, a charging circuit is needed. Section 4 on batteries gave two simple circuits, one for constant voltage (lead-acid), the other for constant current (NiCad) charging. It should be noted here that lead-acid batteries can be charged with a constant current if care is taken to avoid overcharging. Since overcharging is a waste of power and can be damaging to the battery, it should be avoided anyway.

At the same time, a continuing trickle charge is necessary to overcome the self-discharge characteristic of secondaries. This implies a dual potential (voltage) or split rate (current) charger. The switching circuits discussed earlier incorporated simple charging circuits with little protection from overcharging. The circuits to be discussed here provide that protection through two stage charging. The main charging circuit is typically set for a charge rate of 0.1 C (10% of capacity).

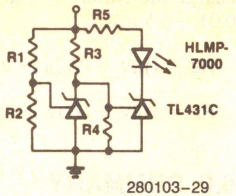
When the battery reaches full charge, the circuit switches off, leaving a trickle charge circuit enabled, providing a continuous charge at a 0.01C rate. Temperature affects the charge acceptance of the battery so, if it is to be re-charged at higher rates or in higher than normal room temperatures, temperature compensation must be incorporated into the charger.

NOTE:
Because batteries come in various chemical systems and capacities, the charging circuit MUST be tailored to the specific battery used.

5.4.1 FAST CONSTANT VOLTAGE

The first circuit is a fast constant voltage charger. Referring to Figure 31, the current is limited initially to about 1.5 amps by the internal current limit of the

*LinCMOS is a trademark of Texas Instruments



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LED Is Off When Battery Is Charged, Turns On When Battery Is Low And Turns Off Again When Battery Is Discharged To Cutoff Level.

$$R1 + R2 = \frac{V_L}{10(I_{ref})}$$

$$R2 = \frac{V_{ref}}{10(I_{ref})}$$

$$R3 = \frac{V_L - V_{RF}}{I_F} \text{ or } \frac{V_C - V_{ref}}{I_T}$$

$$I_T = \frac{V_C - V_{ref}}{R3}$$

$$R4 = \frac{V_{ref}}{I_T}$$

$$R5 = \frac{V_C - V_{LF} - V_{RF}}{I_L}$$

Where:

V_L = Battery Low Voltage
V_C = Battery Cutoff Voltage
V_{ref} = Regular Ref. Input Voltage
I_{ref} = Reg. Ref. Input Current
V_{LF} = Led Forward Volt. Drop
V_{RF} = Reg. Forward Volt. Drop
I_L = Led Min. Forward Current
I_F = Reg. Min. Forward Current
I_T = R3 + R4 Current To Turn On Led

For Example:

$$R1 + R2 = \frac{5.8V}{20\ \mu A} = 290K$$

$$R2 = \frac{2.5V}{20\mu A} = 125K$$

$$R1 = 290K - 125K = 165K$$

$$R3 = \frac{5.8 - 0.0005}{400\ \mu A} = 14.5K$$

$$I_T = \frac{5.1 - 2.5}{14.5K} = 179.3\ \mu A$$

$$R4 = \frac{2.5}{179.3\ \mu A} = 13.9K$$

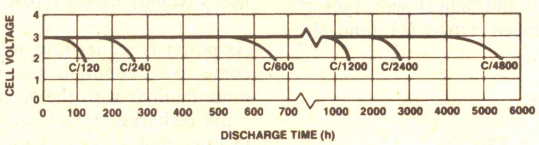
$$R5 = \frac{5.1 - 1.8 - 0.1}{2\ mA}$$

$$R5 = 1.6K$$

V_L = 5.8V
V_C = 5.1V
V_{ref} = 2.5V
I_{ref} = 2 μA
V_{LF} = 1.8V
V_{RF} = 0.0005V
I_L = 2 mA
I_F = 400 μA

Figure 29. Battery Low Indicator #2

Discharge Curves of Lithium Manganese Dioxide Cells ($LiMnO_2$)



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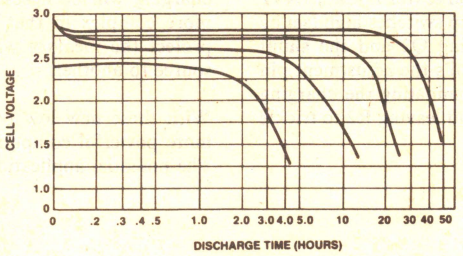
A. Typical Discharge Curves for Button Cells at 68°F (20°C)



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B. Typical Discharge Curves, Cylindrical Cells at 68°F (20°C)

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Figure 30. Discharge Curves of Lithium Manganese Dioxide Cells

LM317. As the charge on the battery increases, the current to the battery (through R6) decreases. When the voltage across R6 decreases below the voltage across R2, the outout of the op amp goes low, reducing the effective value of R1 and lowering the output of the voltage regulator. This terminates the voltage regulator charging of the battery and leaves the trickle charge resistor R7 to maintain the battery at the 0.01C rate. In addition, when the output of the op amp goes low, it turns on the LED, indicating the battery has reached full charge. A momentary contact switch is provided to initiate a charge cycle on a partially discharged battery. The diodes on the positive terminal of the battery prevent the battery from being discharged through the charger circuits when the line power is off.

5.4.2 CURRENT LIMITED CONSTANT VOLTAGE

The second circuit is a current limited constant voltage charger. The charge current is set by resistor R3. When the voltage across the battery reaches (for lead acid, $2.35 \times 3 =$) 7.05 volts indicating full charge, the shunt regulator turns on which, through the transistor, pulls the LM317 'adjustment' pin low shutting down the voltage regulator. This leaves the trickle charge resistor to maintain the battery.

5.4.3 CONSTANT CURRENT

The final circuit is a constant current charger. R3 adjusts the range wherein the voltage regulator turns on and off, R9 and R12 adjust the point at which the op amp switches. The charge current is set by R1. At 5.0V the op amp switches low (adjusted by R3 and R12), turning off Q2 and the shunt regulator and turning on Q1. The charge current is then determined by the differential between the 'output' and 'adjustment' pins of the voltage regulator, developed across R1 (and the transistor). In this case:

$$R1 = (1.2V - V_{CE})/0.1C =$$

$$R1 = (1.2V - 0.1V/50\ mA = 22\Omega$$

When the battery reaches full charge (for NiCad, 1.4V/cell $\times$ 5 cells = 7.0V) the op amp switches high (set by the zener diode and R9), turning Q2 and the shunt regulator on and Q1 off. This pulls the adjustment pin of the voltage regulator low, terminating the charging of the battery by the regulator and leaving R2 to trickle charge the battery at the 0.01C rate of (500 mAh $\times$ 0.01 =) 5 mA.

$$R2 = [12V - (V_{batt} + V_{diode})]/0.01C =$$

$$R2 = [12V - (7.0V + 0.8V)]/5\ mA = 840\Omega$$

6.0 SUMMARY

The new availability of a wide variety of fast CMOS products can lead to many new, low power applications such as lap or portable computers and high-speed solid state disks. The designer will have to consider a number of issues unique to this low power environment. For example, CMOS products have a much greater change from standby to active current than NMOS products so, while they expand the options (low power, high bandwidth, etc.) available to the design engineer, care must be taken to power them properly. This means proper decoupling and possibly more use of four layer printed circuit boards with power and ground inner layers. (Figure 34)

Many new products are in development (such as an 82C85 clock generator with the ability to stop the clock and an 82C08 CHMOS DRAM controller that supports extended refresh) that will help the designer take advantage of the features of the CMOS products and (s)he will have to stay abreast of them.

Systems to be operated with the limited power of a battery must be designed with careful attention to keeping active power low and making maximum use of the low power features of CMOS, features like stopping the clock and extended refresh. At the same time, means must be provided to notify the user when the battery needs recharging (or replacing).

As power is reduced, battery powered systems will become more common and the designer must become more familiar with the chemical systems available. We think rechargeable batteries will be the more prevalent in this application so knowledge of methods both for detecting batteries in a low state of charge and for recharging will be necessary. Battery backup is a little more complex in that special care must be taken to protect the memory when switching from one power source to another.

With these new low power products, new and much more powerful computing products can be developed. The potential applications are legion.

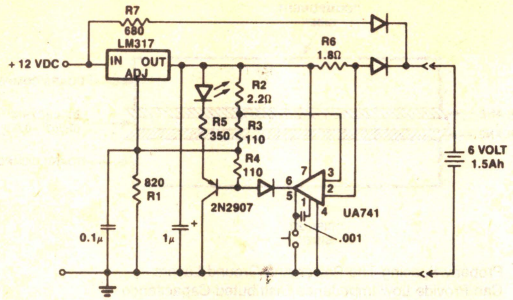

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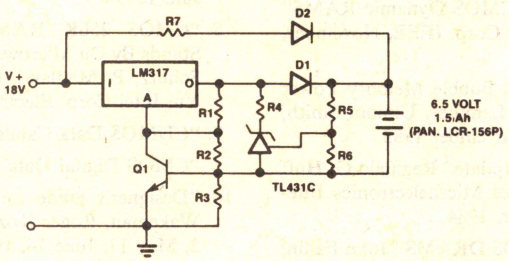
Figure 31. Two Stage Fast Constant Voltage Charger

Current Limited Constant Voltage Charger



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Overcharge Protection:

V_{REF} (TL431C) = 2.5V

$$\text{High Limit} \approx V_{REF}\left(1 + \frac{R5}{R6}\right)$$

High Limit = 2.35 V/Cell × 3 Cells = 7.05V

I_{REF} = 3 μA

I_{R5} (and I_{R6}) = 10 (I_{REF}) = 30 μA

$$R5 + R6 = \frac{7.05}{30\ \mu A} = 235\ K\Omega$$

$$R6 = \frac{V_{REF}}{I_{R6}} = \frac{2.5V}{30\ \mu A} = 83.3\ K\Omega$$

R5 = 235K − 83.3K = 151.7 KΩ

Trickle Charge:

$$R7 = \frac{(V+) - V_{D2} - V_B}{I_T}$$

$$R7 = \frac{18V - 0.8V - 7.05V}{15\ mA} = 676.7 = 680\Omega$$

Where:

V_{D2} = Voltage Drop Across D_2

V_B = Voltage Across Fully Charged Battery

I_T = Trickle Charge Current

Figure 32. Two Stage Current Limited Constant Voltage Charger

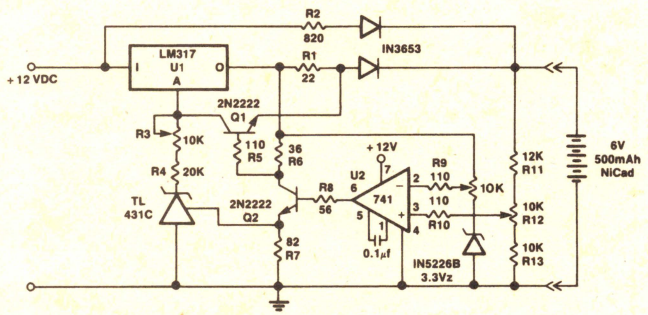

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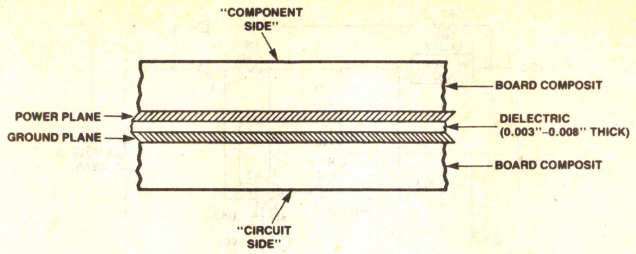
Figure 33. Two Stage Constant Current Charger



Properly Spacing The Power And Ground Layers
Can Provide Low Impedance Distributed Capacitance

Figure 34. Four Layer P.C. Board

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Modular Approach To C-MOS Technology Tailors Process To Application

KIM KOKKONEN AND RICHARD PASHLEY
Intel Corporation

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Modular approach to C-MOS technology tailors process to application

Despite the proliferation of applications, a few C-MOS process variations can address the functional requirements of many different products

by Kim Kokkonen and Richard Pashley, *Intel Corp., Santa Clara, Calif.*

☐ In the past few years, the interest in complementary-MOS technology and its applications to new products has exploded. Traditional arguments for C-MOS center on its low power dissipation, the large noise margins of complementary logic, and its simple ratioless design. With the advent of very large-scale integration, these arguments are taking on new meaning and importance.

As an example, Fig. 1 compares the performance of H-MOS (high-performance n-channel MOS) inverters with their equivalent in Intel's C-H-MOS (complementary high-performance MOS) technology. Though H-MOS's speed continues to improve with further scaling, its delay-power product is more than an order of magnitude higher than a C-H-MOS implementation with identical n-channel transistors. In a VLSI part with 50,000 gates, C-H-MOS could mean the difference between 1 and 10 watts of power dissipation, which might save the expense and difficulty of a sophisticated cooling system or extend a portable system's operating time by a factor of 10.

That C-MOS performance is now on a par with n-MOS technology has also accelerated its popularity. In addition, the density of C-MOS circuitry has improved dramatically with advances in technology. Finally, the number of process alternatives has grown so large that almost any integrated-circuit design can be supported with available C-MOS technology.

Unfortunately, the wave of enthusiasm for C-MOS and the needs of different applications have multiplied the number of approaches that C-MOS developers are taking. Several major issues remain in VLSI C-MOS design—namely latchup and soft-error prevention, interconnections, and logic-design techniques. A building-block approach with a limited number of basic process modules can be used to create a close-knit family of technologies that squarely addresses these issues and simultaneously supports a wide range of applications.

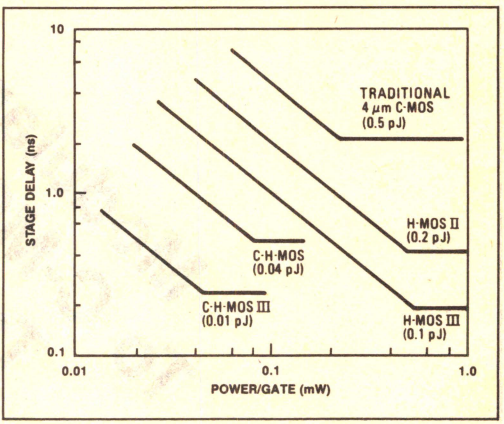
The basis for C-H-MOS

A firm foundation in n-MOS-transistor physics will support the advancement of C-MOS technology. As channel lengths approach 1 micrometer, n-channel transistors become more difficult to optimize because the standard 5-volt power supply causes problems with high-intensity fields. Improperly designed transistors may be unreliable as a result of hot-carrier injection into gate oxides, or they may cause less localized problems by injecting carriers into the MOS substrate—there to bleed charge from storage nodes or even trigger a destructive latchup.

The resources to develop and verify the reliability of a 1-μm n-channel transistor are well established and substantial. In Intel's C-H-MOS process, the basic design of the n-channel transistor is identical to its H-MOS counterpart, as shown in the table. Even at the more detailed levels of doping profiles, the H-MOS and C-H-MOS transistors are nearly identical.

Thus a high-performance C-MOS technology may be born out of an established n-MOS line. The relatively simple addition of an n-well in the same high-resistivity substrate results in a C-MOS process that serves as the basis for several optimized technologies. This is just a start, however, as other important issues remain.

Latchup has been the traditional nemesis of C-MOS. Given the presence of parasitic silicon controlled rectifiers within every bulk C-MOS chip, a current pulse of sufficient magnitude either inside or outside the chip may cause a catastrophic latchup. Many schemes have been proposed to combat latchup, ranging from carefully scrutinizing the layout (which imposes no burden on the technology) to a buried layer (which significantly in-



1. Power down. Despite the continuous improvement of H-MOS (high-performance MOS) by scaling, the delay-power product for C-H-MOS (complementary-MOS H-MOS) is more than an order of magnitude lower in the typical integrated circuit.

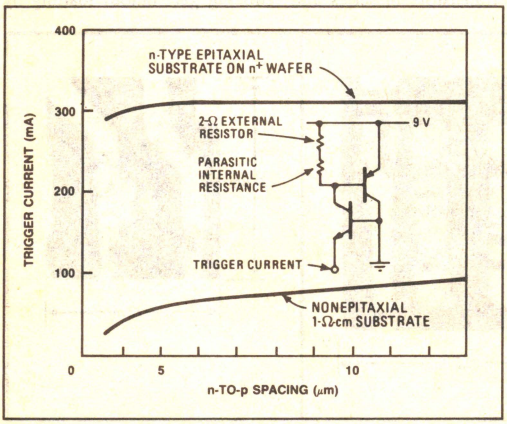
n-CHANNEL TRANSISTOR COMPARISON					
Technology		Gate-oxide thickness (Å)	Channel length (μm)	Threshold voltage (V)	Graded drain profile
n-MOS	C-MOS				
H-MOS I	—	700	3.0	0.7	no
H-MOS II	C-H-MOS	400	2.0	0.7	no
H-MOS II	C-H-MOS III	250	1.0	0.7	yes

creases complexity and processing cost). All have some degree of effectiveness.

A modular approach to a broad-based line of C-MOS technologies requires other measures besides mere physical latchup resistance. The latchup spoiler must be applicable to dynamic random-access memories, erasable programmable ready-only memories, and static RAMs, as well as to microprocessors and controllers. In order to improve latchup resistance, it cannot increase the distance between n- and p-channel transistors (this constraint is most significant in random logic and full C-MOS six-transistor static-RAM cells). The technique must be compatible with low-cost and large-volume manufacturing. Finally, the approach must be consistent with the use of an automated checking algorithm, so that every gate of a large semirandom logic design need not be scrutinized for latchup susceptibility.

Epitaxial benefits

Figure 2 shows the margin gained in latchup trigger current when an epitaxial substrate is used. The epitaxial substrate brings the same latchup benefits to all product lines, and in many cases provides additional advantages such as improved surface lifetimes (for dynamic RAMs) and reduced dc resistance (for E-PROMs and logic). Epitaxial substrates are now available in volume from commercial silicon vendors, adding less than 5% to the cost of a finished wafer. No additional or exotic fabrication equipment needs to be installed. Because the epitaxial substrate's heavily doped bulk effectively eliminates the vertically triggered latchup mode, it is possible to develop a set of computer-aided-design tools that can flag latchup-sensitive layouts on the largest VLSI chips.



2. Benefits. By raising the margin of latchup trigger current, an epitaxial substrate effects a dramatic improvement in combatting latchup, a major concern in complementary-MOS chip design.

Since grasping the phenomenon of upsets induced by alpha particles, in 1977, memory designers have taken care to ensure that enough charge is stored within each cell to minimize the problem. As critical chip dimensions are reduced, this problem becomes more severe, however, since both parasitic and storage capacitances are naturally reduced. For the latest 1.5-μm n-MOS process, stored charge is low enough to caution even microprocessor designers to guard against random storage nodes suffering from soft errors. Fortunately, C-MOS provides a natural barrier against soft errors if the storage node is located within the C-MOS well.

The well junction is reverse-biased by the power-supply voltage. The electric field at this junction naturally repels any carriers generated outside the well that might otherwise diffuse up to surface storage nodes. The combination of the well structure and an epitaxial substrate is even more effective. Here the funneling mechanism that usually collapses local electric fields during the passage of an alpha particle is also minimized. By using epitaxial substrates and the protection of a C-MOS well, the amount of charge collected during an alpha event can be reduced by an order of magnitude.

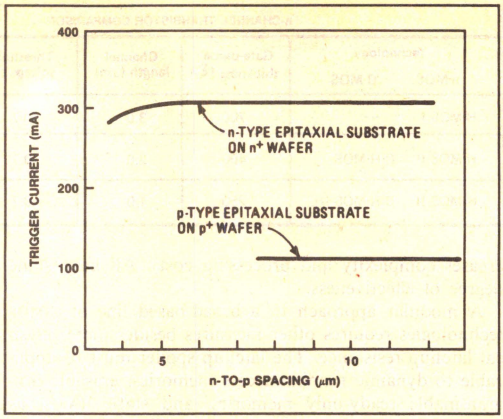
Of course, the designer must arrange for the storage node to reside within the well. This constraint, combined with other performance issues, leads to different choices of well and substrate polarities, depending on application. For example, in a C-MOS technology that is optimized for dynamic RAM, the ideal memory cell should have a p-channel pass gate and a p-channel capacitor located within an n-well in a p-type substrate. The p-channel transistor is chosen because it injects far fewer spurious carriers into the substrate and thus does not by itself disturb the state of neighboring cells.

The conductance of the p-channel device, while lower than that of an n-channel device of the same size, does not degrade the RAM's performance, since dynamic-RAM sensing is limited primarily by the amount of stored charge. Experimental results with C-H-MOS dynamic RAMs based on these principles show a soft-error rate of less than 300 FIT (failures in time, or device failures per billion hours) at a power supply of only 3 V. This is an improvement of more than three orders of magnitude over traditional n-MOS dynamic-RAM technology and offers the possibility of dynamic-RAM systems that require no error correction and that are compatible with low-voltage battery backup.

High-density, high-performance static RAMs present the other side of the coin. The smallest static-RAM cells today are built using polysilicon-load resistors that sustain the stored-node voltage. On the time scale of an alpha event, however, these resistors in effect do not exist. Because the storage node's RC time constant is on the order of milliseconds and the alpha event's time scale

is nanoseconds, the cell appears dynamic. In this sense, polysilicon-load static-RAM cells are very similar to dynamic-RAM cells. The major difference arises in the way the cells sense the cell's information. The static-RAM cell provides a direct current, and to maximize the cell's performance, that current must be as large as possible while contained in a minimum area. Thus the chip designer must use high-gain n-channel transistors for the cell's pass gates and pulldowns. For good soft-error protection, then, the cell must be located in a p-well within an n-type substrate.

The p-well approach benefits even full C-MOS six-transistor static-RAM cells. The area of such cells depends strongly on the distance allowed between n- and p-channel devices. Using a straightforward implementation of epitaxial C-MOS, the p-well approach provides more margin against latchup at small n-to-p spacings (Fig. 3). This phenomenon occurs because of the differing diffusion properties of n- and p-type dopants. The heavy doping in the n-type substrate is less mobile than is the p-type dopant, resulting in less outdiffusion during thermal processing and thus minimizing the shunt resistance that controls latchup.



3. P-well margin. With an epitaxial substrate, a p-well structure (upper curve) yields a greater margin against latchup than n-well at smaller n- and p-device spacings.

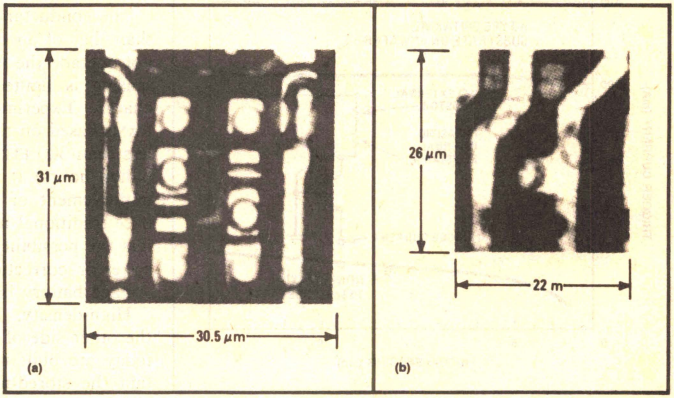
Hooking it up

One of the challenges of C-MOS in logic applications is interconnection. Designers of n-MOS chips are accustomed to buried contacts, which directly connect n-type polysilicon and n-type transistor source or drain regions. Because C-MOS requires contact to both p and n regions, the traditional n-type buried contact becomes much less useful, and a version suitable for both diffusion polarities is quite difficult to implement. This increases the burden on contact and metallization modules.

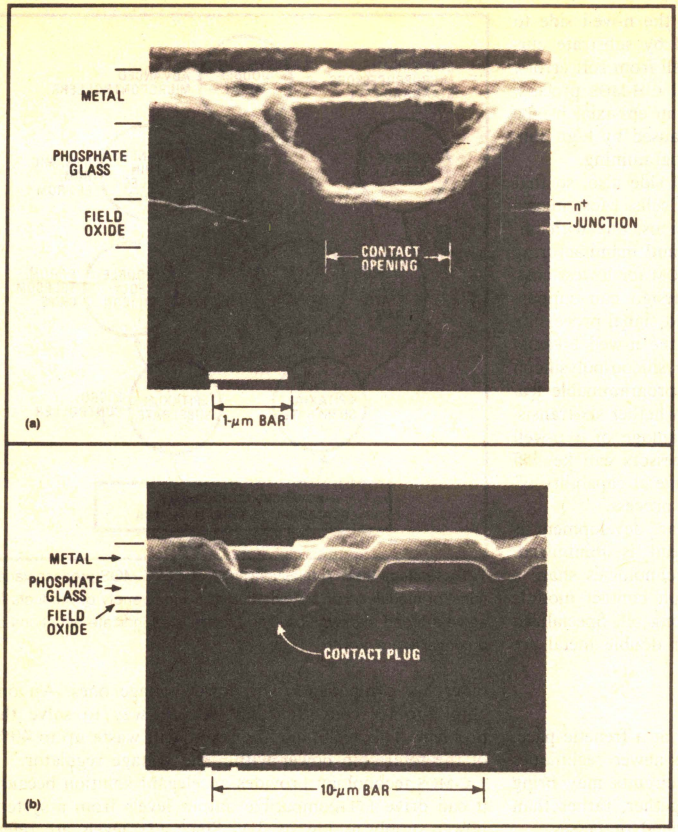
For high-density C-MOS logic, the first level of metal is all but consumed by local connections between p and n transistors. The payback from adding a second level of metal for longer-distance routing is very high. A good example exists for the six-transistor static-RAM cell commonly used by logic designers. Figure 4 compares single- and double-metal versions of this cell, both implemented with 1.5-μm design rules. Here the second-metal layer provides the bit lines for the cell. Similar arguments justify the use of second metal in global power, clock, and data routing in complex microprocessor chips.

Contacts themselves are more difficult to build in C-MOS. N-MOS technology accustomed process engineers to adding a phosphorus contact plug after the contacts have been etched. This plug brought several advantages: the phosphorus gettered metallic contaminants from the wafer, reducing junction leakage; and the high-temperature diffusion rounded the profile of the contact sidewall, easing the step coverage of the metal subsequently deposited. Further, the plug had self-aligning features. If the contact etch attacked the silicon substrate or if the contact was misaligned toward the field-oxide edge, the plug would rejuvenate the resulting weakened junctions. In C-MOS, these same attributes must be obtained differently, through improved fabrication, cleanliness, new gettering techniques, improved dielectrics, and tightly controlled contact etching. Figure 5 shows the difference in implementing a 1.5-μm contact structure in n-MOS and C-MOS.

Along with the proliferation of C-MOS technologies has come a wave of innovation in C-MOS design techniques. For digital logic, the major contenders for broad use are full complementary design and domino logic, first proposed by AT&T Bell Laboratories (Fig. 6). For many applications, traditional C-MOS logic is a winner. It requires no clocks, has larger operating margins, and uses fewer transistors for simple gates. For more complex gates, however, domino logic uses fewer transistors and runs faster. The speed results from connecting fewer transistors in series and reducing gate-fanout loading by



4. Payback. The use of double-metal layers for a six-transistor static-RAM cell can produce a large savings in real-estate. In two cells implemented with a 1.5-μm design rules, the savings can amount to one third of the total area. The cell at right uses second-layer metal for bit lines.



5. Making contact. Contacts are more difficult to build in C-MOS than in conventional n-MOS. The phosphorous contact plug used in n-MOS after contact etching (a) adds desirable features such as reduced junction leakage and improved step coverage by the metal layer. To gain the same advantages in C-MOS requires greater process control (b).

up to a factor of two compared with full C-MOS.

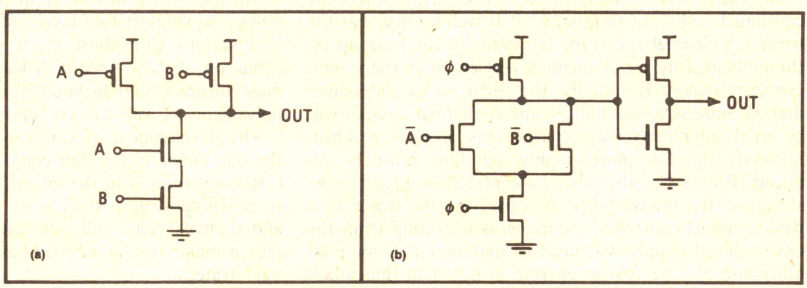
Interestingly, the choice of design style influences the optimal type of C-MOS well. The speed of full C-MOS is limited by the slower of the two transistor polarities. Since the trip point is quite close to half the power supply, the time required for either transistor type to discharge its load capacitance by about 2.5 V sets the gate's speed. Since the p-channel device is the weaker one, it pays to choose a well type that improves the p-channel's conductance. P-well does this because the p-device is fabricated in an uncompensated substrate and thus has maximum mobility. Comparisons between n- and p-well construction show that the p-channel's conductance may be improved by as much as 10% with the proper well type.

By contrast, domino logic is at its best in an n-well technology. Here, the n-channel transistor dominates both performance and transistor count. Placing the n-channel device outside the well improves its conductance and reduces the dominant parasitic junction capacitance. Density also increases because no well contacts are required for the majority of the transistors.

The twin-well approach to C-MOS blurs these distinctions. In this approach, a high-resistivity epitaxial layer is grown on a heavily doped starting wafer. Then the doping for each transistor polarity may be independently optimized without need for doping compensation. Performance arguments based on mobility or junction capacitance thus become moot. Nonetheless, domino logic will still be best on a p-type substrate (equivalent to n-well) because it does not require well contacts to collect the large parasitic substrate currents from the n-channel transistors, thus improving packing density.

Matching process to product

These and other technical arguments may be combined into a consistent strategy (Fig. 7) for creating a line of C-MOS processes serving a broad marketplace. For at least the next several years, a complete technology line must include C-MOS based on both p- and n-type substrates. Fortunately, choosing epitaxial-latchup control minimizes the development cost of running both process-

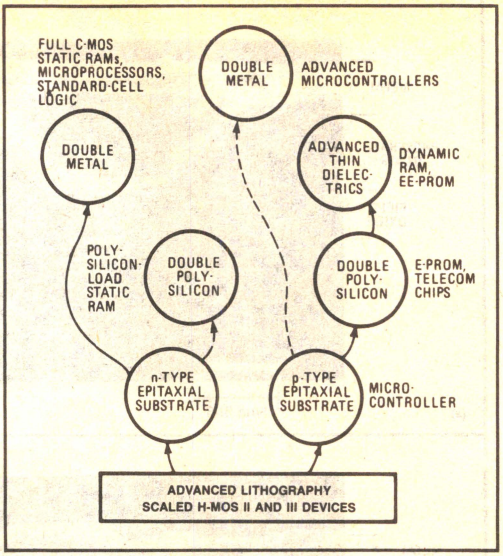


6. Logic. Two major contenders for digital logic design are full complementary (a) and domino logic (b). The former requires no clocks and is simpler for many applications. Domino logic, which performs best in an n-well technology, is faster and simpler for more complex circuits.

es. Dynamic RAMs are supported on the n-well side to minimize pattern sensitivities induced by substrate currents while protecting the p-channel cell from soft errors. E-PROMs are built in a similar n-well C-H-MOS process. Placing Intel's n-MOS E-PROM cell in an epitaxial p-type substrate eliminates parasitic effects caused by high substrate currents flowing during cell programming.

Microcontrollers land on the n-well side also, so that they may incorporate on-chip E-PROM cells. Most microcontroller products come in two versions, one with on-chip E-PROM for system-development and manufacturing flexibility, and another with on-chip ROM for lowest cost. Using n-well C-MOS, a single core design can support both versions. Telecommunications and signal-processing products can also take advantage of the n-well E-PROM process, both for its high-quality polysilicon-polysilicon capacitors and for the E-PROM cell's programmable features. High-performance static RAMs, whether six-transistor or polysilicon-load, can take advantage of a p-well C-H-MOS process. High-end microprocessors can key off the dense n-to-p packing and double-metal capability offered by the six-transistor static-RAM process.

Because these processes are modular, development is simplified and manufacturing overhead is minimized. Just as all the 1.5-μm C-H-MOS III technologies share a common transistor module, the difficult contact module was developed once to be shared among all. Specialized features such as double polysilicon or double metal are extensions of the common base.



7. Technology tree. A relatively small line of C-MOS process variations, or modules, can be matched to a wide variety of products to serve a broad marketplace. The broken lines indicate directions of potential future growth.

The future

C-MOS technology is still developing at a frenetic pace. Surprisingly, the application of some newer techniques and the demands of next-generation circuits may bring the various forms of C-MOS closer together, rather than further splitting the number of integrated processes.

One example of this trend is the development of a trench-isolation technique for separating n and p devices. When this module is perfected, there will be no reason to develop six-transistor static-RAM cells on p-well technology. The near-ideal trench isolation will prevent latchup on either substrate type. Similarly, if stacked C-MOS static-RAM cells can be perfected, there will be no need for polysilicon loads. The stacked C-MOS cell will have the same density but with improved performance and soft-error immunity. At that time, twin-well C-MOS on a p-type substrate, augmented by specialized features for specific product lines, will become the one approach to a broad line of C-MOS processes.

Another factor affecting future C-MOS integration is the continued scaling of transistors. It is well known that the weaker p-channel transistor is gradually catching up on the n-channel device as channel lengths enter the submicrometer region. Eventually, the performance differences may become so small that p- and n-channel devices will be used interchangeably. Before this level is reached, however, the 5-V power-supply standard must be reduced. Because of the large base of TTL-compatible designs and the impossibility of converting the world to a new standard overnight, components operating from the new reduced supply will need to maintain TTL compatibility and also be able to operate in a system that mixes older 5-V components with lower-voltage ones. An on-chip 5-to-3-V converter may be one way to solve the problem. This technique, however, will waste up to 40% of the total chip power within the voltage regulator.

C-MOS technology provides an elegant solution because it can drive TTL-compatible output levels from a system power supply as low as 3 V. Since TTL levels are referenced to the negative (ground) rail, the grounded substrate offered by n-well C-MOS is a much-preferred means of integrating submicrometer transistors into such a system. This will be a strong motive to standardize on p-substrate C-MOS.

A final factor that tends to drive future C-MOS processes toward commonality is the growing importance of RC delays in overall chip performance. The latest high-performance static RAMs use an aluminum strap in parallel with the polysilicon word line because the RC delay induced by even the best refractory metal polycides is several nanoseconds too long. Studies of dynamic RAMs larger than 1 megabit similarly indicate that refractory word lines will probably be inadequate, forcing the technology to support two layers of metal. Combining these observations with those made previously regarding the evolution of static-RAM cells leads to the conclusion that most future C-MOS technologies will have two layers of polysilicon as well as two layers of metal.

The development of silicon-on-insulator technology is the one major factor that could renew the divergence of C-MOS approaches in the future. However, until the quality of SOI substrates is adequate to support dynamic RAM and E-PROM cells, and not just static logic, it will not play a major role in a broad-based and modular technology strategy. □

Memories

CMOS outshines NMOS on high-speed digital chips

After many years in the shadow of NMOS technology, CMOS is taking over the bulk of NMOS applications, with high-speed, low-power architecture. A new CMOS RAM proves it can top NMOS in both performance and price

Steve Smith
Program Manager
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Senior Engineer

Intel Corp.
Static RAM Operation
Santa Clara, CA

Until recently NMOS technology was the front-running process for manufacturing digital memories and logic. It was simpler and cheaper than its archrival, CMOS. It was faster, too, and had no latch-up problems. But the scene has changed. NMOS is giving way and CMOS is taking the lead.

For one thing, today's state-of-the-art NMOS processes are far more complex than those of their predecessors. Four or five transistor types have replaced the two basic types of the past. The single-layer polysilicon and metal-interconnect schemes of early NMOS devices are losing ground to double-level polysilicon and double-level metal.

At the same time, RC time-constant delays, once critical CMOS speed limiters, are dropping, thanks to a variety of low-resistance gate techniques. The result is that the complexity of NMOS fabrication—and hence its cost—is now on par with that of CMOS.

Many factors at work

Other factors have also been at work. CMOS, with its new submicron, high-speed-geometry transistors, has been rapidly moving into NMOS high-speed digital-IC territory. In addition, its latch-up sensitivity has been brought under control, and transistor scaling has boosted the formerly weak p-channel CMOS chip to reasonable strength.

Of course, CMOS's traditional forte, low power dissipation, hasn't changed, so new chip designs can be pushed to the limit without violating package power limits. And the inherently high CMOS noise immunity allows future power-supply scaling to low signal levels with a minimum

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number of circuit changes. Clearly, CMOS is moving into the No. 1 spot for all semiconductor classifications.

Taking advantage of the new capabilities of CMOS, Intel has developed a CMOS version of its high-performance NMOS process (HMOS III). The new technology, called CHMOS III, uses p-wells on n^- Epi-layer processing, which incorporates 1.3-μm p and n devices. Transistors are interconnected by two-layer metal and single-layer polysilicon. P-well processing maximizes performance. This permits tighter well-to-

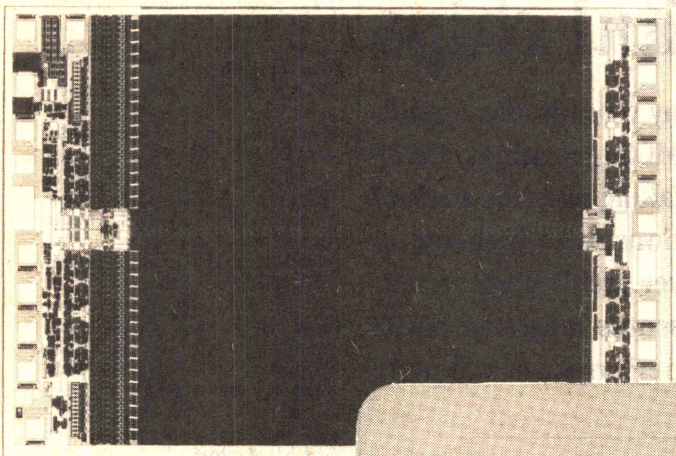

Fig. 1. A state-of-the-art process, Intel's CHMOS III eliminates the traditional CMOS drawbacks—low speed, latch-up, and low density. The 51C67 16-Kbit CHMOS III RAM has 35-ns access time and dissipates less power than previous 1-Kbit chips.

diffusion spacing than other methods —and the denser packing of devices.

An n^- Epi layer on an n^+ substrate virtually eliminates latch-up woes, while the low resistivity of the n^+ substrate shunts mosts of the dangerous substrate current to the V_{CC} supply. P-well V_{SS} taps collect any stray well currents. Double-level metal reduces parasitic RC delays in the CHMOS III. It eliminates all polysilicon interconnections of heavily loaded nodes and reduces delay significantly. For example, a typical metal-strapped static-RAM word line has a delay of ¼ ns. Using an equivalent length of polysilicon, the delay is close to 15 ns.

Sound physics

Proving that the semiconductor physics theory behind CHMOS III is sound, Intel has designed a new 16 K x 1-bit static RAM, the 51C67, using the process (see *Fig. 1*). Performance tests indicate that the device's maximum read-write cycle time is 35 ns—measured between signal lows of 0.8 V and highs of 2.0 V—with 100-mA active and 10-mA standby current limits.

To achieve a speed of 35 ns consistently throughout a manufacturing process, various process-tolerant circuit architectures must be used. One of the most process-sensitive circuits is an input buffer. Typically, a simple inverter serves as the first stage of the buffer. Although such an input device can be optimized for typical (5-V) operation, its performance is very sensitive and can degrade rapidly with variations in V_{CC}, temperature or processing.

The 51C67's input buffer uses a resistor-divider ratio to set a reference voltage (V_1) of about 1.4 V as shown in *Fig. 2*. Voltage V_1 is fed into a feedback reference generator to produce a bias voltage (V_2) for the input buffers. Voltage V_2 is maintained at such a level that the input inverters are biased just to their trip point. Thus, a small change in a pad voltage will cause a buffer's output to trip.

The reference generator is designed so that V_2 depends only on V_1. An inverter's trip point, in turn, depends on bias voltage V_2. In effect, the input buffer trip point is determined by the resistor-divider

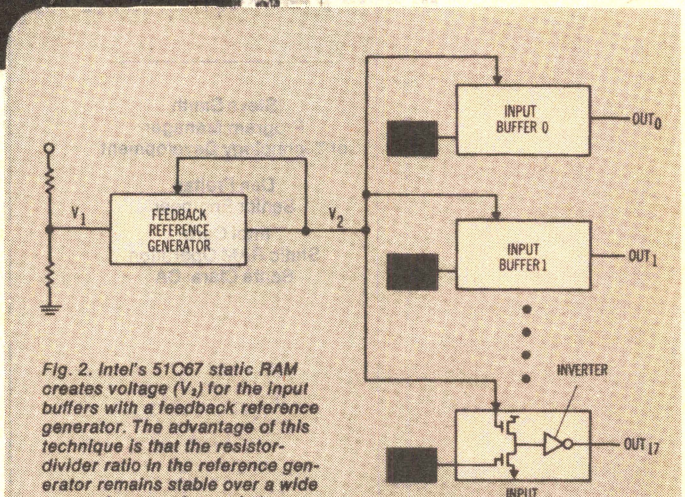

Fig. 2. Intel's 51C67 static RAM creates voltage (V_2) for the input buffers with a feedback reference generator. The advantage of this technique is that the resistor-divider ratio in the reference generator remains stable over a wide range of processing variations.

voltage. Since a resistor divider is constant over any processing variation, the input buffer's trip point is also constant over these variations.

In a high-speed RAM, the heavily loaded data path is usually clamped to avoid large, low-slew voltage swings. These clamped data signals are fed to a differential sense amplifier for level restoration and buffering before being fed to the data-out terminal pin.

The sense amplifier is usually the first device to fail under extended V_{CC}-range operation because it is a saturated-transistor circuit strongly dependent on bias voltage. Improper biasing causes the input, load, or current-source transistors to fall out of saturation. This leads to reduced gain, less common-mode rejection, and ultimately, operational failure.

To extend the usable range of the sense amplifier, the 51C67 uses a bias-controlled differential amplifier (see *Fig. 3*). The amplifier's load and current-source transistors are biased by V_1 and V_2. As V_{CC} rises or falls, V_1 and V_2 are varied to rebias the amplifier. The bias generator is self-compensating for variations in temperature, process, and voltage. In standby, both the bias generator and sense amplifier powerdown, eliminating any linear DC power dissipation.

After differential data signals have been amplified to full CMOS levels, additional buffering is necessary before driving the output pin. The 51C67 uses a preferential delay technique to speed up the read-1 path—the reading of a logic-1 from the device. That is, the read-1 path through the buffer inverters is optimized at the expense of the time through the read-0 path.

To compensate for the additional delay in the read-0 bath, the sense-amplifier output is preset to zero upon the transition of any address. Essentially, this gives the read-0 path a head start, so the additional delay through the sense amplifier does not limit the overall access time of the device.

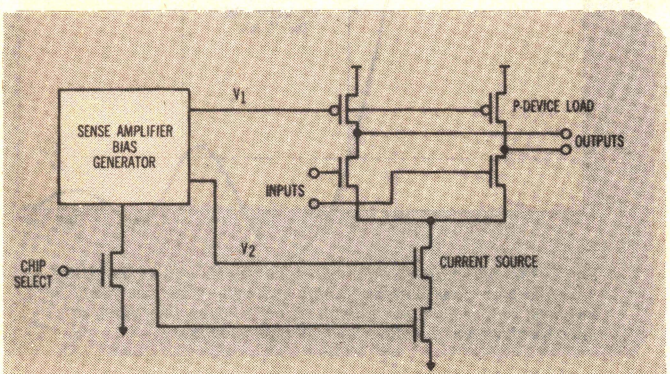

Fig. 3. A bias generator that self-compensates for temperature, voltage, and processing variations extends the range of the 51C67's sense amplifiers. Voltage V_1 and V_2 change with variations in supply voltage to rebias the sense amplifiers.

The 51C67's preset-to-zero scheme eliminates any unknown data-out states. It turns out that the same pulse used to preset the output also equalizes the data path. As in any equalized device, the sense-amplifier input becomes invalid during equalization. With the inputs invalid, the output data is indeterminate.

To eliminate the indeterminate state, a designer can latch, three-state, or preset the output. Latching requires a latch/unlatch clock with adequate margin to prevent latching the wrong data. But margins built into the latch directly increase access time, a less-than-desirable situation for a high-speed RAM.

Three-stating the output offers little improvement since during equalization, the output state is determined by the output load configuration. Presetting, on the other hand, forces data values to a known state during equalization, allowing the optimization of the other state.

Writing and power-down

There are always tradeoffs between the read and write circuitry of a RAM. For example, high-speed design practice dictates strong column clamps to minimize bit-line voltage swings. This is a good procedure for fast reads, but the write drivers must pull against the clamps when writing data to a memory cell. The result is a degraded low signal level, which, under some conditions, may be insufficient to write correct data to the cell.

In the 51C67, column-load switching is used to get the best of both worlds. During a read, strong column clamps enhance read speed while eliminating marginal cell conditions such as read-disturb in a noisy environment. During a write, the column clamps are switched off, allowing the column drivers to pull the column essentially to V_{SS}. This low level ensures a solid write signal in any system environment.

A key characteristic of the 51C67 is its power-down feature. During deselect—chip select (CS) set to a logic 1—the RAM goes into a low-power standby mode, dissipating only 1/10 of its active power.

However, some high-speed portions of a system cannot take advantage of power-down. An instruction cache, for example, must be continuously updated with new instructions, and thus can never be deselected.

For non-power-down applications, Intel offers a sister chip to the 51C67, the 51C66. This RAM's access time is specified at 20 ns. Both active and standby power are specified the same, 100 mA. The 20-ns access time is the equivalent of an output-

enable access for a common I/O device. In other words, after the addresses are first set up, the CS pin (equivalent to an output enable) is brought low. For normal access—with CS always low and the addresses changing—the read-access time is the same as that of the 51C-67, namely 35 ns max.

Effects of noise

A data sheet may specify a RAM as a 35-ns device, yet the system fails to operate with a 40-ns strobe signal. Before concluding that the RAM is bad, the designer should check the system's cleanliness.

First, high-speed devices use extremely strong output drivers. An output can easily generate a 150-mA peak during switching. When driving a 100-pF load with a V_{SS} inductance on the order of 10 nH, the low output-level can easily bounce up to 0.8 V (see *Fig. 4*). With data-word lines of 16 or 32 bits, the V_{SS} line must be implemented with large-gauge wire.

The bouncing of V_{SS} not only degrades speed. It affects input-level specifications such as the input high- and low-levels V_{ih}/V_{il}. If the input to the device sits 200 mV above the trip point and the output driver bounces 400 mV below ground, the device suddenly sees an effective input voltage 200 mV below the trip point. Such a large amount of noise means that the input must be driven further to overcome the so-called V_{SS} feedback (see *Fig. 5*).

High-speed systems can be built, of course, but they require care. Reducing inductance is the first step. Inductance in power-supply lines causes anI x L drop when large current surges occur. That is, the magnitude of the drop is L (di/dt). Thus, memory boards that were satisfactory for the last generation of RAMs may be inadequate for the latest super RAMs because of the larger current glitches made possible by strong output drivers. Clearly, power planes or gridding with ample bypass capacitor density are a necessity in the power-distribution design of today's high-speed memory systems.

To reduce the inductance of components, lead lengths should be trimmed appropriately on filter capacitors. Long leads interface with the filtering effect since a lead's series inductance increases the capacitor-to-power supply impedance.

Series inductance in an output lead is just as detrimental because it contributes to impedance mismatching with the signal transmission line. Mismatching causes the ringing of the output signal, and if the ringing is severe enough, it causes a false data transition to the next stage. Thus, the bottom line on high-speed memory system performance is that it is as dependent on careful board design as on fast memory access-time.

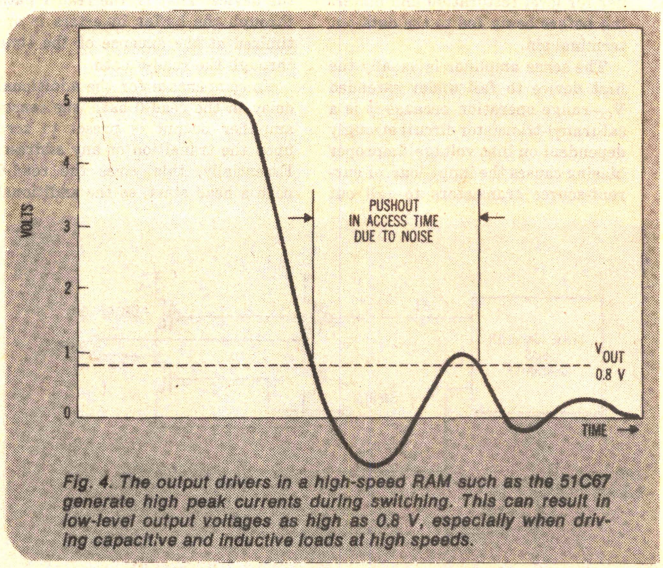

Fig. 4. The output drivers in a high-speed RAM such as the 51C67 generate high peak currents during switching. This can result in low-level output voltages as high as 0.8 V, especially when driving capacitive and inductive loads at high speeds.

Fast RAM applications

Since microprocessors operate at fixed clock rates, their data-fetch cycles consume a predetermined amount of time based on the clock rate. If the access time of external RAM is longer than a data-fetch cycle, wait states must be generated. Essentially, a wait state is wasted time since the processor cannot execute its current instruction without the data coming from the RAM. The end result is reduced system-level throughput.

One technique for decreasing the memory-access time delay is to use a fast intermediate memory—called a cache memory—located between the processor and the large main-storage memory. Caches are designed with extremely fast static RAMs that store blocks of data from main memory. Since static RAMs are faster than the dynamic RAMs that make up main memory, the processor can access data from the cache within its data-fetch cycle and thus eliminate time-consuming wait states.

Cache RAM is a system application that demands the highest speed RAMs. But the most stringent demands don't always come from end-user system designers. Most logic-system designers use microprocessor emulators to debug new applications. And the emulator itself demands the fastest static RAMs.

Emulators use RAMs for programmable control store, state machines, and capture memory. Each of these functions emulates the target microprocessor's internal functions. As

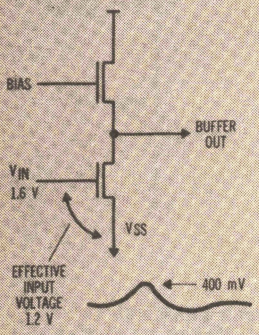

Fig. 5. When the V_{ss} line bounces (as shown in Fig. 4), it affects the high- and low-level voltage inputs to the RAM. Here an input voltage of 1.6 V is reduced significantly—to 1.2 V—by a 400-mV bounce in the V_{ss} line. Noise such as this effectively debiases the input, slowing down the throughput of the device.

such, they must be capable of running at the speed of the processor's internal clock rate.

The internal control memory must be faster than the external data memory since one external fetch cycle is equal to many internal control cycles. To make matters worse, an emulator is a board-level system that must operate at chip-level data speeds.

Another problem is writing to the RAM. One of the functions of an emulator is to trap and record blocks of data in real time. To do this, the RAM must be able to write as fast or faster than it can read.

RAM speed is the priority in high-performance systems, but dense chips—large storage capacity—are also desirable. In a cache memory, if the data block is small, there is little chance of having all the needed data within a single block. To maximize the "hit rate" (the probability of having the required data in the cache at the proper time), a large cache is necessary.

Emulators can also benefit from large memories. Circuits, such as a programmable control store, copy the functions of internal control ROMs, which are often large memories. And circuits such as the capture RAM determine how much status data can be recorded during a trapping operation. Traditionally, however, only small memories (1 to 4 Kbits) had sufficient speed to serve in these applications. Thus, there is a clear need for high-density, high-speed static RAMs.

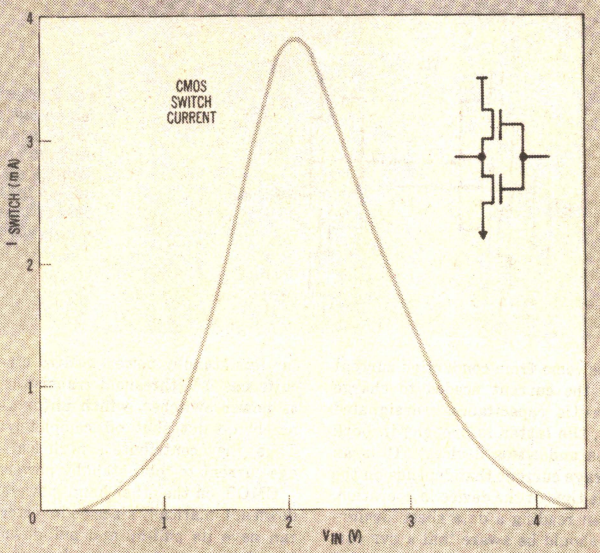

Fig. 6. One of the contributors to a CMOS RAM's power dissipation is simultaneous conduction current, which results when the CMOS complementing transistors are both partially on during switching. Reducing transition time reduces dissipation.

NMOS can't do the job

The principal difficulty with NMOS technology is that it is up against a power wall. As speed demands increase, more powerful transistors are required to charge external parasitic capacitances faster. The NMOS solution is transistor scaling—building a smaller and more powerful transistor. Scaling, therefore, puts a greater number of powerful transistors on a single chip. But the increased density means that the chip must dissipate more power per unit area, and the entire chip, therefore, must be capable of dissipating more power.

As a chip's dissipation increases, the limits of its package dissipation are reached. When this happens, the only alternative is to slow down the circuitry to reduce the power. As a result, the tradeoff in NMOS technology is to build slower devices to conserve power.

CMOS technology, on the other hand, has no such limitations. The CMOS advantage lies in its complementary pull-up and pull-down transistors. Since only one device is on at a time, DC power dissipation is extremely low. Using CMOS, it is possible to get the best of both worlds—very dense chips that can run at high speed.

The major power contributions in

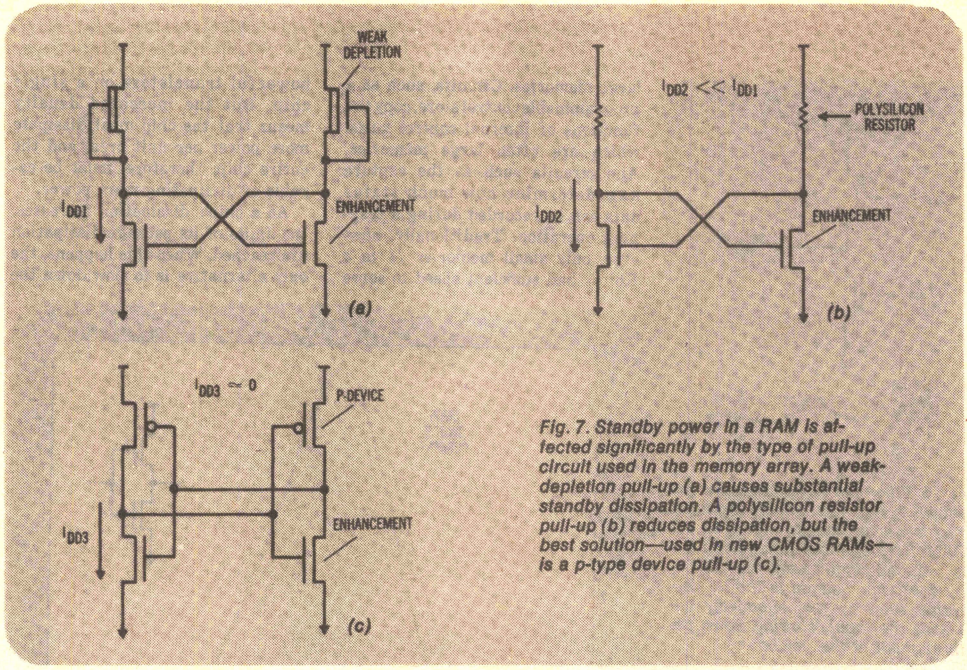

Fig. 7. Standby power in a RAM is affected significantly by the type of pull-up circuit used in the memory array. A weak-depletion pull-up (a) causes substantial standby dissipation. A polysilicon resistor pull-up (b) reduces dissipation, but the best solution—used in new CMOS RAMs—is a p-type device pull-up (c).

CMOS come from conduction current and the current needed to charge parasitic capacitances (designated CVF, the latter is present in both CMOS and NMOS devices). It is an average current that depends on the cycle time of the device in operation. When reading a data sheet, designers should be aware that a CVF current specified at a frequency of 1 MHz is meaningless if the device will actually cycle at 20 MHz.

Simultaneous conduction current (see *Fig. 6*) is switching current. In a CMOS inverter, both the pull-up and pull-down transistors are on for a brief time as the output switches.

High-speed CMOS devices may also have a DC component. The resultant DC power comes mostly from linear circuitry dissipation by non-CMOS devices such as differential sense-amplifiers, which are necessary in memory devices to achieve maximum performance, even at the expense of high power dissipation.

A major advantage of CMOS over NMOS RAMs is that CMOS dissipates far less standby power. NMOS circuits use 0-V threshold transistors as power switches, which unfortunately do not shut off completely. Thus, they contribute a high leakage-current to total standby power.

CMOS, on the other hand, powers down automatically since no inverter can have its pull-up and pull-down transistors on simultaneously in the DC case. In fact, CMOS linear-circuit leakage is reduced to almost zero by using ½-V threshold p- and n-type power-switching transistors.

A second source of standby power dissipation is in the memory array itself. Since a RAM cell is simply a set of cross-coupled inverters, the type of pull-up an inverter uses has a significant effect on standby power dissipation.

Some NMOS RAMs use a weak depletion-transistor as a pull-up (see *Fig. 7a*). The standby power is I_{pu} times the number of memory cells. For a 16-Kbit RAM having a weak-depletion drain current of 10 μA, the arrays contribution to standby current is 16 mA. Such a large current is far from optimum for a large memory array.

A resistor load is another type of pull-up (see *Fig. 7b*) in which lightly doped polysilicon forms the resistor. Resistor values as high as hundreds of megaohms can be fabricated with this technique, thereby substantially reducing array current. But the problem with polysilicon resistors is high sensitivity to noise, soft errors, and pull-down leakage. The biggest problem, however, is that the sensitivities are "soft" by nature. That is, they are all but impossible to identify in a production test environment.

CMOS offers another possibility—the p-type load (see *Fig. 7c*). A p-device is much stronger than either a resistor or weak-depletion pull-up. A strong p-device virtually eliminates soft sensitivities and draws no standby power. The resulting overall standby power is reduced to just a fraction of an equivalent NMOS chip's power. □

EPROMs (Erasable Programmable Read Only Memories)

4

EPROMs
(Erasable Programmable Read
Only Memories)

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- **Industry Standard Pinout ... JEDEC Approved 24 Pin Ceramic Package**
  (See Packaging Spec. Order #231369)

The Intel 2732A is a 5V-only, 32,768-bit ultraviolet erasable (cerdip) Electrically Programmable Read-Only Memory (EPROM). The standard 2732A access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

An important 2732A feature is Output Enable ($\overline{OE}$) which is separate from the Chip Enable ($\overline{CE}$) control. The $\overline{OE}$ control eliminates bus contention in microprocessor systems. The $\overline{CE}$ is used by the 2732A to place it in a standby mode ($\overline{CE}$ = V_{IH}) which reduces power consumption without increasing access time. The standby mode reduces the current requirement by 65%; the maximum active current is reduced from 100 mA to a standby current of 35 mA.

*HMOS is a patented process of Intel Corporation.

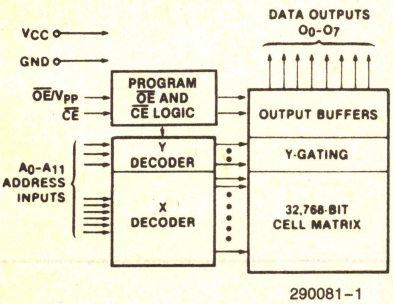
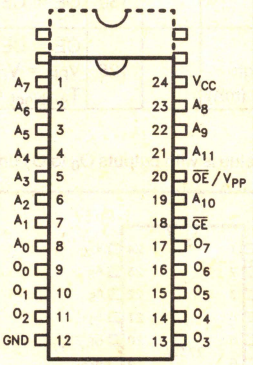


Figure 1. Block Diagram

Pin Names

A_0–A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
O_0–O_7	Outputs

27128 27128A	2764 2764A 27C64 87C64	2716
V_{PP}	V_{PP}	
A_{12}	A_{12}	
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND



2716	2764 2764A 27C64 87C64	27128 27128A
	V_{CC} $\overline{PGM}$	V_{CC} $\overline{PGM}$
V_{CC}	N.C.	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM configurations are shown in the blocks adjacent to the 2732A pins.

Figure 2. Cerdip Pin Configuration

October 1987
Order Number: 290081-003

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD2732A LD2732A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		45	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. Maximum current value is with outputs O_0 to O_7 unloaded.

EXPRESS EPROM PRODUCT FAMILY

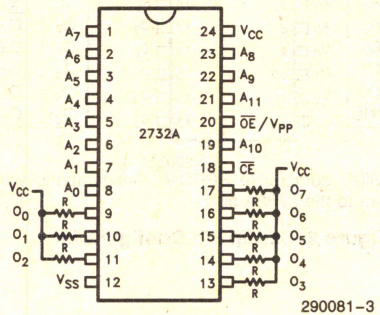
PRODUCT DEFINITONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

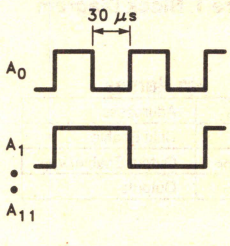
2732A Versions

Packaging Options	
Speed Versions	**Cerdip**
−2	Q
STD	Q, T, L
−3	Q
−4	Q, T, L
−20	Q
−25	Q, T, L
−30	Q
−45	Q, T, L



290081-3

$\overline{OE}/V_{PP} = +5V$, R = 1KΩ, $V_{CC} = +5V$
V_{SS} = GND, $\overline{CE}$ = GND



290081-4

Binary Sequence from A_0 to A_{11}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. During Read .....0°C to +70°C
Temperature Under Bias .....−10°C to +80°C
Storage Temperature .....−65°C to +125°C
All Input or Output Voltages with Respect to Ground.....−0.3V to +6V
Voltage on A9 with Respect to Ground.....−0.3V to +13.5V
V_{PP} Supply Voltage with Respect to Ground During Programming .....−0.3V to +22V
V_{CC} Supply Voltage with Respect to Ground .....−0.3V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(3)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{SB}(2)	V_{CC} Current (Standby)			35	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(2)	V_{CC} Current (Active)			100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

A.C. CHARACTERISTICS $0°C \le T_A \le 70°C$

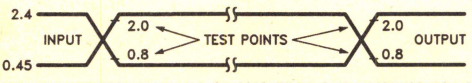
Versions	$V_{CC} \pm 5\%$	2732A-2		2732A		2732A-3		2732A-4		Units	Test Conditions
	$V_{CC} \pm 10\%$	2732A-20		2732A-25		2732A-30		2732A-45			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300		450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		70		100		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}/V_{PP}$ High to Output Float	0	60	0	60	0	130	0	130	ns	$\overline{CE} = V_{IL}$
t_{OH}(4)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE (2) $T_A = 25°C, f = 1\ MHz$

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	$V_{IN} = 0V$
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

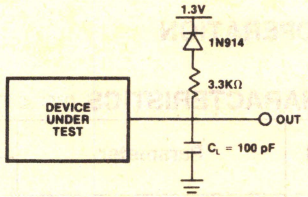
A.C. TESTING INPUT/OUTPUT WAVEFORM



290081-5

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

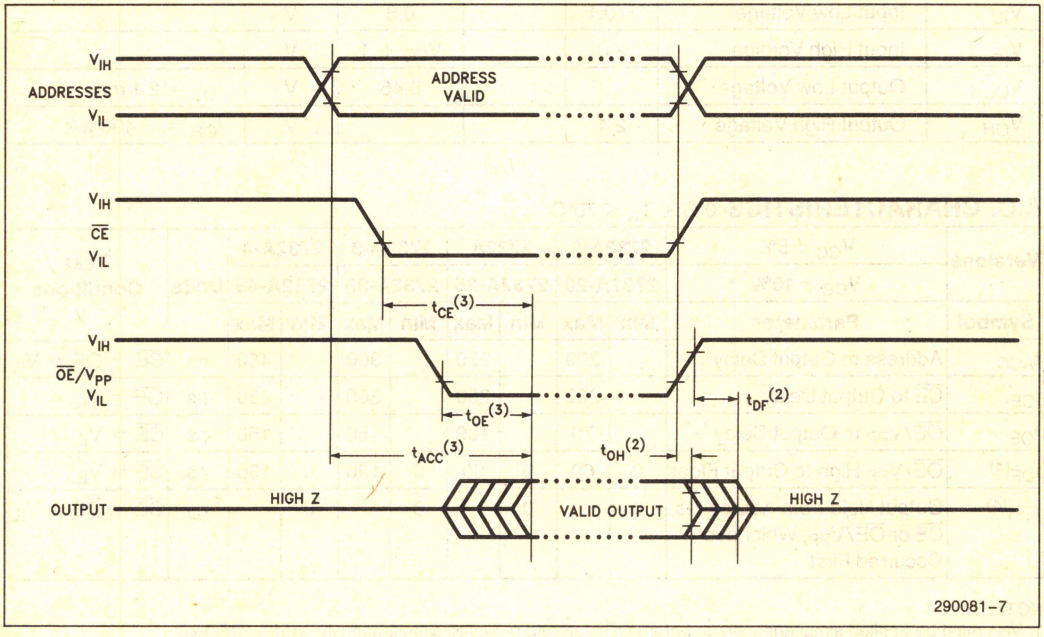
A.C. TESTING LOAD CIRCUIT



290081-6

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



290081-7

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested. Output float is defined as the point where data is no longer driven—see timing diagram.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{CE}.

DEVICE OPERATION

The modes of operation of the 2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming and 12V on A_9 for the int$_e$ligent Identifier™ mode. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	Outputs
Read/Program Verify	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
Program Inhibit	V_{IH}	V_{PP}	X	X	V_{CC}	High Z
Int$_e$ligent Identifier(3)						
—Manufacturer	V_{IL}	V_{IL}	V_H	V_{IL}	V_{CC}	89H
—Device	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	01H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. V_H = 12V ±0.5V.
3. A_1–A_8, A_{10}, A_{11} = V_{IL}.

Read Mode

The 2732A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum active current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided two control lines which accommodate this multiple memory connection. The two control lines allow for:

a) The lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's two-line control and by use of properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for

every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

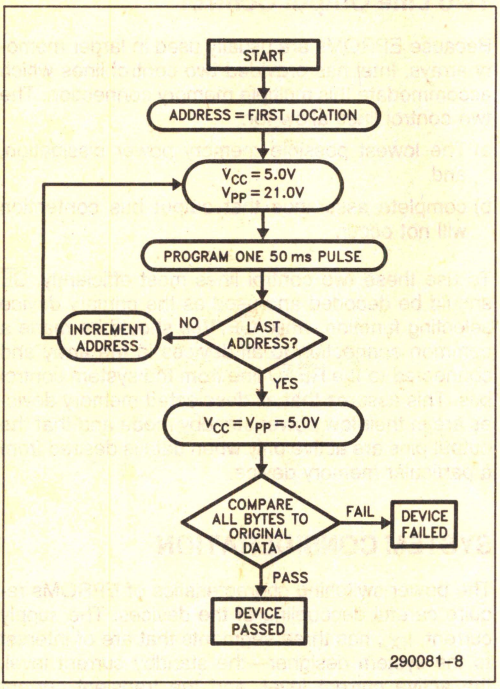


Figure 3. Standard Programming Flowchart

PROGRAMMING MODES

CAUTION: Exceeding 22V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure (cerdip EPROMs), all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" in cerdip EPROMs is by ultraviolet light erasure.

The device is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 20 ms (50 ms typical) active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed (see Figure 3). Any location can be programmed at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high level $\overline{CE}$ input inhibits the other EPROMs from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROMs may be common. A TTL low level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that selected device.

Program Verify

A verify (Read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Units	Test Conditions (Note 1)
		Min	Typ(3)	Max		
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage During Verify			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4			V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program and Verify)		85	100	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5		12.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

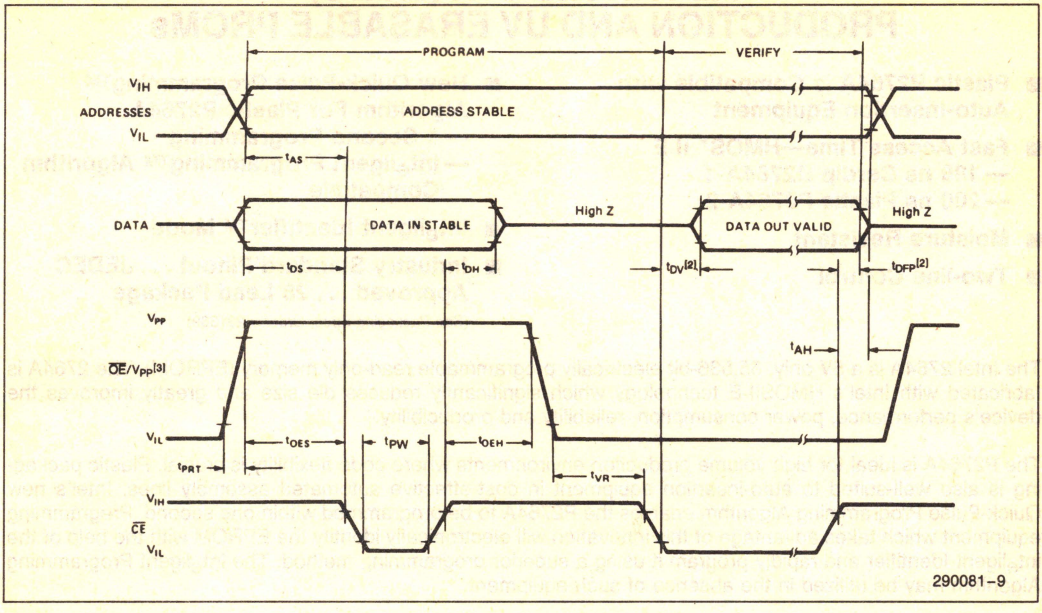
Symbol	Parameter	Limits			Units	Test Conditions* (Note 1)
		Min	Typ(3)	Max		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}/V_{PP}$ High to Output Not Driven	0		130	ns	(Note 2)
t_{PW}	$\overline{CE}$ Pulse Width During Programming	20	50	55	ms	
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			μs	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{IL}$
t_{VR}	V_{PP} Recovery Time	2			μs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

*A.C. TEST CONDITIONS

Input Rise and Fall Time (10% to 90%) ..... ≤20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 2732A, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which can damage the device.

2764A
ADVANCED 64K (8K x 8)
PRODUCTION AND UV ERASABLE PROMs

- **Plastic P2764A is Compatible with Auto-Insertion Equipment**
- **Fast Access Time—HMOS* II E**
  - **— 180 ns Cerdip D2764A-1**
  - **— 200 ns Plastic P2764A-2**
- **Moisture Resistant**
- **Two-line Control**
- **New Quick-Pulse Programming™ Algorithm For Plastic P2764A**
  - **— 1 Second Programming**
  - **— int$_e$ligent Programming™ Algorithm Compatible**
- **int$_e$ligent Identifier™ Mode**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Package**

(See Packaging Spec, Order #231369)

The Intel 2764A is a 5V only, 65,536-bit electrically programmable read-only memory (EPROM). The 2764A is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, power consumption, reliability and producibility.

The P2764A is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P2764A to be programmed within one second. Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

The 2764A provides access times to 180 ns (2764A-1). This is compatible with high-performance microprocessors, such as Intel's 8 MHz iAPX 186 allowing full speed operation without the addition of WAIT states. The 2764A is also directly compatible with the 12 MHz 8051 family.

Two-line control and JEDEC-approved, 28 pin packaging are standard features of Intel higher density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between non-volatile memory alternatives.

*HMOS is a patented process of Intel Corporation.

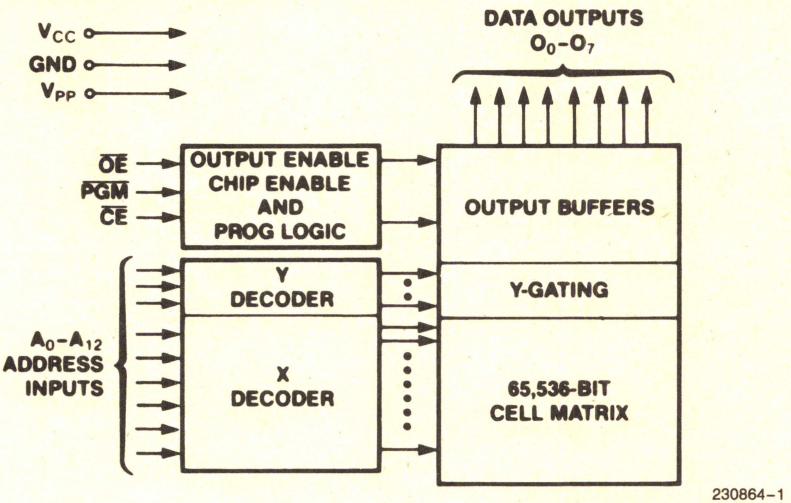


Figure 1. Block Diagram

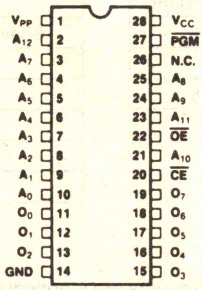
October 1987
Order Number: 230864-005

Pin Names

A_0–A_{12}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
N.C.	No Connect
D.U.	Don't Use

27916	27513	27512	27256	27128A	2732A	2716
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0	A_0
O_0	I/O_0	O_0	O_0	O_0	O_0	O_0
O_1	I/O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd

2764A
P2764A



230864-2

2716	2732A	27128A	27256	27512	27513	27916
		V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{14}	A_{14}	$\overline{WE}$	$\overline{PGM}/\overline{WE}$
V_{CC}	V_{CC}	A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the 2764A pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

2764A VERSIONS

Speed Versions	Packaging Options	
	Cerdip	Plastic
−2	Q	
STD	Q, T, L	T
−3	Q, T, L	T
−25	Q, T, L	T
−30	Q, T, L	

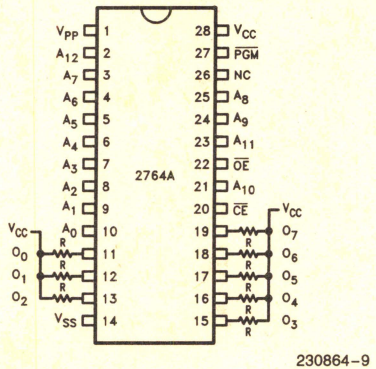
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

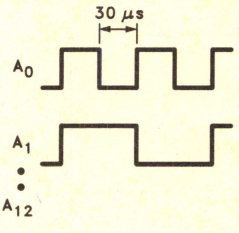
Symbol	Parameter	TD2764A LD2764A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		40	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1} (1)	V_{CC} Active Current (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		75	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



230864-9

$\overline{OE}$ = +5V R = 1 KΩ V_{CC} = +5V
V_{PP} = +5V V_{SS} = GND $\overline{CE}$ = GND
PGM = +5V



230864-10

Binary Sequence from A_0 to A_{12}

Burn-in Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Inputs or Output Voltages with
Respect to Ground ..... −0.6V to +6.25V
Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V
V_{PP} Supply Voltage with
Respect to Ground
During Programming ..... −0.6V to +14.0V

V_{CC} Supply Voltage with Respect
to Ground ..... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Conditions
		Min	Max	Unit	
I_{LI}	Input Load Current		10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = 5.5V$
I_{PP}(2)	V_{PP} Current Read		5	mA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby		35	mA	$\overline{CE} = V_{IH}$
I_{CC}(2)	V_{CC} Current Active		75	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
V_{PP}(2)	V_{PP} Read Voltage	3.8	V_{CC}	V	$V_{CC} = 5.0V \pm 0.25V$

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

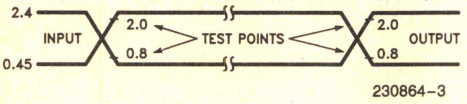
Versions(4)	$V_{CC} \pm 5\%$	2764A-1		2764A-2 P2764A-2		2764A P2764A		2764A-3 P2764A-3		2764A-4		Unit	Test Conditions
	$V_{CC} \pm 10\%$			2764A-20		2764A-25 P2764A-25		2764A-30 P2764A-30		2764A-45			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		180		200		250		300		450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		180		200		250		300		450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		65		75		100		120		150	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	55	0	55	0	60	0	105	0	130	ns	$\overline{CE} = V_{IL}$
t_{OH}(3)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
4. Model Number Prefixes: No prefix = CERDIP; P = Plastic DIP.

CAPACITANCE[2] (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ [1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

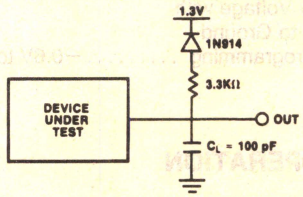
A.C. TESTING INPUT/OUTPUT WAVEFORM



230864-3

A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

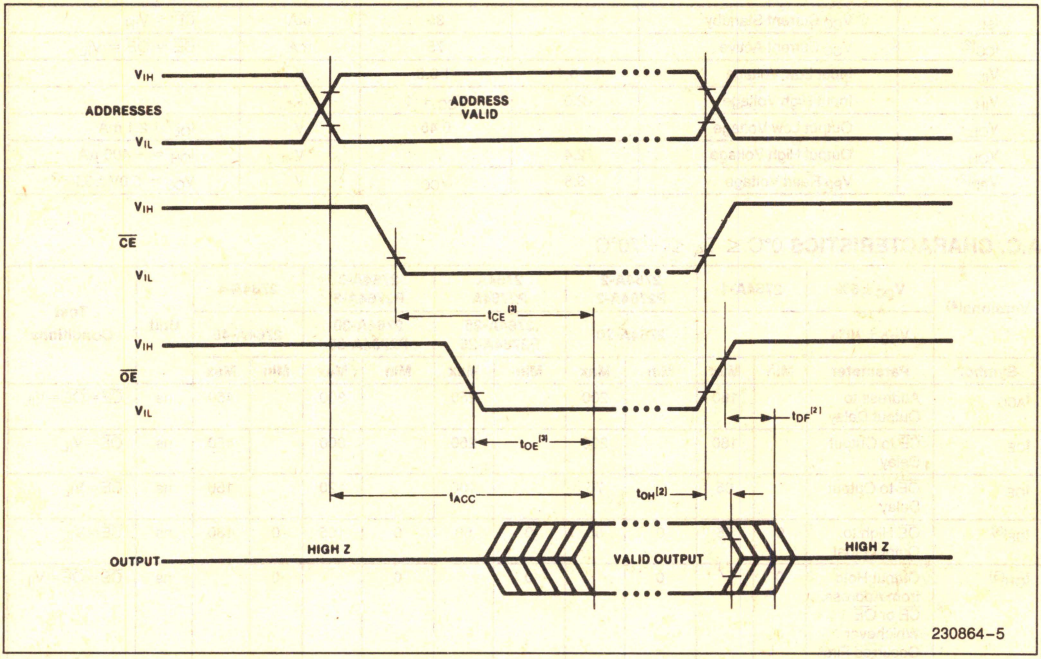
A.C. TESTING LOAD CIRCUIT



230864-4

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



230864-5

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 2764A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent identifier mode.

Table 1. Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	High Z
int$_e$ligent Identifier(3) —manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	5.0V	89H(5) 88H(5)
—device	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	5.0V	08H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. $V_H = 12.0V \pm 0.5V$.
3. A_1–A_8, A_{10}–$A_{12} = V_{IL}$.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturers identifier reads 89H for Cerdip EPROMs; 88H for Plastic EPROMs.

Read Mode

The 2764A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum current of the devices by applying a TTL-high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light exposure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (see Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at its programming voltage (see Table 2) will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device.

To activiate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1(A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The EPROM should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the EPROM to high intensity UV light for longer periods may cause permanent damage.

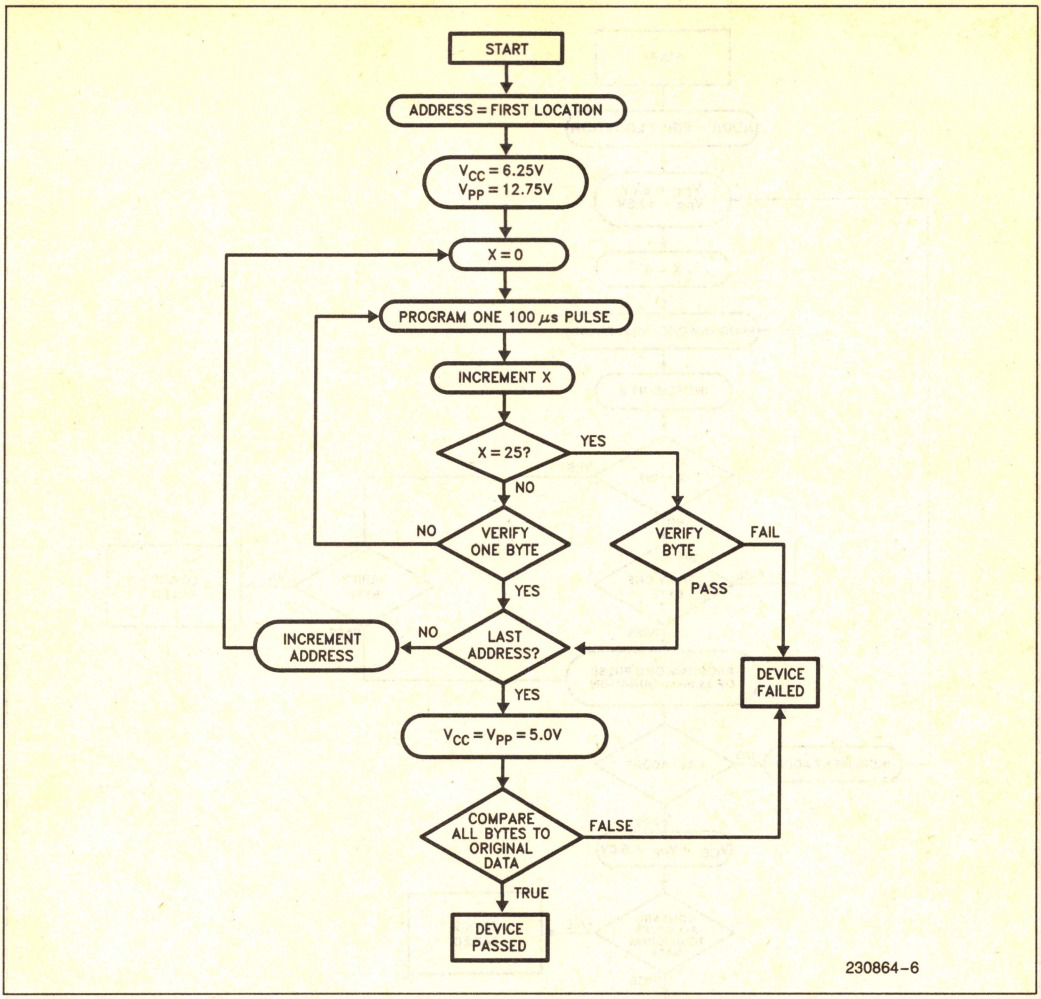


Figure 3. Quick-Pulse Programming™ Flowchart

Quick-Pulse Programming™ Algorithm (Plastic P2764A)

Intel's Plastic EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows Plastic P2764A devices to be programmed in under one second, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25–100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, Plastic and PLCC EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

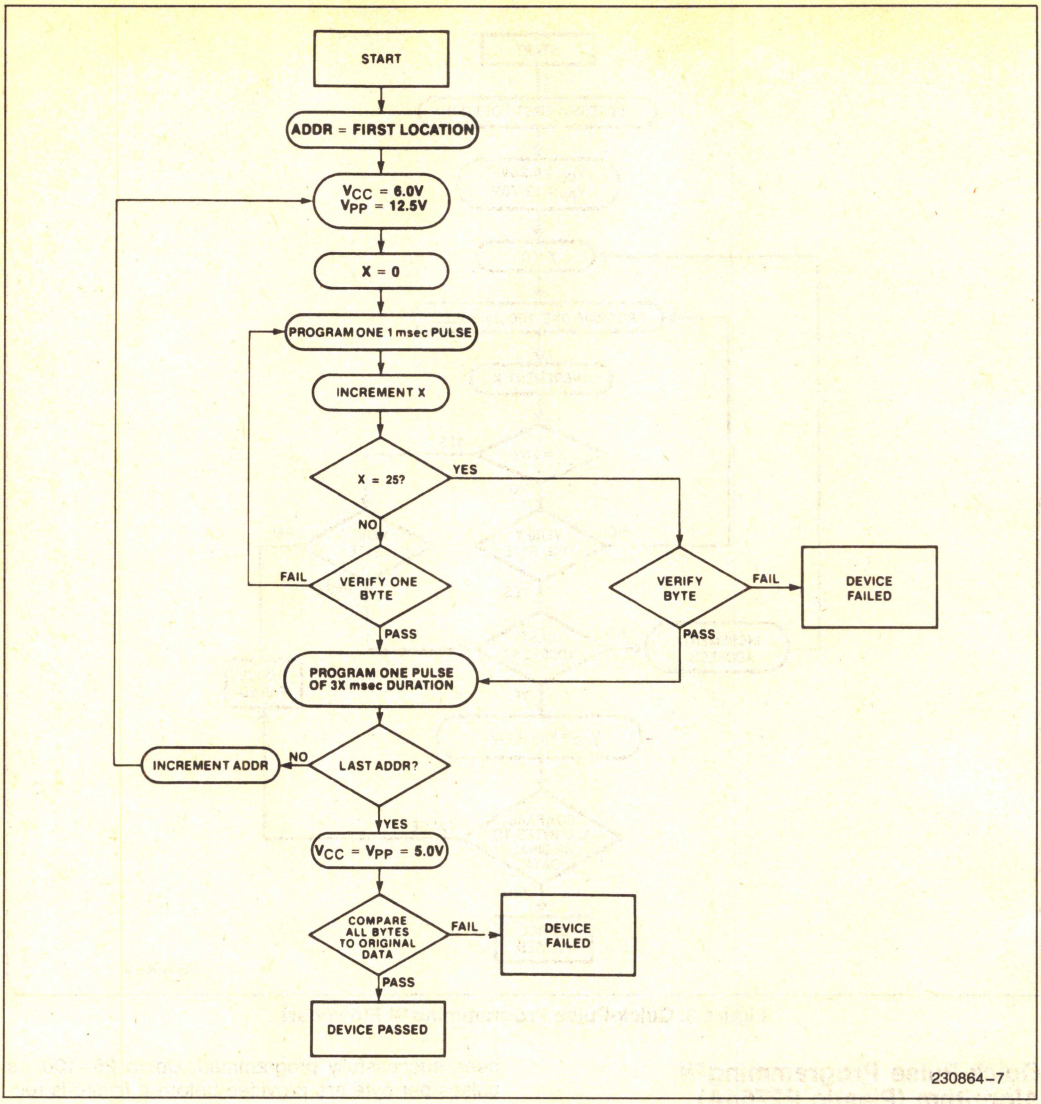


Figure 4. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm, a standard in the industry for the past few years, is required for all of Intel's 12.5V CERDIP EPROMs. Plastic EPROMs may also be programmed using this method. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 4.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

Table 2

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (see Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output HIgh Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		75	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A9 inteligent Identifier Voltage	11.5	12.5	V	
V_{PP}	inteligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	inteligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (see table 2 for V_{CC} and V_{PP} voltages)

Symbol	Parameter	Limits				Test Conditions* (see Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(See Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	inteligent Programming
		95	100	105	μs	Quick-Pulse Programming
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(see Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns

Input Pulse Levels ..... 0.45V to 2.4V

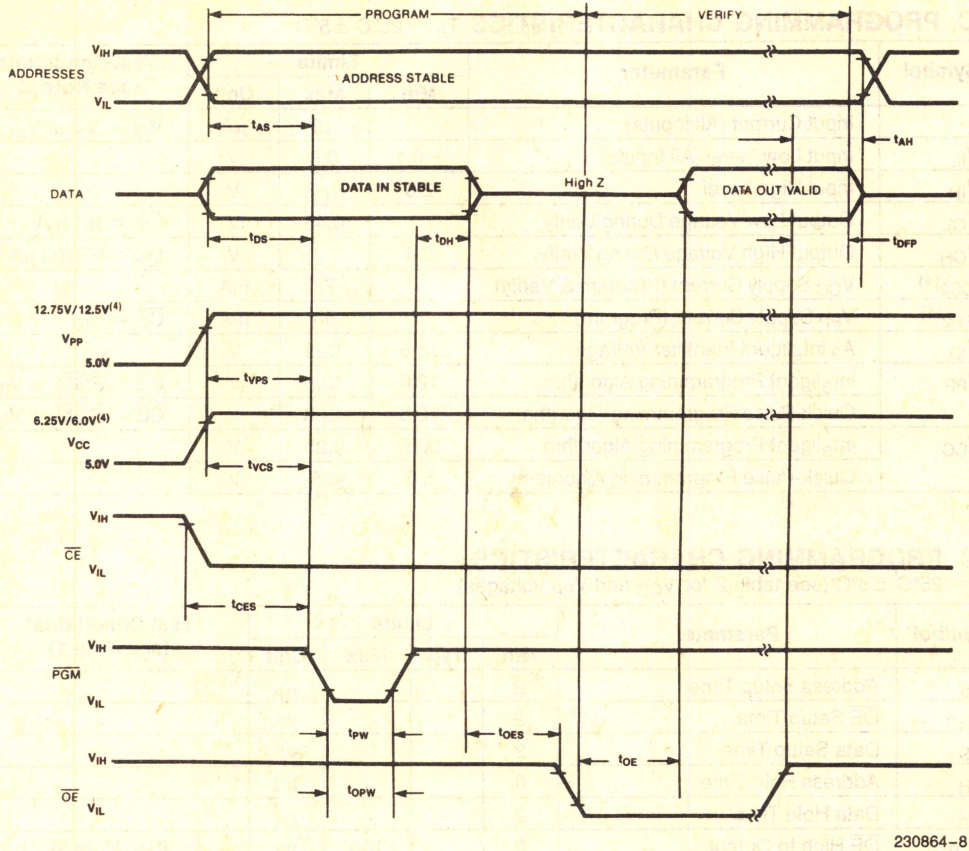
Input Timing Reference Level ..... 0.8V and 2.0V

Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X (inteligent Programming Algorithm only).
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with Outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 2764A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for Int$_e$ligent Programming Algorithm.

27C64/87C64
64K (8K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- **CHMOS Microcontroller and Microprocessor Compatible**
  - **87C64-Integrated Address Latch**
  - **Universal 28 Pin Memory Site, 2-line Control**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current**
- **Noise Immunity Features**
  - **$\pm$10% V_{CC} Tolerance**
  - **Maximum Latch-up Immunity Through EPI Processing**
- **High Performance Speeds**
  - **150 ns Maximum Access Time**
- **New Quick-Pulse Programming™ Algorithm (1 second programming)**
- **Available in 28-Pin Cerdip and Plastic DIP Package and 32-Lead PLCC Package.**

(See Packaging Spec, Order #231369)

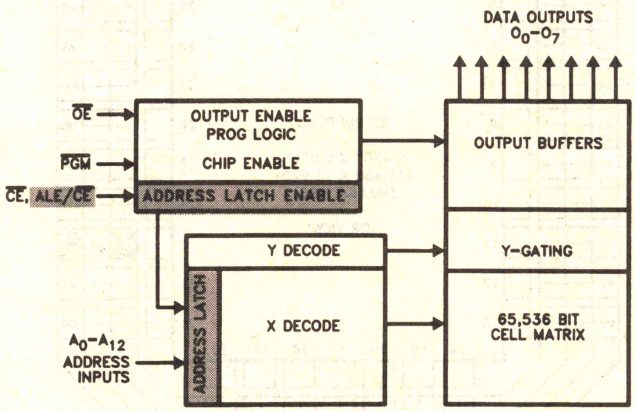
Intel's 27C64 and 87C64 CHMOS EPROMs are 64K bit 5V only memories organized as 8192 words of 8 bits. They employ advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 87C64 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C64 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 2764A (HMOS II-E).

The 27C64 and 87C64 are offered in both a ceramic DIP, Plastic DIP, and Plastic Leaded Chip Carrier (PLCC) Packages. Cerdip packages provide flexibility in prototyping and R&D environments, whereas Plastic DIP and PLCC EPROMs provide optimum cost effectiveness in production environments. A new Quick-Pulse Programming™ Algorithm is employed which can speed up programming by as much as one hundred times.

The 87C64 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can eliminate an external address latch by tieing address and data pins of the 87C64 directy to the processor's multiplexed address/data pins. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs (A_0–A_{12}) of the 87C64 is latched internally. The address inputs are then ignored as data information is passed on the same bus.

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from -1V to $V_{CC} + 1$V.

*HMOS and CHMOS are patented processes of Intel Corporation.



Shaded Areas represent the 87C64 version

290000-1

Figure 1. Block Diagram

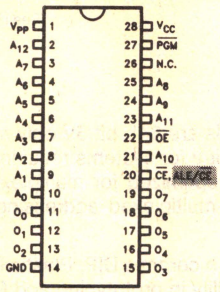
October 1987
Order Number: 290000-007

Pin Names

A_0-A_{12}	ADDRESSES
O_0-O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
ALE/$\overline{CE}$	ADDRESS LATCH ENABLE /CHIP ENABLE
$\overline{PGM}$	PROGRAM STROBE
N.C.	NO CONNECT
D.U.	DON'T USE

27256	27128	2732A	2716
V_{PP}	V_{PP}		
A_{12}	A_{12}		
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

27C64/87C64
P27C64/P87C64

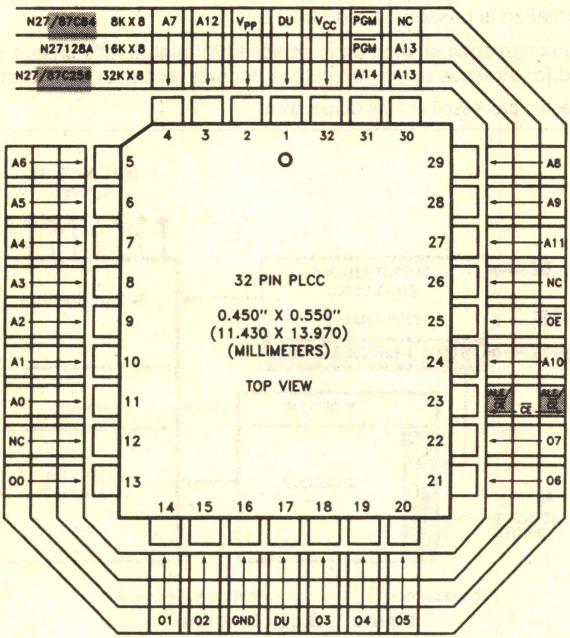


290000-2

2716	2732A	27128	27256
		V_{CC} / $\overline{PGM}$	V_{CC}
			A_{14}
V_{CC}	V_{CC}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site" Compatible EPROM Pin Configurations are shown in the adjacent blocks to 27C64 Pins.
Shaded Areas represent the 87C64 version

Figure 2. Pin Configuration



290000-11

Figure 3. PLCC(N) Lead Configuration

Extended Temperature (Express) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications.

EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available along with automotive temperature range (−40°C to +125°C) products. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM Product Family

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0 to +70	168 ±8
T	−40 to +85	NONE
L	−40 to +85	168 ±8
A	−40 to +125	NONE
B	−40 to +125	168 ±8

EXPRESS Options

27C64/87C64 Versions

Packaging Options			
Speed Versions	Cerdip	PLCC	Plastic DIP
−1	T, L, Q	T	T
−15	T, L, Q	T	T
−2	T, L, Q, A, B	T, A	T, A
−20	T, L, Q, A	T	T
−STD	T, L, Q, A, B	T, A	T, A
−25	T, L, Q, A	T	T
−3	T, L, Q, A, B	T, A	T, A
−30	T, L, Q, A	T	T

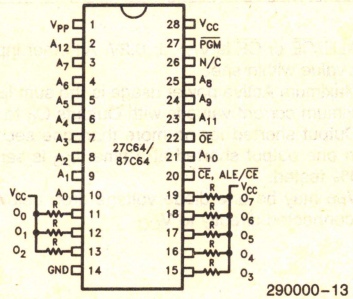
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

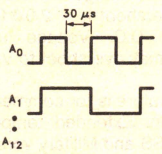
Symbol	Parameter		27C64 87C64 Min	27C64 87C64 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)	CMOS		0.1	$\overline{CE} = V_{CC}$, $\overline{OE} = V_{IL}$
		TTL		1.0	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)	TTL		20, 30	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature	TTL		20, 30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{ambient} = 85°C$

NOTE:
1. See notes 4 and 6 of Read Operation D.C. Characteristics.



290000-13

$\overline{OE}$ = +5V R = 1 KΩ V_{CC} = +5V
V_{PP} = +5V GND = 0V $\overline{CE}$ = 33.3 KHz
$\overline{PGM}$ = +5V



290000-14

Binary Sequence from A_0 to A_{12}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C(2)

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +150°C

Voltage on Any Pin with
Respect to Ground ..... −2.0V to 7V(1)

Voltage on Pin A_9 with
Respect to Ground ..... −2.0V to +13.5V(1)

V_{PP} Supply Voltage with Respect to Ground
During Programming ..... −2.0V to +14V(1)

V_{CC} Supply Voltage with
Respect to Ground ..... −2.0V to +7.0V(1)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter		Notes	Min	Typ(3)	Max	Unit	Test Condition
I_{LI}	Input Leakage Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{PP_1}	V_{PP} Current Read		6			100	µA	$V_{PP} = V_{CC}$
I_{SB}	V_{CC} Current Standby with Inputs—	CMOS	5			100	µA	$\overline{CE} = V_{CC}$
		TTL	4			1.0	mA	$\overline{CE} = V_{IH}$
I_{CC_1}	V_{CC} Current Active		4, 6			20, 30	mA	$\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage(±10% Supply) (TTL)			2.0		$V_{CC}+0.5$	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			$V_{CC}-0.2$		$V_{CC}+0.2$		
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			3.5			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		7			100	mA	
V_{PP}	V_{PP} Read Voltage		8	$V_{CC}-0.7$		V_{CC}	V	

NOTES:

1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. Voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. 20 mA for STD and −3 versions; 30 mA for −2 and 150 ns versions.
   V_{IL}, V_{IH} levels at TTL inputs.
5. ALE/$\overline{CE}$ or $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with Outputs O_0 to O_7 unloaded.
7. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
8. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.

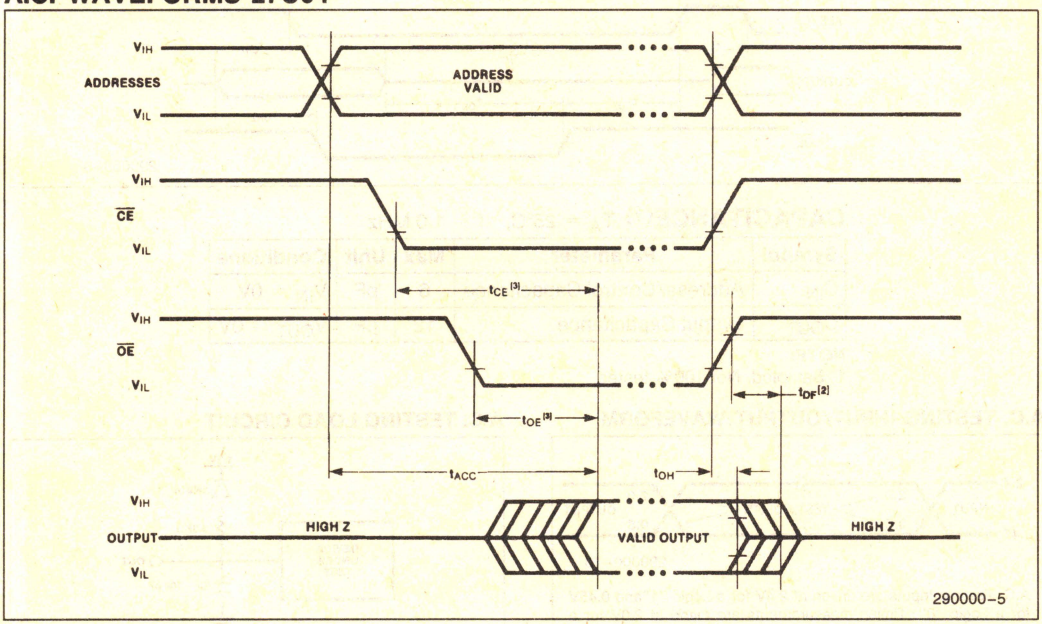
READ OPERATION

A.C. CHARACTERISTICS 27C64[1] $0°C \leq T_A \leq +70°C$

Versions (3)		$V_{CC} \pm 5\%$		27C64-1 N27C64-1 P27C64-1		27C64-2 N27C64-2 P27C64-2		27C64 N27C64		27C64-3 N27C64-3		Unit
		$V_{CC} \pm 10\%$		27C64-15 N27C64-15 P27C64-15		27C64-20 N27C64-20 P27C64-20		27C64-25 N27C64-25		27C64-30 N27C64-30		
Symbol	**Characteristic**			**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay				150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay				150		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay				75		75		100		120	ns
t_{DF}[2]	$\overline{OE}$ High to Output High Z				35		55		60		105	ns
t_{OH}[2]	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First			0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.
3. Model Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS 27C64



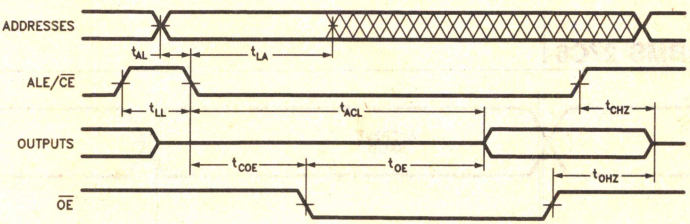
NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. CHARACTERISTICS 87C64(1) $0°C \le T_A \le +70°C$

Versions (3)		$V_{CC} \pm 5\%$		87C64-1 N87C64-1 P87C64-1		87C64-2 N87C64-2 P87C64-2		87C64 N87C64		87C64-3 N87C64-3		Unit
		$V_{CC} \pm 10\%$		87C64-15 N87C64-15 P87C64-15		87C64-20 N87C64-20 P87C64-20		87C64-25 N87C64-25		87C64-30 N87C64-30		
Symbol	**Parameter**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LL}	Chip Deselect Width		50		50		60		75		ns
t_{AL}	Address to $\overline{CE}$-Latch Set-up		7		20		25		30		ns
t_{LA}	Address Hold from $\overline{CE}$-LATCH		30		45		50		60		ns
t_{ACL}	CE-Latch Access Time			150		200		250		300	ns
t_{OE}	Output Enable to Output Valid			75		75		100		120	ns
t_{COE}	ALE/$\overline{CE}$ to Output Enable		30		45		50		60		ns
t_{CHZ}(2)	Chip Deselect to Output in High Z			45		50		60		75	ns
t_{OHZ}(2)	Output Disable to Output in High Z			35		50		60		75	ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.
3. Model Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS 87C64



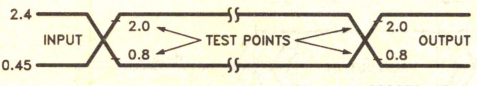
290000-6

CAPACITANCE(1) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	pF	$V_{OUT} = 0V$

NOTE:
1. Sampled. Not 100% tested.

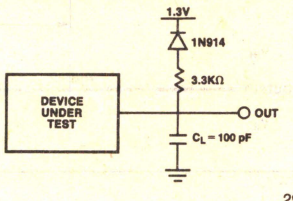
A.C. TESTING INPUT/OUTPUT WAVEFORM



290000-10

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



290000-3

$C_L = 100$ pF
C_L Includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the 27C64/87C64 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for inteligent Identifier mode.

Table 1. Mode Selection for 27C64 and 87C64

Mode \ Pins	ALE/$\overline{CE}$ / $\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (7)	A_9	A_0	V_{PP} (7)	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	HIGH Z
inteligent Identifier(3) -Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H (6) 88 H (6)
inteligent Identifier(3) -27C64	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	07 H
inteligent Identifier(3, 5) -87C64	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	37 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $V_H = 12.0V \pm 0.5V$.
3. A_1–A_8, $A_{10-12} = V_{IL}$.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. ALE/$\overline{CE}$ has to be toggled in order to latch in the addresses and read the signature codes.
6. The Manufacturer's identifier reads 89H for Cerdip devices; 88H for Plastic DIP and PLCC devices.
7. In Read Mode tie $\overline{PGM}$ and V_{PP} to V_{CC}.

Read Mode: 27C64

The 27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

Read Mode: 87C64

The 87C64 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C64 is designed as shown in Figure 4. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C64. All address inputs of the 87C64 are latched when ALE/$\overline{CE}$ is brought low, thus eliminating the need for a separate address latch.

The 87C64 internal address latch is directly enabled through the use of the ALE/$\overline{CE}$ line. As the transition occurs on the ALE/$\overline{CE}$ from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM by the $\overline{OE}$ pin.

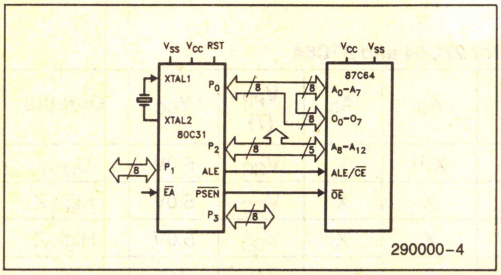


Figure 4. 80C31 with 87C64 System Configuration

Standby Mode

The 27C64 and 87C64 have Standby modes which reduce the maximum V_{CC} current to 100 μA. Both are placed in the Standby mode when $\overline{CE}$ or ALE/$\overline{CE}$ are in the CMOS-high state. When in the Standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (or ALE/$\overline{CE}$) should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient and inductive current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ (or ALE/$\overline{CE}$) and $\overline{PGM}$ are both at TTL low and $\overline{OE}$ = V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ (or ALE/$\overline{CE}$) or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$ (or ALE/$\overline{CE}$), all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ (or ALE/$\overline{CE}$) = V_{IL} will program the selected device.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ (or ALE/$\overline{CE}$) at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{CC} and V_{PP} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{OE}$.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1. ALE/$\overline{CE}$ of the 87C64 has to be toggled in order to latch in the addresses and read the Signature Codes.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from −1V to V_{CC} + 1V.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

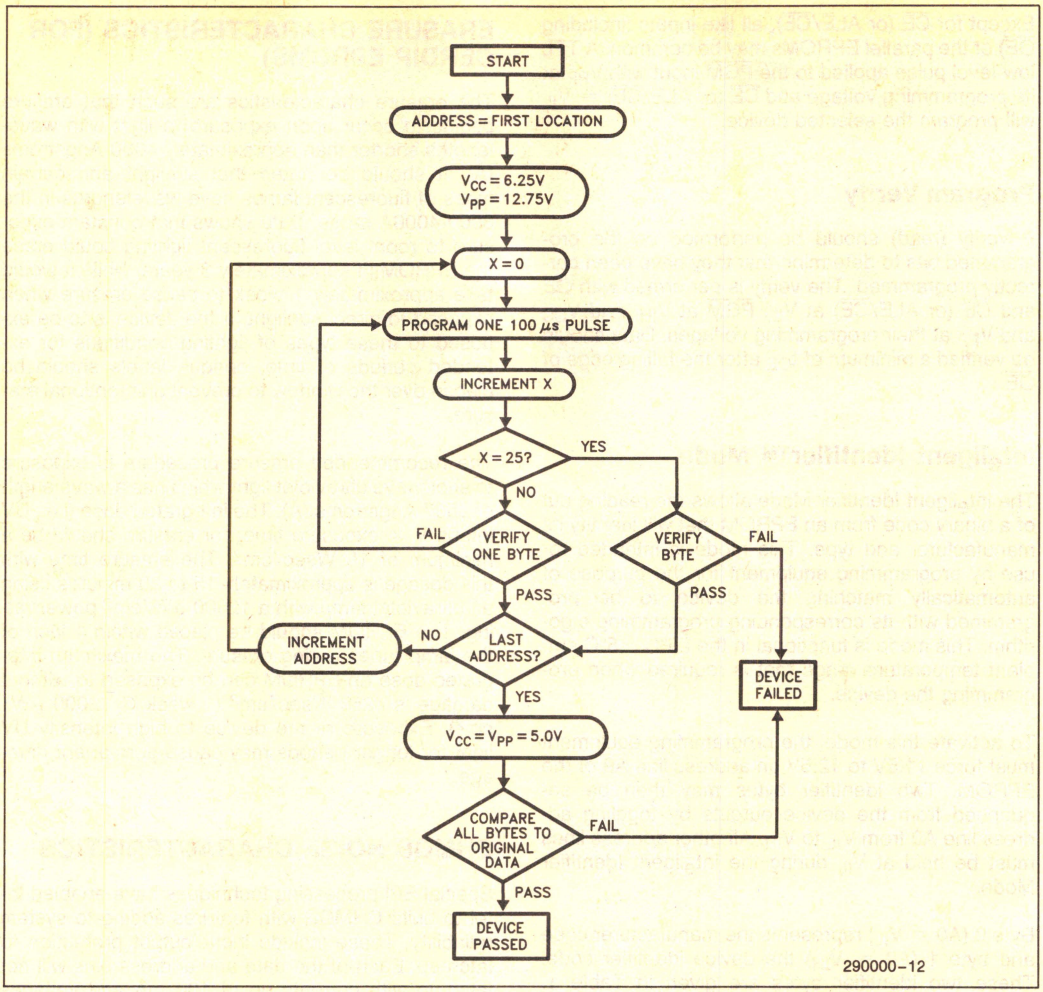


Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27C64 and 87C64 EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production environment. This algorithm allows these devices to be programmed in under one second, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS (27C64/87C64) $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	µA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5$ mA
I_{CC2}(3)	V_{CC} Supply Current		30	mA	
I_{PP2}(3)	V_{PP} Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Programming Voltage	12.5	13.0	V	
V_{CC}	Supply Voltage During Programming	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS 27C64

$T_A = 25°C \pm 5°C$, See Table 2 for V_{CC} and V_{PP} Voltages

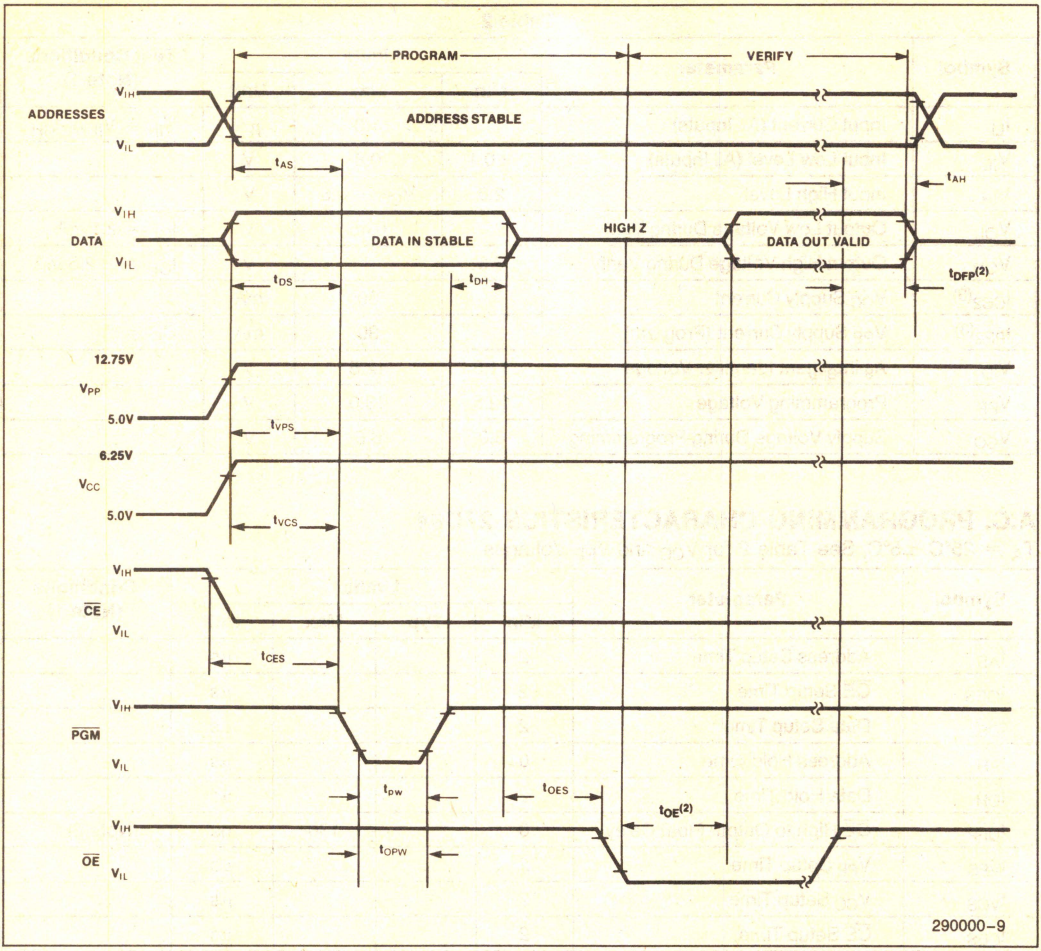
Symbol	Parameter	Limits				Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{CES}	$\overline{CE}$ Setup Time	2			µs	
t_{PW}	$\overline{PGM}$ Program Pulse Width	95	100	105	µs	Quick-Pulse
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 3.5V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0 to O_7 Unloaded.

PROGRAMMING WAVEFORMS 27C64



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C64, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

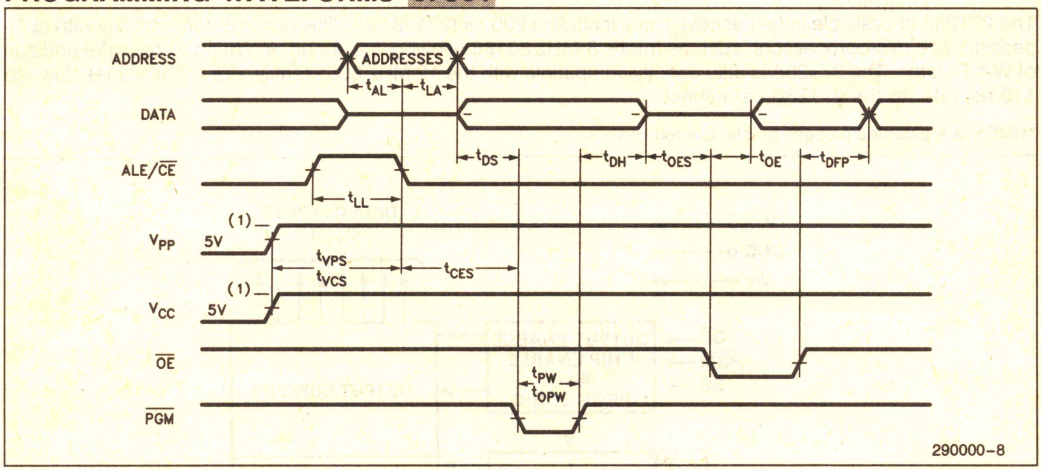
A.C. PROGRAMMING CHARACTERISTICS 87C64

T_A = 25°C ±5°C, See Table 2 for V_{CC} and V_{PP} Voltages.

Symbol	Parameter	Limits			Unit	Conditions
		Min	Typ	Max		
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{LL}	Chip Deselect Width	2			µs	
t_{AL}	Address to Chip Select Setup	1			µs	
t_{LA}	Address Hold from Chip Select	1			µs	
t_{PW}	$\overline{PGM}$ Pulse Width	95	100	105	µs	Quick-Pulse
t_{DS}	Data Setup Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Data Float	0		130	ns	
t_{OES}	Output Enable Setup Time	2			µs	
t_{OE}	Data Valid from Output Enable			150	ns	
t_{DH}	Data Hold Time	2			µs	
t_{CES}	$\overline{CE}$ Setup Time	2			µs	

NOTE:
1. Programming tolerances and test conditions are the same as 27C64.

PROGRAMMING WAVEFORMS 87C64



NOTE:
1. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm.

27128A
ADVANCED 128K (16K x 8) PRODUCTION AND UV ERASABLE PROMs

- **Fast 200 nsec Access Time**
  - **— HMOS* II-E Technology**
- **Low Power**
  - **— 100 mA Maximum Active**
  - **— 40 mA Maximum Standby**
- **int$_e$ligent Identifier™ Mode**
  - **— Automated Programming Operations**
- **Compatible with 2764A, 27128, 27256**
- **New Quick-Pulse Programming™ Algorithm**
  - **— Used on Plastic DIP**
  - **— int$_e$ligent Programming™ Algorithm Compatible**
- **±10% V_{CC} Tolerance Available**
- **Available in 28-Pin Cerdip and Plastic Packages**
  (See Packaging Spec, Order #231369)

The Intel 27128A is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 27128A is an advanced high speed version of the 27128 and is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, reliability and manufacturability.

The 27128A is currently available in two different package types. CERDIP packages provide flexibility in prototyping and R&D environments where reprogrammability is required. Plastic DIP EPROMs provide optimum cost effectiveness in production environments.

Intel's new Quick-Pulse Programming Algorithm enables these Plastic EPROMs to be programmed within two seconds. Programming equipment that takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment and is used to program CERDIP devices.

The 27128A is available in fast access times including 200 ns (27128A-2). This ensures compatibility with high-performance microprocessors, such as Intel's 8 MHz 80186 allowing full speed operation without the addition of WAIT states. The 27128A is also directly compatible with the 12 MHz 8051 family. For access times down to 110 ns, refer to the 27128B data sheet.

*HMOS is a patented process of Intel Corporation.

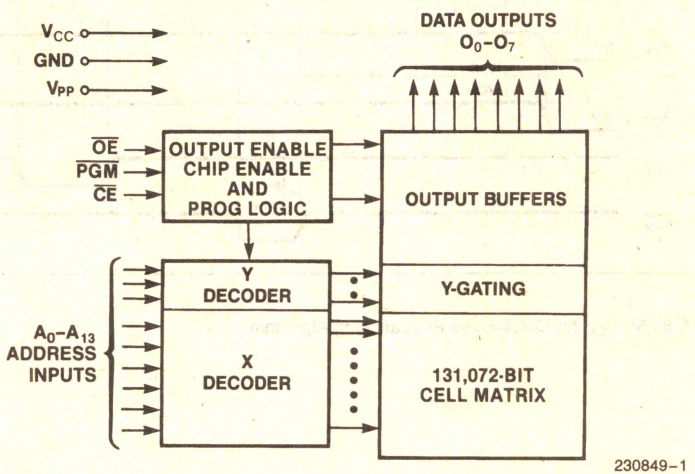


Figure 1. Block Diagram

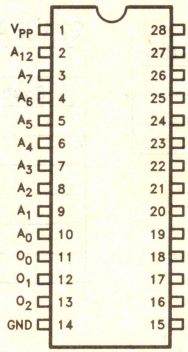
October 1987
Order Number: 230849-007

Pin Names

A_0–A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT
D.U.	DON'T USE
$\overline{WE}$	WRITE ENABLE

27916	27513	27512	27256 87C256 27C256	2764 2764A 27C64 87C64	2732 2732A	2716
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0	A_0
O_0	D_0/O_0	O_0	O_0	O_0	O_0	O_0
O_1	D_1/O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND	GND	GND

27128A
P27128A



230849-2

2716	2732 2732A	2764 2764A 27C64 87C64	27256 87C256 27C256	27512	27513	27916
		V_{CC} $\overline{PGM}$	V_{CC} A_{14}	V_{CC} A_{14}	V_{CC} $\overline{WE}$	V_{CC} $\overline{PGM/WE}$
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3	O_3

NOTE: Intel "Universal Site"—Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27128A Pins

Figure 2. Cerdip(D)/Plastic(P) DIP Pin Configurations

EXTENDED TEMPERATURE (EXPRESS) EPROMS

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27128A Versions

Packaging Options		
Speed Versions	**Cerdip**	**Plastic**
-2	T, L, Q	
-20	T, L, Q	
-STD	T, L, Q	
-25	T, L, Q	
-3	T, L, Q	
-30	Q	

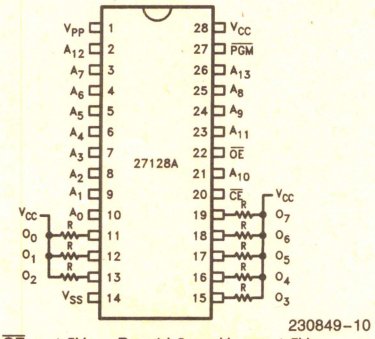
READ OPERATION

D.C. CHARACTERISTICS

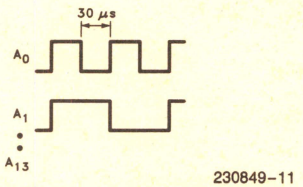
Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27128A, LD27128A		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		100	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with Outputs O_0 to O_7 unloaded.



$\overline{OE}$ = +5V R = 1 kΩ V_{CC} = +5V
V_{PP} = +5V V_{SS} = GND $\overline{CE}$ = GND



Binary Sequence from A_0 to A_{13}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with Respect to Ground ..... −0.6V to +6.25V

Voltage on A_9 with Respect to Ground ..... −0.6V to +13.5V

V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits				Conditions
		Min	Typ(3)	Max	Units	
I_{LI}	Input Load Current			10	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.5V$
I_{PP1}(2)	V_{PP} Current Read			5	mA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby			40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(2)	V_{CC} Current Active			100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	V	$V_{CC} = 5.0V \pm 0.25$

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions(5)	$V_{CC} \pm 5\%$	27128A-2 P27128A-2		27128A P27128A		27128A-3 P27128A-3		Unit
	$V_{CC} \pm 10\%$	27128A-20		27128A-25 P27128A-25		27128A-30 P27128A-30		
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		75		100		100	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	55	0	60	0	60	ns
t_{OH}(4)	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns

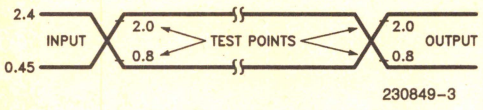
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
5. Packaging options: No prefix = Cerdip; Plastic DIP = P.

CAPACITANCE[2] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

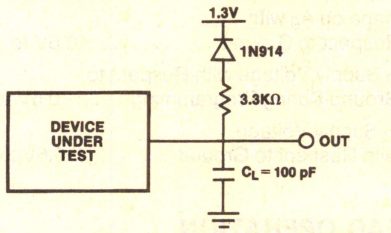
A.C. TESTING INPUT/OUTPUT WAVEFORM



230849-3

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

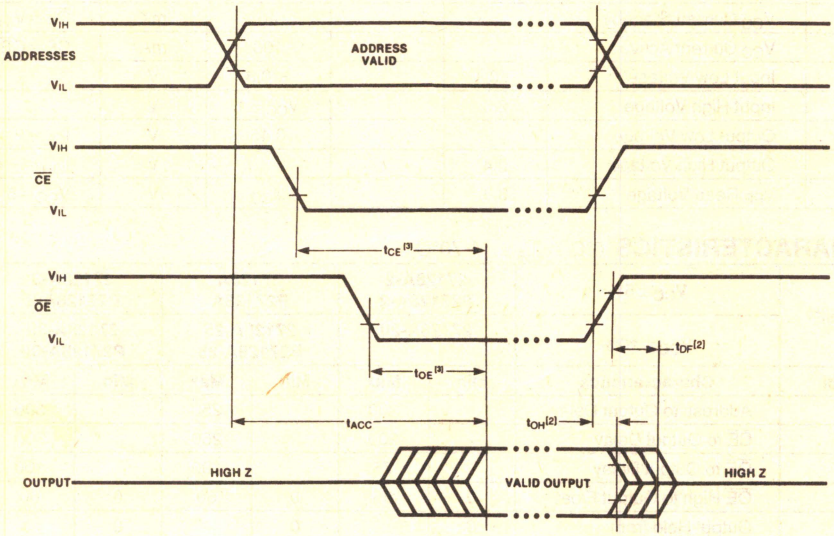
A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

230849-4

A.C. WAVEFORMS



230849-5

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27128A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Modes Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby		V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent	Manufacturer(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	5.0V	89 H(5) 88 H(5)
Identifier	Device(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	5.0V	89 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1–A_8, A_{10}–$A_{12} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturer's Identifier reads 89H for Cerdip EPROMs: 88H for Plastic EPROMs.

Read Mode

The 27128A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week @ 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

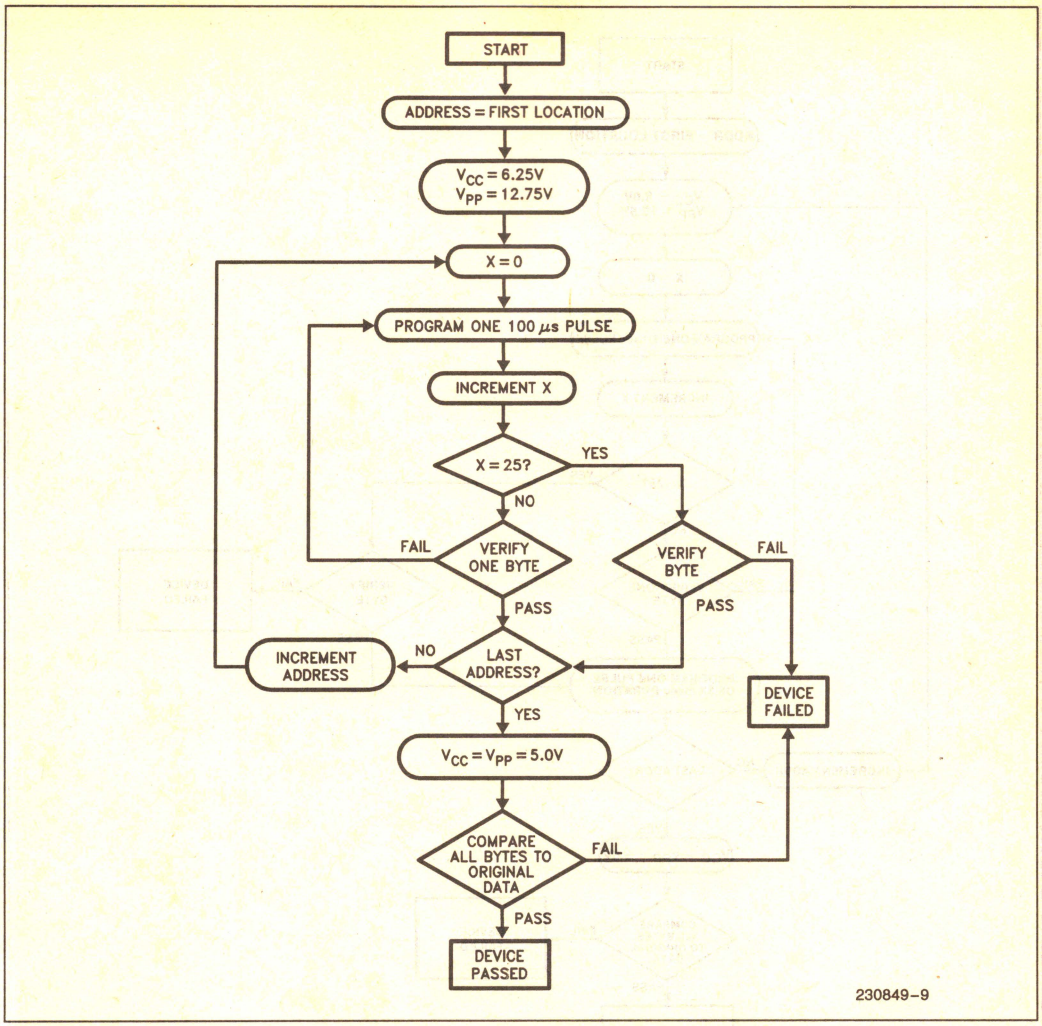


Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (For Plastic EPROMs)

Intel's Plastic EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows Plastic devices to be programmed in under two seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, Plastic EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

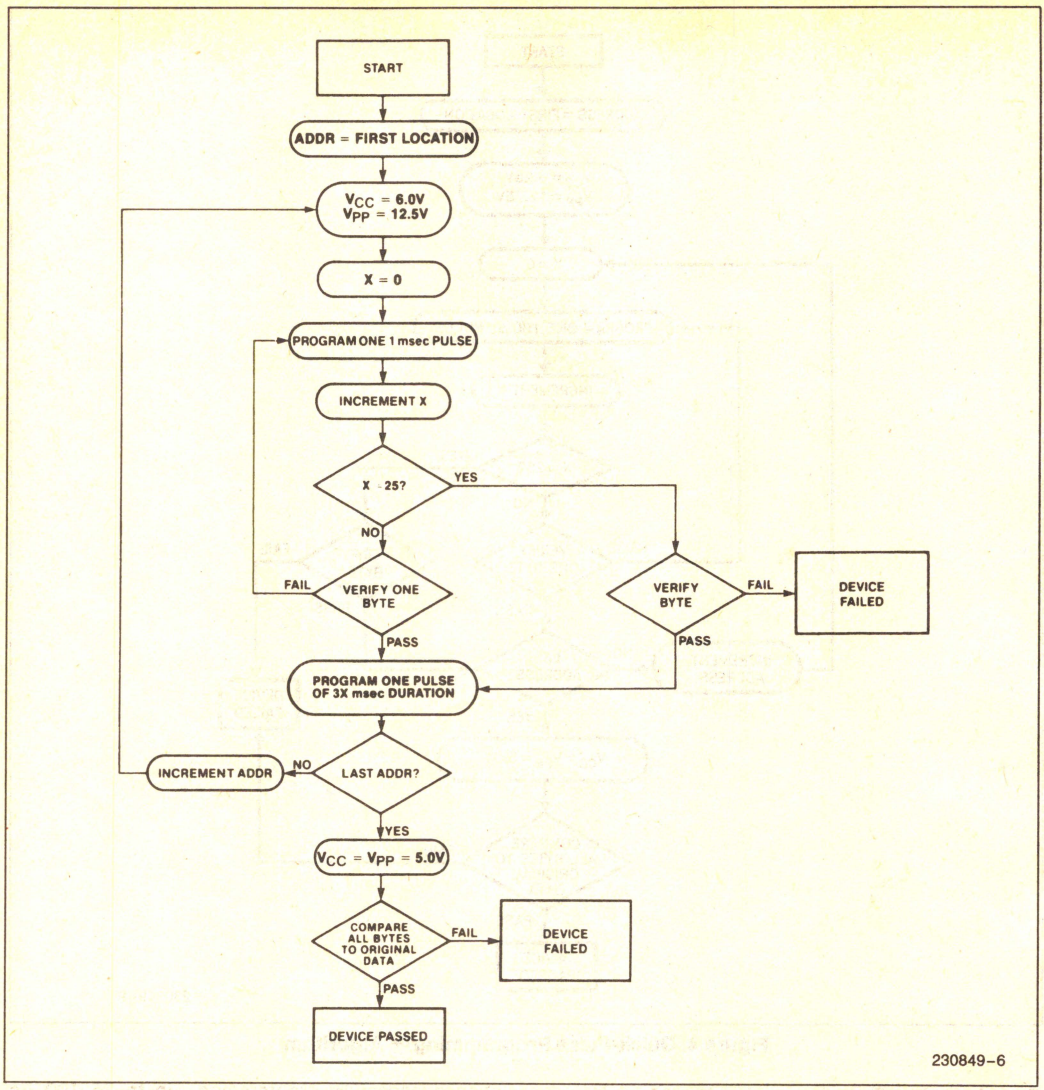


Figure 5. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm, a standard in the industry for the past few years, is required for all of Intels 12.5V V_{PP} Cerdip EPROMs. Plastic EPROMs may also be programmed using this method. A flow-chart of the int$_e$ligent Programming Algorithm is shown in Figure 5.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	intelligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	intelligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

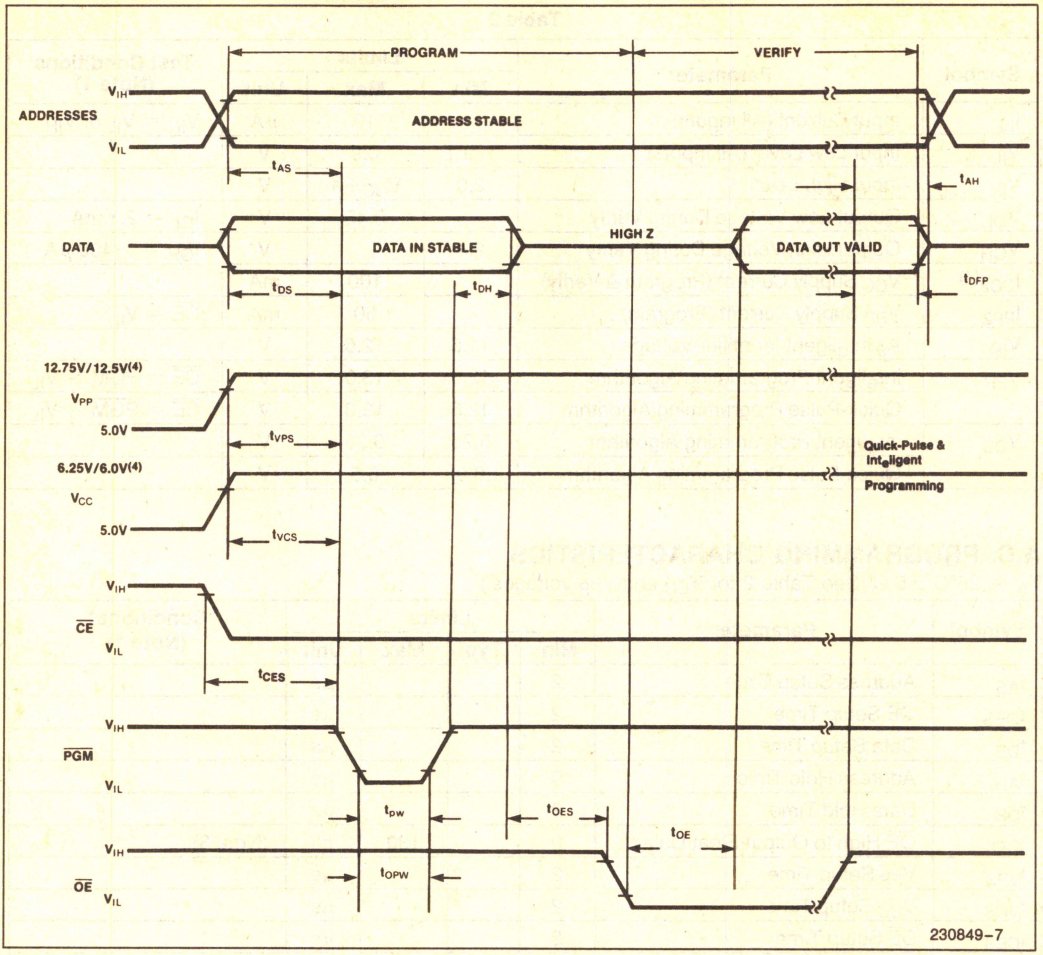
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	intelligent Programming
		95	100	105	μs	Quick-Pulse Programming
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (intelligent Programming Algorithm only) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27128A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

27128B
ADVANCED 128K (16K x 8) UV ERASABLE PROM

- **Fast 110 nsec Access Time**
  — HMOS* II-E Technology
- **Low Power**
  — 100 mA Maximum Active
  — 40 mA Maximum Standby
- **int$_e$ligent Identifier™ Mode**
  — Automated Programming Operations
- **Compatible with 2764A, 27128A, 27256**
- **int$_e$ligent Programming™ Algorithm**
  — Fast EPROM Programming
- **±10% V_{CC} Tolerance Available**
- **Available in 28-Pin Cerdip Package**
  (See Packaging Spec, Order #231369)

The Intel 27128B is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 27128B is an advanced high speed version of the 27128 and is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, reliability and manufacturability.

Several advanced features have been designed into the 27128B that allow fast and reliable programming—the int$_e$ligent Programming Algorithm and the int$_e$ligent Identifier Mode. Programming equipment that takes advantage of these innovations will electronically identify the 27128B and then rapidly program it using an efficient programming method.

The 27128B is available in fast access times including 110 ns (27128B-110V05), 135 ns (27128B-135V05), and 150 ns (27128B-150V10). This ensures compatibility with high-performance microprocessors, such as Intel's 10 MHz 80286 allowing full speed operation without the addition of WAIT states. The 27128B is also directly compatible with the 12 MHz 8051 family.

*HMOS is a patented process of Intel Corporation.

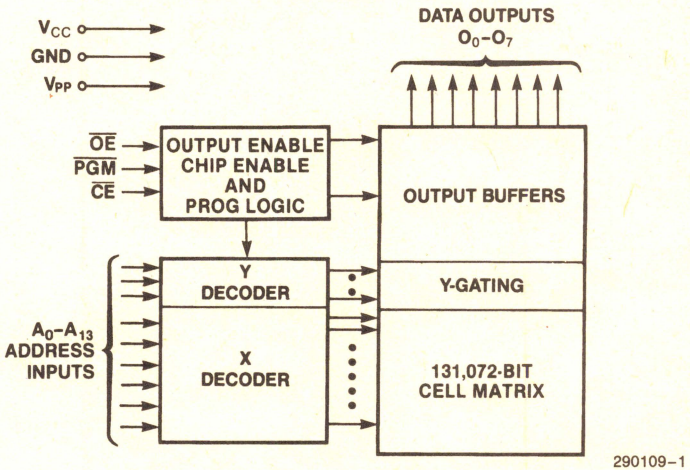


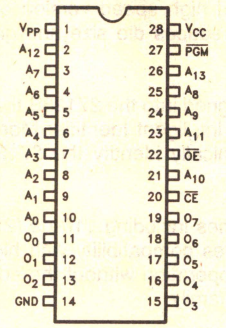
Figure 1. Block Diagram

February 1986
Order Number: 290109-001

Pin Names

A_0–A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT
D.U.	DON'T USE
$\overline{WE}$	WRITE ENABLE

27916	27513	27512	27256 87C256 27C256	2764 2764A 27C64 87C64	2732 2732A	2716
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0	A_0
O_0	D_0/O_0	O_0	O_0	O_0	O_0	O_0
O_1	D_1/O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND	GND	GND



290109-2

2716	2732 2732A	2764 2764A 27C64 87C64	27256 87C256 27C256	27512	27513	27916
		V_{CC} $\overline{PGM}$	V_{CC} A_{14}	V_{CC} A_{14}	V_{CC} $\overline{WE}$	V_{CC} $\overline{PGM}/\overline{WE}$
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3	O_3

NOTE: Intel "Universal Site"—Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27128B Pins

Figure 2. Cerdip(D) Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with Respect to Ground ..... −0.6V to +6.25V

Voltage on A_9 with Respect to Ground ..... −0.6V to +13.5V

V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits				Conditions
		Min	Typ(3)	Max	Units	
I_{LI}	Input Load Current			10	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.5V$
I_{PP1}(2)	V_{PP} Current Read			5	mA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby			40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(2)	V_{CC} Current Active			100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	V	$V_{CC} = 5.0V \pm 0.25$

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions	$V_{CC} \pm 5\%$ / $V_{CC} \pm 10\%$	27128B-110V05		27128B-135V05		27128B-150V10		Unit
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		110		135		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		110		135		150	ns
t_{OE}	$\overline{OE}$ to Output Delay		55		65		65	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	45	0	55	0	55	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns

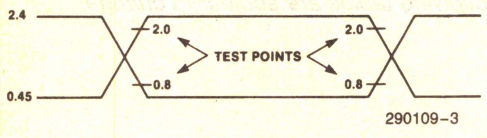
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE[2] T_A = 25°C, f = 1MHz

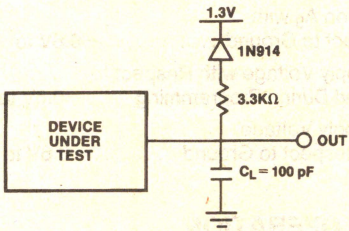
Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. TESTING INPUT/OUTPUT WAVEFORM



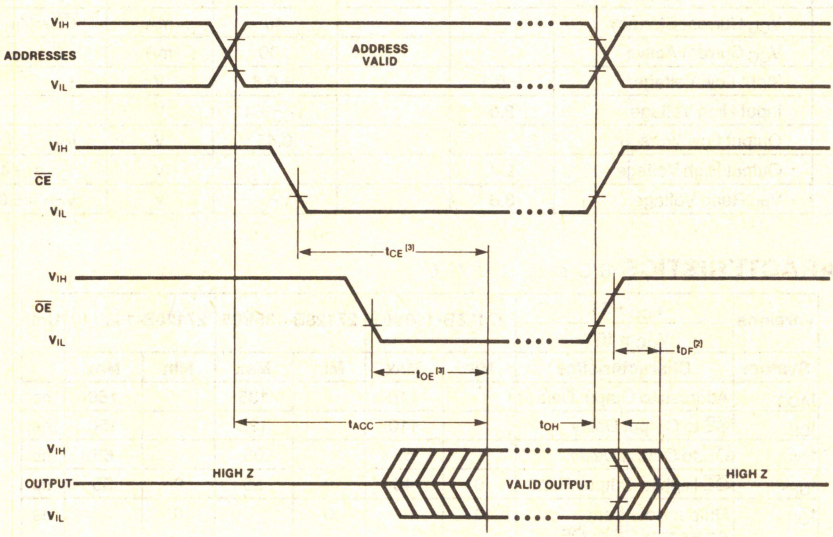
A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27128B are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Modes Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby		V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	5.0V	89 H
	Device(3)	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	5.0V	89 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1–A_8, A_{10}–$A_{12} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27128B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

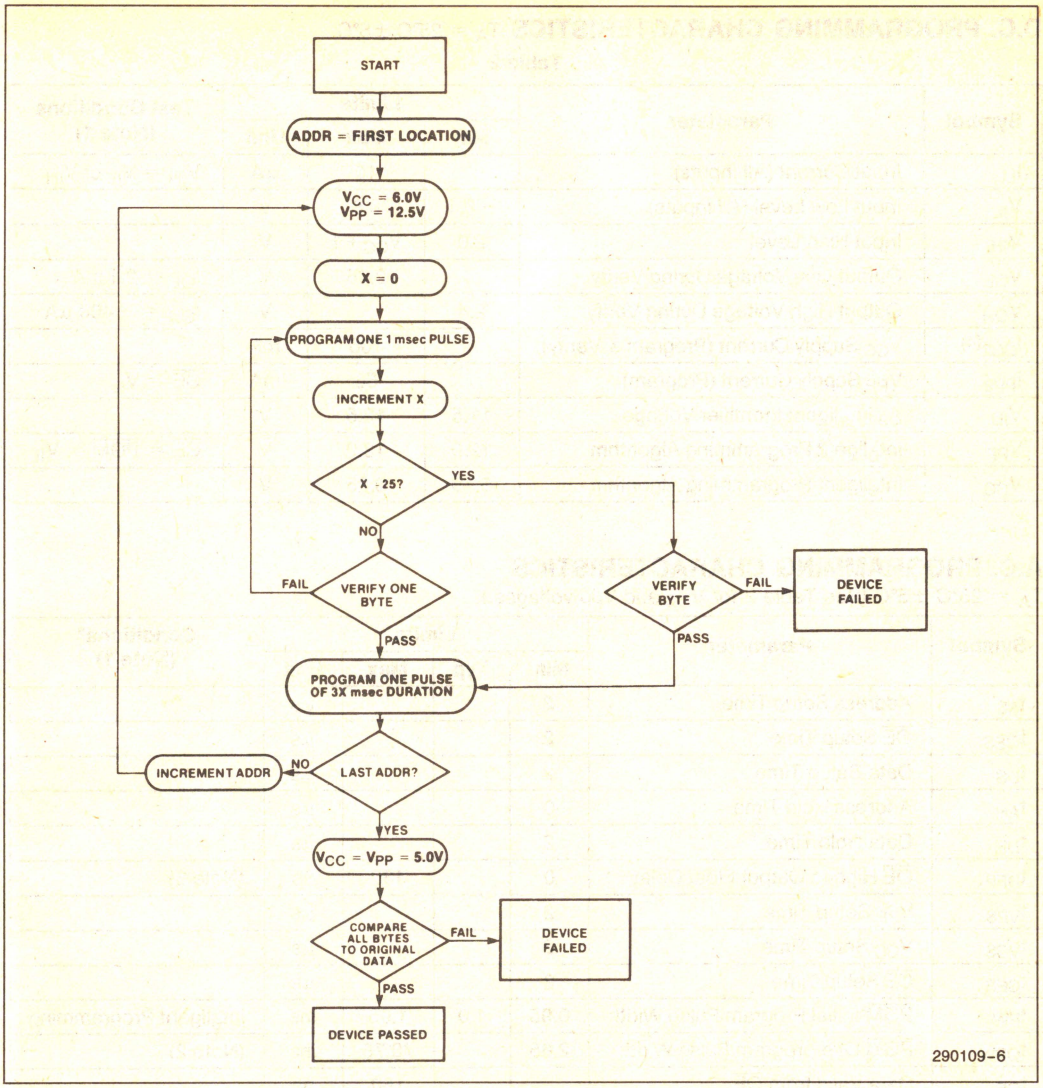


Figure 5. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm, a standard in the industry for the past few years, can be used to program all of Intels 12.5V V_{PP} EPROMs. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 5.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		100	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

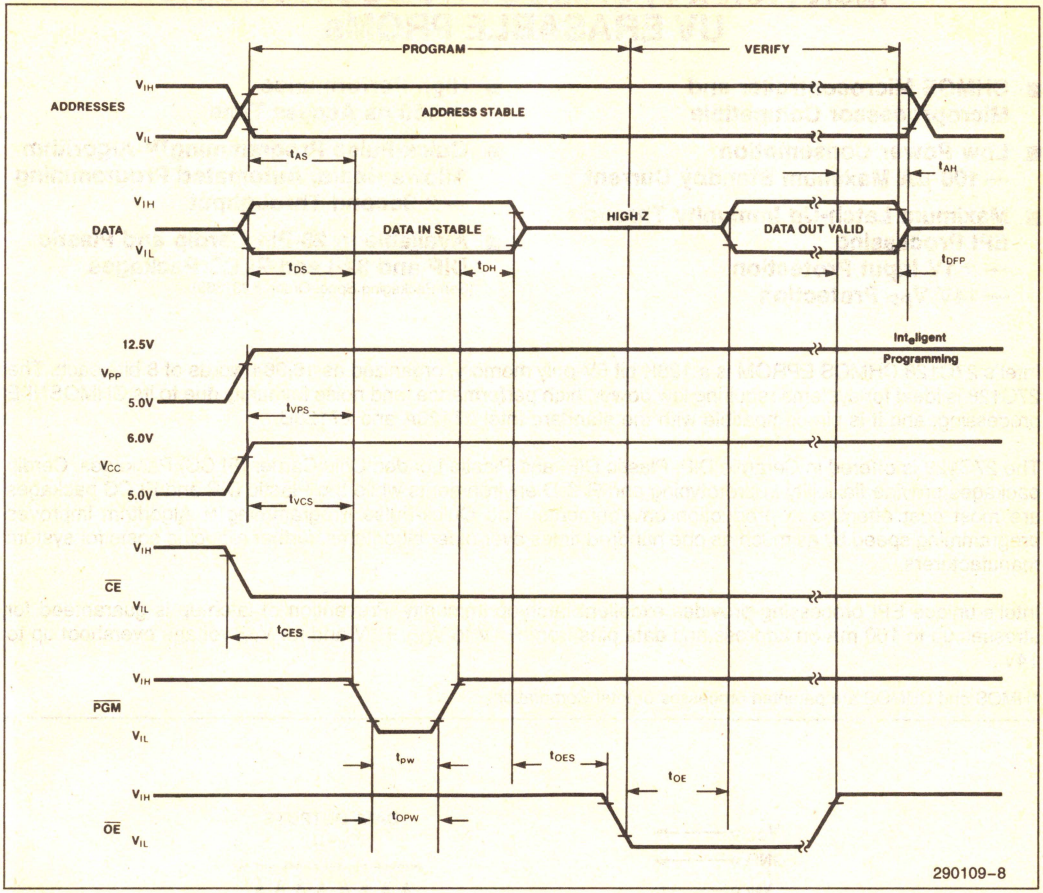
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (int$_e$ligent Programming Algorithm only) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27128B, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

27C128
128K (16K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMs

- **CHMOS Microcontroller and Microprocessor Compatible**
- **Low Power Consumption**
  — 100 μA Maximum Standby Current
- **Maximum Latch-Up Immunity Through EPI Processing**
  — ± 1V Input Protection
  — 14V V_{PP} Protection
- **High Performance**
  — 150 ns Access Time
- **Quick-Pulse Programming™ Algorithm Allows Rapid, Automated Programming**
  — 2 Second Throughput
- **Available in 28-Pin Cerdip and Plastic DIP and 32-Lead PLCC Packages**
  (See Packaging Spec. Order #231369)

Intel's 27C128 CHMOS EPROM is a 128K bit 5V-only memory, organized as 16,384 words of 8 bits each. The 27C128 is ideal for systems requiring low power, high performance, and noise immunity due to its CHMOS*II-E processing, and it is pin compatible with the standard Intel 27128A and 27128B.

The 27C128 is offered in Ceramic DIP, Plastic DIP, and Plastic Leaded Chip Carrier (PLCC) Packages. Cerdip packages provide flexibility in prototyping and R & D environments while the Plastic DIP and PLCC packages are most cost effective in production environments. The Quick-Pulse Programming™ Algorithm improves programming speed by as much as one hundred times over older algorithms, further reducing costs for system manufacturers.

Intel's unique EPI processing provides excellent latch-up immunity. Prevention of latch-up is guaranteed for stresses up to 100 mA on address and data pins from $-1V$ to $V_{CC} + 1V$ and for V_{PP} voltage overshoot up to 14V.

*HMOS and CHMOS are patented processes of Intel Corporation.

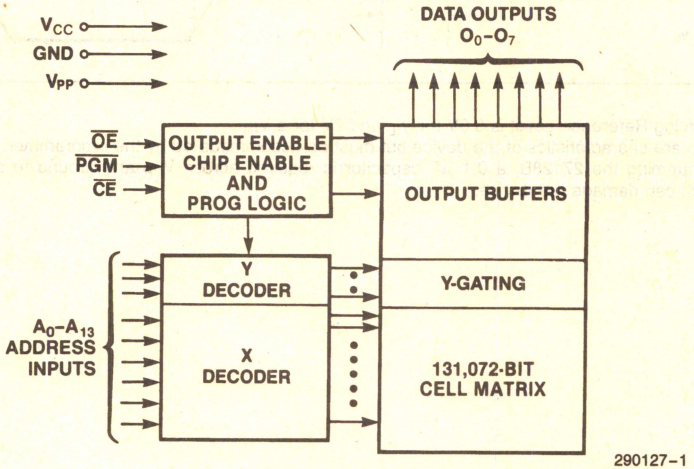


Figure 1. Block Diagram

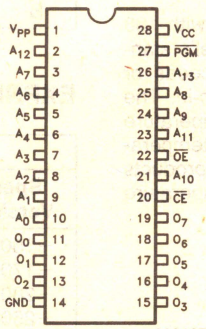
October 1987
Order Number: 290127-002

Pin Names

A_0–A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	No Internal Connect
D.U.	Don't Use

27C128

27C256	27C64	2732A
V_{PP}	V_{PP}	
A_{12}	A_{12}	
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
Gnd	Gnd	Gnd

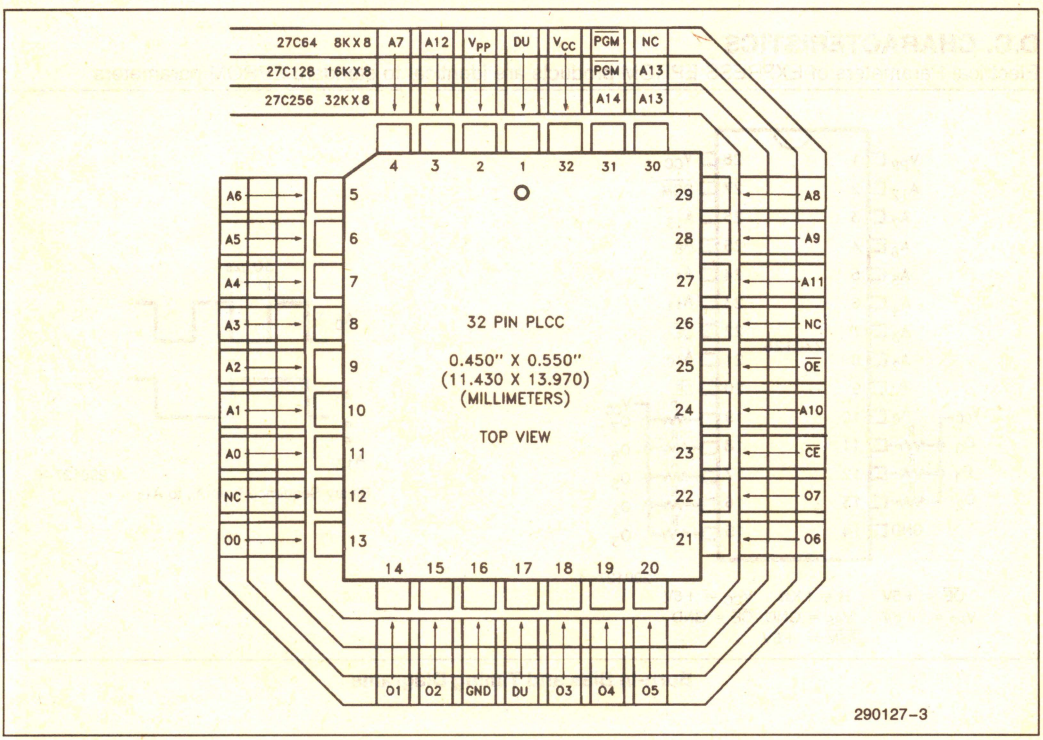


290127-2

2732A	27C64	27C256
	V_{CC}	V_{CC}
	$\overline{PGM}$	A_{14}
V_{CC}	N.C.	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

NOTE:
Intel "Universal Site"-Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27C128 Pins.

Figure 2. Cerdip(D)/Plastic(P) DIP Pin Configurations



290127-3

Figure 3. PLCC(N) Lead Configuration

Extended Temperature (Express) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications.

EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available along with automotive temperature range (−40°C to +125°C) products.

EXPRESS EPROM Product Family

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0 to +70	168 ±8
T	−40 to +85	NONE
L	−40 to +85	168 ±8
A	−40 to +125	NONE
B	−40 to +125	168 ±8

EXPRESS Options

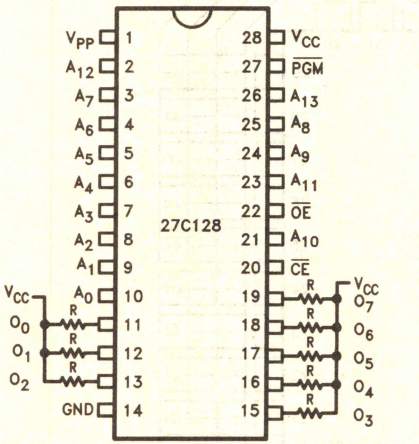
27C128 Versions

Packaging Options			
Speed Versions	**Cerdip**	**PLCC**	**Plastic DIP**
−150V05	T, L, Q		
−170V05	T, L, Q	T	T
−200V05	T, L, Q, A, B	T, A	T, A
−250V05	T, L, Q, A, B	T, A	T, A

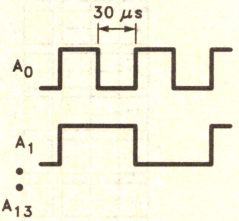
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters



$\overline{OE}$ = +5V R = 1 KΩ V_{CC} = +5V
V_{PP} = +5V V_{SS} = GND $\overline{CE}$ = GND
$\overline{PGM}$ = +5V



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Binary Sequence from A_0 to A_{13}

Burn-in Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... −55°C to +125°C

Temperature Under Bias ..... −55°C to +125°C

Storage Temperature ..... −65°C to +125°C

Voltage on Any Pin with
Respect to Ground ..... −2.0V to +7V(1)

Voltage on Pin A_9 with
Respect to Ground ..... −2.0V to +13.5V(1)

V_{PP} Supply Voltage with Respect to Ground
During Programming ..... −2.0V to +14V(1)

V_{CC} Supply Voltage with
Respect to Ground ..... −2.0V to 7.0V(1)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter		Notes	Min	Typ(2)	Max	Unit	Test Condition
I_{LI}	Input Leakage Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{PP_1}	V_{PP} Current Read		5			100	µA	$V_{PP} = V_{CC}$
I_{SB}	V_{CC} Current Standby with Inputs—	CMOS	4			100	µA	$\overline{CE} = V_{IH}$
		TTL	3			1.0	mA	
I_{CC1}	V_{CC} Current Active		5			30	mA	$\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage (±10% Supply) (TTL)			2.0		V_{CC} + 0.5	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			V_{CC} −0.2		V_{CC} + 0.2		
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			3.5			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	
V_{PP}	V_{PP} Read Voltage		7	V_{CC} − 0.7		V_{CC}	V	

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. Voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C.
3. V_{IL}, V_{IH} levels at TTL inputs.
4. $\overline{CE}$ is V_{CC} ± 2.0V. All other inputs can have any value within spec.
5. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with Outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.

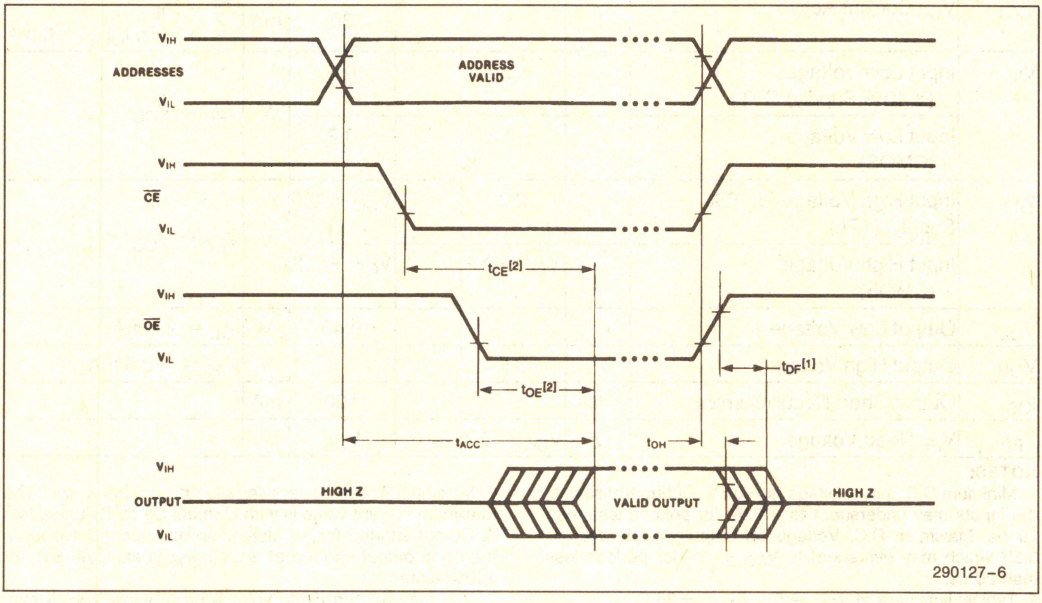
READ OPERATION

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Versions(3)		$V_{CC} \pm 5\%$	27C128-150V05		27C128-170V05 P27C128-170V05 N27C128-170V05		27C128-200V05 P27C128-200V05 N27C128-200V05		27C128-250V05 P27C128-250V05 N27C128-250V05		Unit
		$V_{CC} \pm 10\%$	27C128-150V10		27C128-170V10		27C128-200V10 P27C128-200V10 N27C128-200V10		27C128-250V10 P27C128-250V10 N27C128-250V10		
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay			150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay			75		75		75		100	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z			35		55		55		60	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First		0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 3.5V$.
2. Guaranteed and sampled.
3. Part Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS



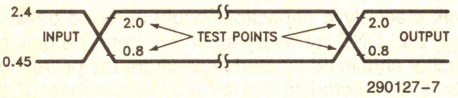
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE(1) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	pF	$V_{OUT} = 0V$

NOTE:
1. Sampled. Not 100% tested.

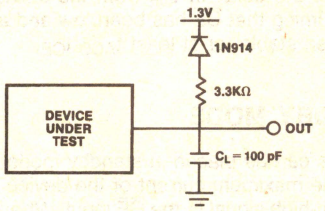
A.C. TESTING INPUT/OUTPUT WAVEFORM



290127-7

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



290127-8

C_L = 100 pF
C_L includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the 27C128 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for inteligent Identifier mode.

Table 1. Mode Selection for 27C128

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	High Z
inteligent Identifier(3) -Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H
inteligent Identifier(3) Device	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	FC H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $V_H = 12.0V \pm 0.5V$.
3. A_1–A_8, $A_{10-13} = V_{IL}$.
4. See Table 2 for V_{CC} and V_{PP} voltages.

READ MODE

The 27C128 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient and inductive current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low and $\overline{OE}$ = V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ = V_{IL} will program the selected device.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{CC} and V_{PP} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{OE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 400 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

HIGH RELIABILITY CHMOS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from -1V to $V_{CC} + 1$V.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

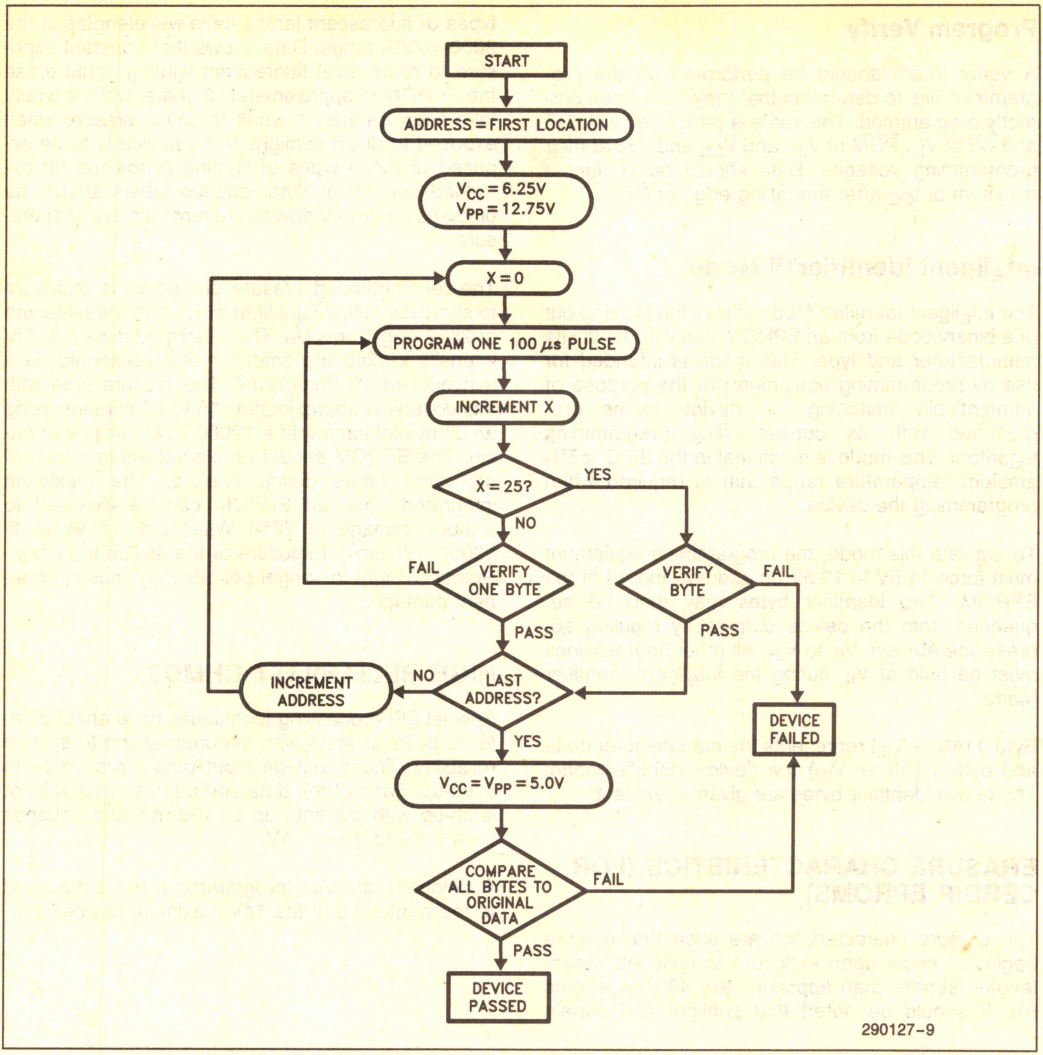


Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27C128 EPROM is programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production environment. This algorithm allows the device to be programmed in under two seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5$ mA
I_{CC2}(3)	V_{CC} Supply Current		30	mA	
I_{PP2}(3)	V_{PP} Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$
V_{ID}	A9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Programming Voltage	12.5	13.0	V	
V_{CC}	Supply Voltage during Programming	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$, See Table 2 for V_{CC} and V_{PP} Voltages

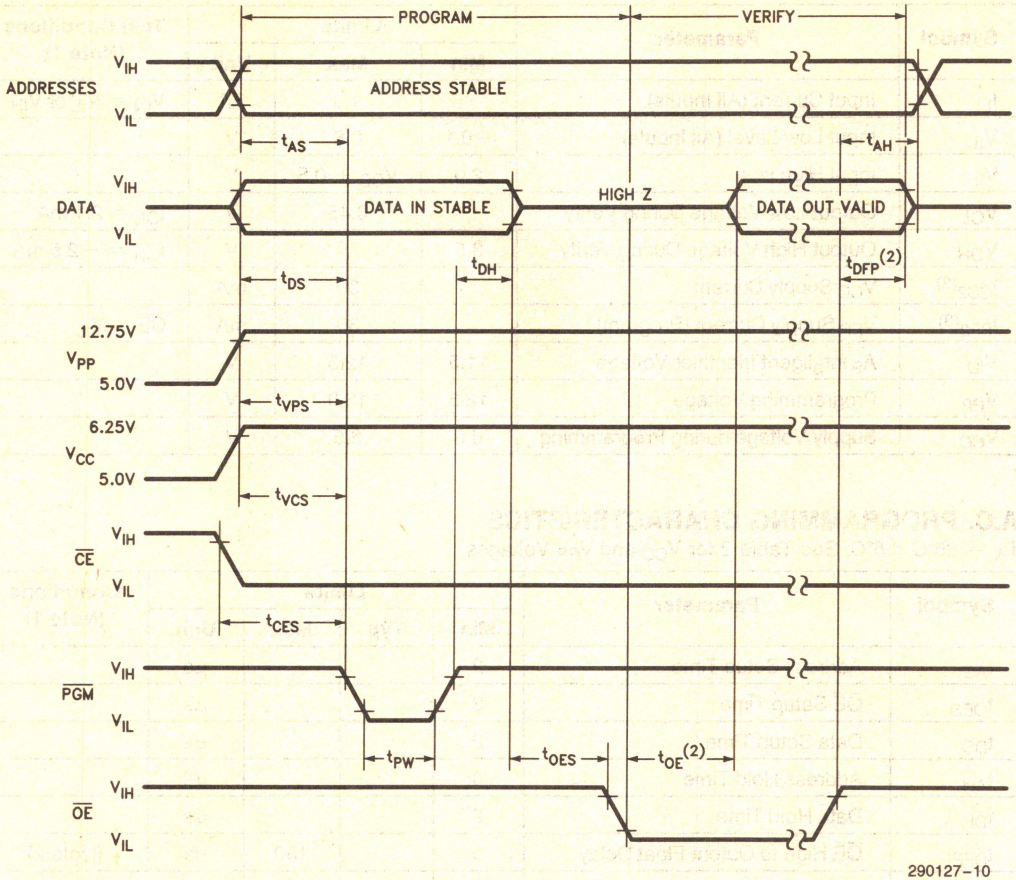
Symbol	Parameter	Limits				Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Intitial Program Pulse Width	95	100	105	μs	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

A.C CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 3.5V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0 to O_7 Unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C128, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

27256
256K (32K x 8) PRODUCTION AND UV ERASABLE PROMS

- **New Quick-Pulse Programming™ Algorithm for Plastic P27256**
  - **— 4 Second Programming**
  - **— int$_e$ligent Programming™ Algorithm Compatible**
- **Fast Access Time**
  - **— 170 ns D27256-1**
  - **— 200 ns P27256-2**
- **int$_e$ligent Identifier™ Mode**
- **Plastic Production P27256 is Compatible with Auto-Insertion Equipment**
- **Moisture Resistant**
- **Industry Standard Pinout . . . JEDEC Approved . . . 28 Lead Cerdip and Plastic Package**

(See Packaging Spec, Order #231369)

The Intel 27256 is a 5V only, 262,144-bit Ultraviolet Erasable (Cerdip)/plastic production (P27256) electrically programmable read-only memory (EPROM). Organized as 32K words by 8 bits, individual bytes can be accessed in less than 170 ns (27256-1). This is compatible with high performance microprocessors, such as the Intel iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The Plastic P27256 is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27256 to be programmed within four seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int$_e$ligent Identifier and rapidly program it using a superior programming method. The int$_e$ligent Programming Algorithm may be utilized in the absence of such equipment.

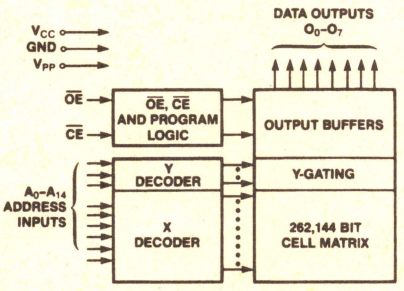
The 27256 enables implementation of new, advanced systems with firmware-intensive architectures. The combination of the 27256's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and elminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS*II-E technology.

*HMOS is a patented process of Intel Corporation.



290097-1

Figure 1. Block Diagram

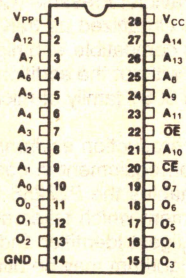
October 1987
Order Number: 290097-003

Pin Names

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
D.U.	Don't Use
$\overline{WE}$	Write Enable

27916	27513	27512	27128A	2764A 27C64	2732A	2716
V_{PP}	D.U.	A_{15}	V_{PP}	V_{PP}		
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}		
A_7	A_7	A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0	A_0	A_0
O_0	D_0/O_0	O_0	O_0	O_0	O_0	O_0
O_1	D_1/O_1	O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd

27256
P27256



290097-2

2716	2732A	2764A 27C64	27128A	27512	27513	27916
		V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{PGM}$	V_{CC} A_{14}	V_{CC} / $\overline{WE}$	V_{CC} / $\overline{PGM/WE}$
V_{CC}	V_{CC}	N.C.	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9	A_9	A_9
V_{PP}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P27256 pins.

Figure 2. Cerdip/Plastic DIP Pin Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27256 VERSIONS

Speed Versions	Packaging Options: Cerdip	Packaging Options: Plastic
-2	Q, T, L	
STD	Q, T, L	
-3	Q, T, L	
-20	Q, T, L	
-25	Q, T, L	
-30	Q, T, L	

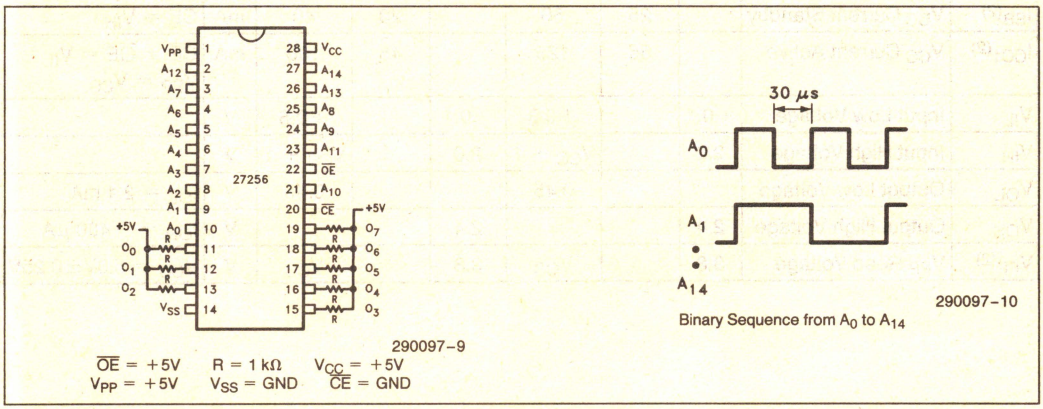
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27256 LD27256 Min	TD27256 LD27256 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC}(1)	V_{CC} Active Current (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with
Respect to Ground ..... −0.6V to +6.25V

Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V

V_{PP} Supply Voltage with Respect
to Ground ..... −0.6V to +14.0V

V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	27256-1, 27256-2, 27256-20, P27256-2 & P27256-5 Limits			27256L-20, 27256-25, 27256-30, 27256L-1, 27256L-2, 27256, 27256-3 P27256-25, P27256-30, P27256 & P27256-3 Limits			Unit	Test Conditions
		Min	Typ (3)	Max	Min	Typ (3)	Max		
I_{LI}	Input Load Current			10			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10			10	μA	$V_{OUT} = 5.5V$
I_{PP_1}(2)	V_{PP} Current Read/Standby			5			5	mA	$V_{PP} = 5.5V$
I_{SB}(2)	V_{CC} Current Standby		25	50		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(2)	V_{CC} Current Active		55	125		45	100	mA	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$
V_{IL}	Input Low Voltage	−0.1		+0.8	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			2.4			V	$I_{OH} = -400$ μA
V_{PP}(2)	V_{PP} Read Voltage	3.8		V_{CC}	3.8		V_{CC}	V	$V_{CC} = 5.0V \pm 0.25V$

READ OPERATION

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions(5)		$V_{CC} \pm 5\%$		27256-1 27256L-1		27256L-2 27256-2 P27256-2		27256 P27256 P27256-5		27256-3 P27256-3		Unit	Test Conditions
		$V_{CC} \pm 10\%$				27256L-20 27256-20		27256-25 P27256-25		27256-30 P27256-30			
Symbol	Parameter			Min	Max	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay				170		200		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay				170		200		250		300	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay				70		75		100		120	ns	$\overline{CE} = V_{IL}$
t_{DF}(4)	$\overline{OE}$ High to Output Float			0	35	0	55	0	60	0	105	ns	$\overline{CE} = V_{IL}$
t_{OH}(4)	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First			0		0		0		0		ns	

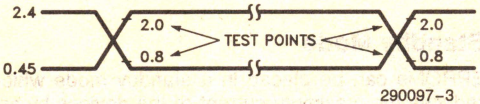
NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with outputs O_0 to O_7 unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP.

CAPACITANCE(2) ($T_A = 25°C$, f = 1 MHz)

Symbol	Parameter	Typ(1)	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

NOTES:
1. $T_A = 25°C$, $V_{CC} = 5.0V$.
2. This parameter is only sampled and is not 100% tested.

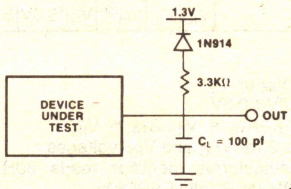
A.C. TESTING INPUT/OUTPUT WAVEFORM



290097-3

A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

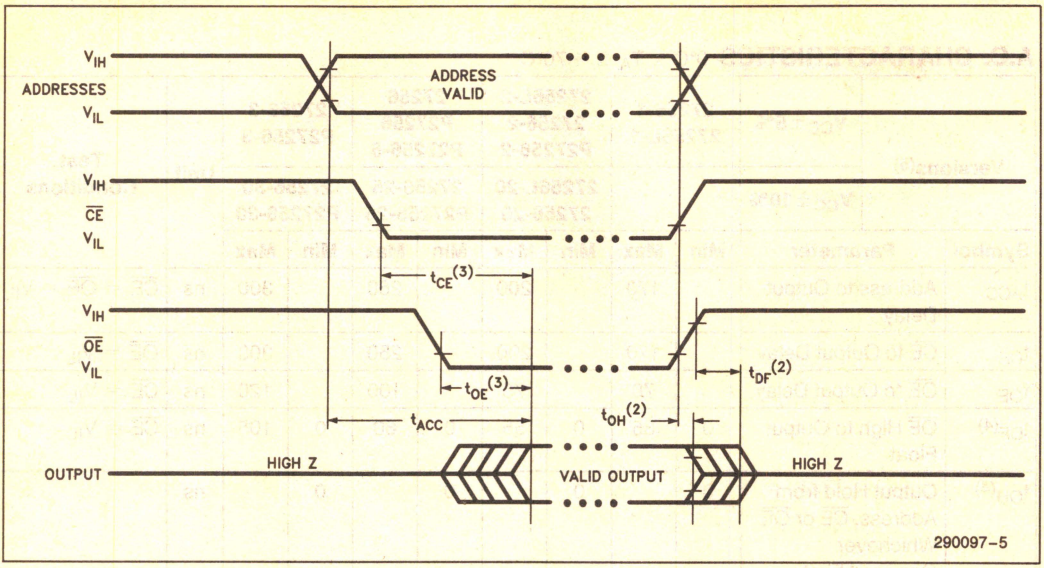
A.C. TESTING LOAD CIRCUIT



290097-4

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

Table 1. Operating Modes

Pins / Mode	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{OUT}
Optional Program Verify	V_{IL}	V_{IL}	X	X	V_{CC}	(4)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(4)	(4)	High Z
intelligent Identifier(3)							89H(5)
—manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	5.0V	5.0V	88H(5)
—device	V_{IL}	V_{IL}	V_H(2)	V_{IH}	5.0V	5.0V	04H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. V_H = 12.0V±0.5V.
3. A_1-A_8, $A_{10}-A_{13}$ = V_{IL}, A_{14} = V_{IH}.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. The manufacturers identifier reads 89H for Cerdip EPROMs; 88H for Plastic EPROMs.

DEVICE OPERATION

The modes of operation of the 27256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for intelligent identifier mode.

Read Mode

The P27256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

EPROMs can be placed in a standby mode which reduces the maximum current of the devices by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1"is by ultraviolet light exposure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with V_{PP} at its programming voltage will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, and V_{PP} and V_{CC} at their programming voltages.

Optional Program Verify

The optional verify may be performed in place of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at its programming voltage. The outputs will tri-state according to the signal presented to $\overline{OE}$. Therefore, all devices with V_{PP} = 12.75V (12.5V int$_e$ligent programming) and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share a common bus, V_{PP} should be lowered to V_{CC} (= 6.25/6.0V—see Table 2) and the normal read mode used to execute a program verify.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device.

To activiate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the EPROM is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

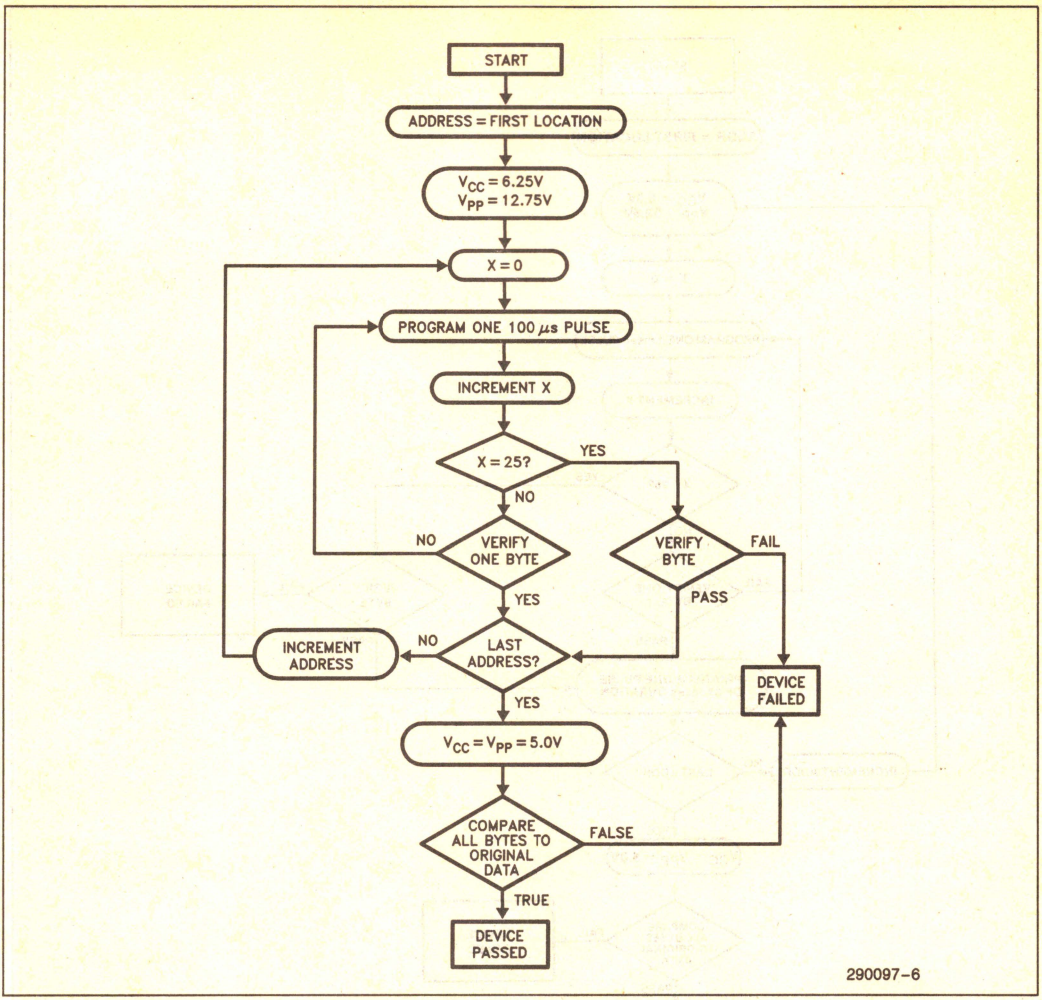


Figure 3. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (For Plastic and PLCC EPROMs)

Intel's Plastic EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows Plastic devices to be programmed in under four seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 3.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, Plastic EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

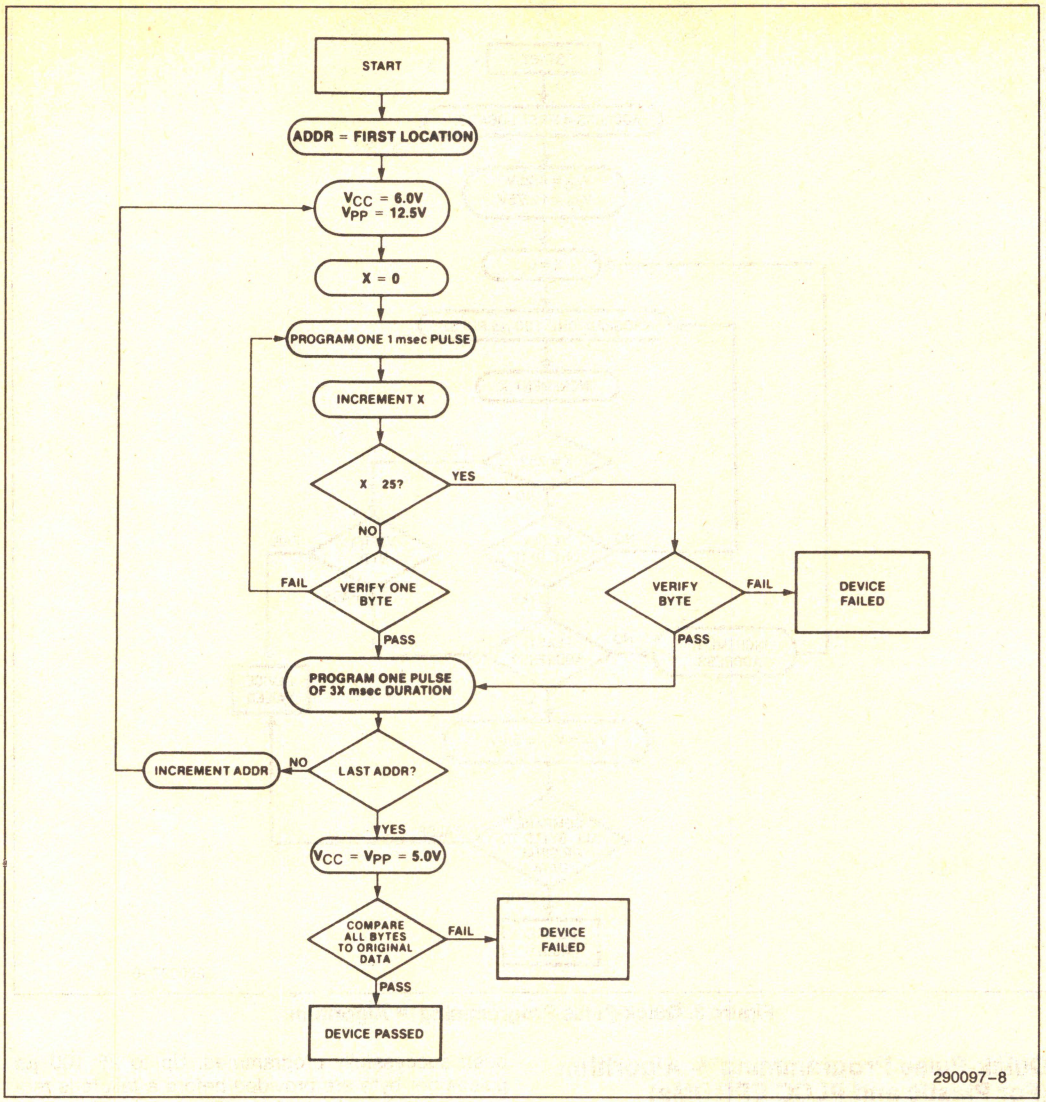


Figure 4. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm has been a standard in the industry for the past few years. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 4.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS $T_A = 25 \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (see Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output HIgh Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		125	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 inteligent Identifier Voltage	11.5	12.5	V	
V_{PP}	inteligent Programming Algorithm	12.0	13.0	V	$\overline{CE} = V_{IL}$
	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = V_{IL}$
V_{CC}	inteligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5°C$ (see table 2 for V_{CC} and V_{PP} voltages)

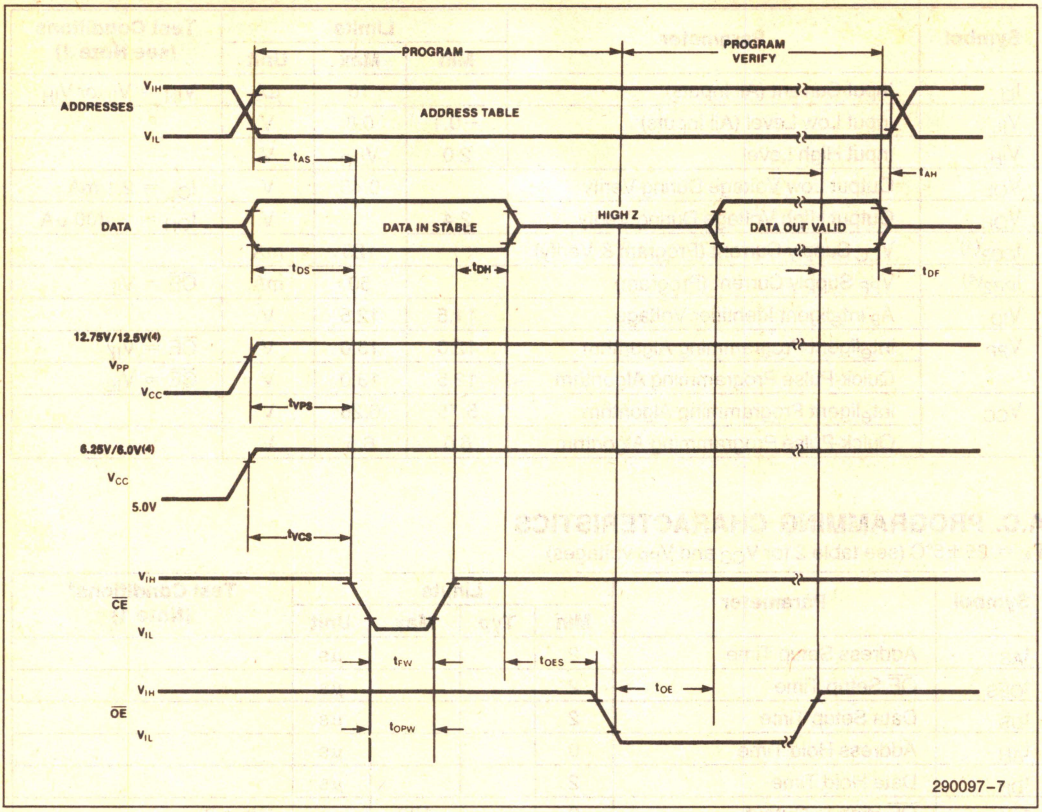
Symbol	Parameter	Limits				Test Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Data Float Delay	0		130	μs	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	inteligent Programming
		95	100	105	μs	Quick-Pulse Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times
(10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X (inteligent Programming Algorithm only).
3. This parameter is only sampled and is not 100% tested. Output Data Float is defined as the point where data is no longer driven—see timing diagram on the following page.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27256 a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm. 12.5V V_{PP} & 6.0V V_{CC} for int$_e$ligent Programming Algorithm.

27C256
256K (32K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- **High Speed***
  - **— 120 ns Access Time**
- **Low Power Consumption***
  - **— 50 μA Standby, 20 mA Active Current Available**
- **Fast Programming**
  - **— 4 Second Programming for High Throughput**
- **EPI Processing**
  - **— Maximum Latch-up Immunity**
- **Simple Interfacing**
  - **— Two Line Control**
  - **— CMOS and TTL Compatible**
- **Versatile JEDEC-Approved Packaging**
  - **— Standard 28 Pin CERDIP**
  - **— Compact 32-Lead PLCC**
  - **— Cost Effective Plastic DIP**

(See Packaging Spec., Order #231369)

Intel's 27C256 EPROM is a 256K-bit 5V-only memory, organized as 32,768 words of 8 bits. The 27C256 is ideal in embedded control applications based on advanced 16-bit CPUs. Fast 120 ns access times allow no-Wait-state operation with 12 MHz 80286. The 27C256 also excels in reprogrammable environments where the system designer must strike an optimal density/performance balance. For example, bootstrap and diagnostic routines run fast with 1 Wait-state on a 16 MHz 80386.

The 27C256 is offered in Ceramic Dual In-Line Package (DIP or CERDIP), Plastic DIP (PDIP), and Plastic Leaded Chip Carrier (PLCC) packages. Cerdip packages provide flexibility in prototyping and R&D environments while PDIP and PLCC are most cost effective in production environments. The Quick-Pulse Programming™ Algorithm improves programming speed by as much as 100 times over older programming algorithms, further reducing cost for system manufacturers.

Intel's unique Epitaxial (EPI) processing provides excellent latch-up immunity. Prevention of latch-up guarantees for stresses up to 100 mA from $-1V$ to $V_{CC} + 1V$ on address and data pins and for V_{PP} voltage overshoot up to 14V.

*These specifications are advance information for the new CMOS III-E version.

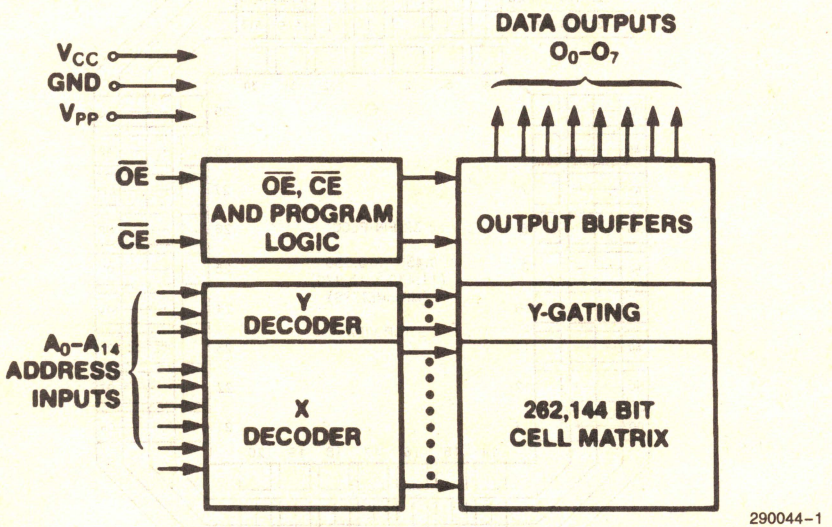


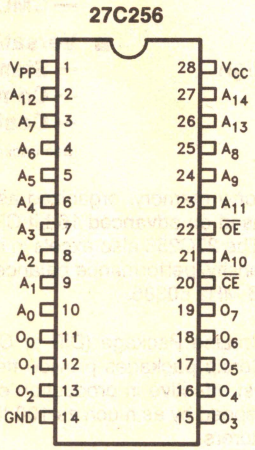
Figure 1. Block Diagram

November 1987
Order Number: 290044-007

Pin Names

A_0–A_{14}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
N.C.	NO CONNECT
D.U.	DON'T USE

27C128	27C64
V_{PP}	V_{PP}
A_{12}	A_{12}
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0
O_0	O_0
O_1	O_1
O_2	O_2
Gnd	Gnd

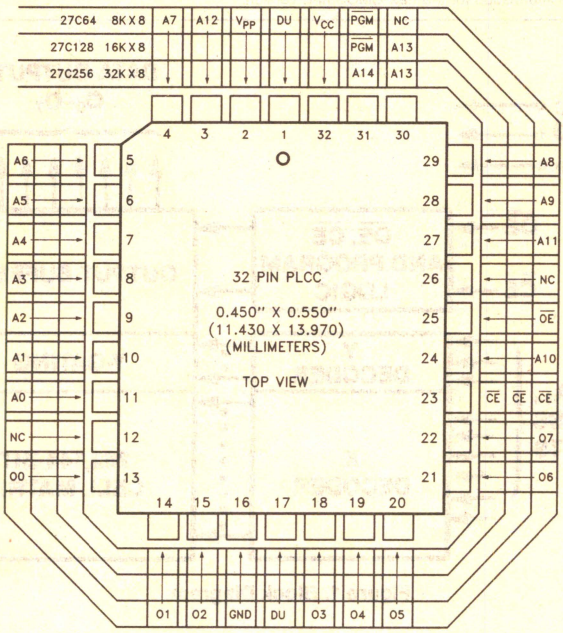


27C64	27C128
V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{PGM}$
N.C.	A_{13}
A_8	A_8
A_9	A_9
A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

290044-2

Figure 2. Pin Configuration

NOTE:
Intel "Universal Site" -Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent.



290044-10

Figure 3. PLCC Lead Configuration

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several EPROM densities allowing the appropriate memory size to match system applications. EXPRESS ROMs are available with 168 +8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process meets or exceeds most industry burn-in specifications. The standard EXPRESS EPROM operating temperature range is 0°C to +70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS and automotive temperature range (−40°C to +125°C) products are also available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

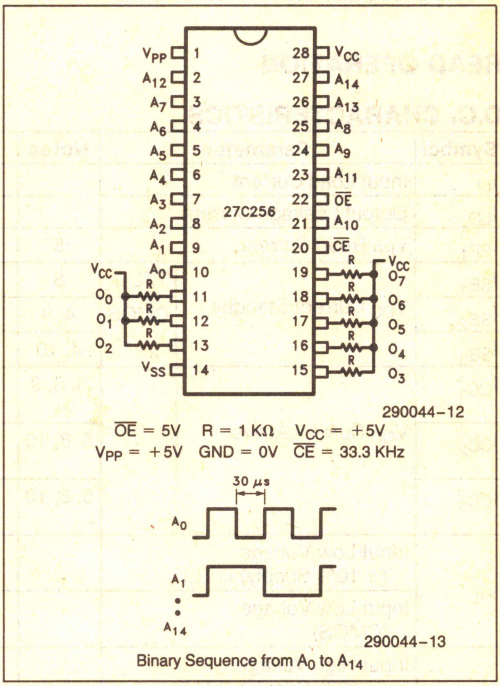
EXPRESS Options

Speed Versions	Packaging Options	
	Cerdip	PLCC
−120V05	Q	
−135V05	Q, T, L	
−135V10	Q, T, L	
−150V05	Q, T, L	
−150V10	Q, T, L	
−2	Q, T, L	
−20	Q, T, L	
−STD	Q, T, L, A	
−25	Q, T, L, A	

EPROM Product Family

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ±8
A(2)	−40°C to +125°C	NONE
B(2)	−40°C to +125°C	168 ±8



Burn-In Bias and Timing Diagrams

READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter		27C256 Min	27C256 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)	CMOS		0.1	$\overline{CE} = V_{CC}$, $\overline{OE} = V_{IL}$
		TTL		1.0	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)	TTL		30	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)	TTL		30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient}$ = 85°C

NOTES:
1. The maximum current value is with outputs O_0 to O_7 unloaded.
2. See Automotive data sheets for current and timing parameters.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C(2)
Temperature Under Bias ..... −10°C to +80°C(2)
Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with Respect to Ground ..... −2V to +7V(1)
Voltage on A_9 with Respect to Ground ..... −2V to +13.5V(1)
V_{PP} Supply Voltage with Respect to Ground During Programming ..... −2V to +14.0V(1)
V_{CC} Supply Voltage with Respect to Ground ..... −2V to +7.0V(1)

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter		Notes	Min	Typ(3)	Max	Unit	Test Conditions
I_{LI}	Input Load Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{PP_1}	V_{PP} Read Current		5			200	µA	$V_{PP} = V_{CC}$
I_{SB_1}	V_{CC} Current Standby	TTL	8			1.0	mA	$\overline{CE} = V_{IH}$
I_{SB_2}		CMOS	4, 9			100	µA	$\overline{CE} = V_{CC}$
I_{SB_3}			4, 10			50	µA	$\overline{CE} = V_{CC}$
I_{CC_1}	V_{CC} Current Active		5, 8, 9			30	mA	$\overline{CE} = V_{IL}$, f = 5 MHz
I_{CC_2}			5, 8, 10			20	mA	$\overline{CE} = V_{IL}$, f = 5 MHz
I_{CC_3}			5, 8, 10			25	mA	$\overline{CE} = V_{IL}$, f = 8 MHz
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2		
V_{IH}	Input High Voltage (±10% Supply) (TTL)			2.0		V_{CC} + 0.5	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			V_{CC} − 0.2		V_{CC} + 0.2		
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			3.5			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	
V_{PP}	V_{PP} Read Voltage		7	V_{CC} − 0.7		V_{CC}	V	

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
8. V_{IL}, V_{IH} levels at TTL inputs.
9. CHMOS II-E (-XX).
10. CHMOS III-E (−xxxVxx).

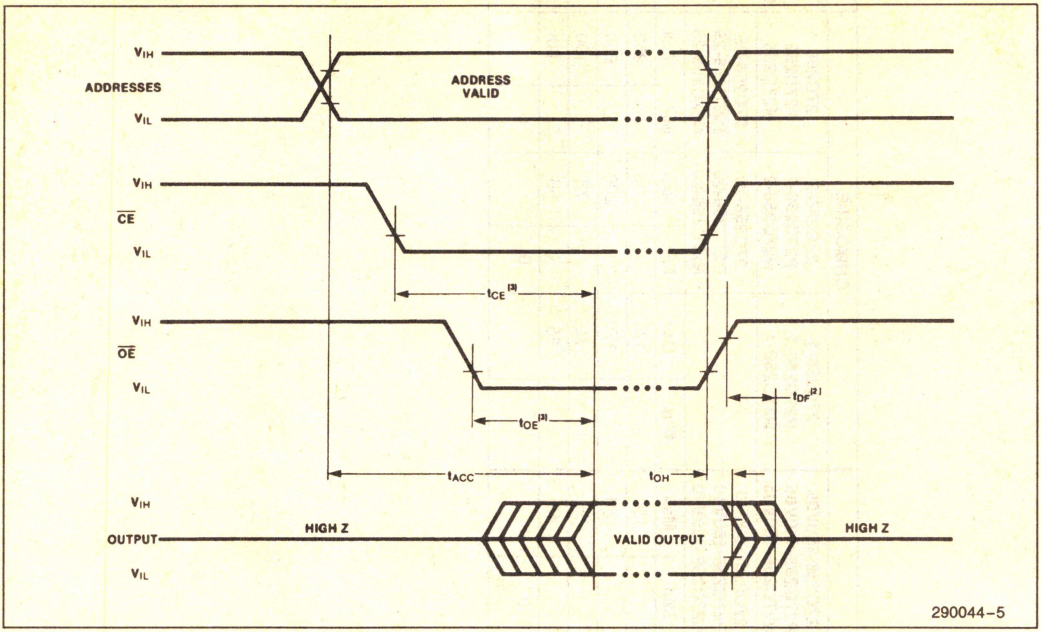
READ OPERATION

A.C. CHARACTERISTICS[1] $0°C \le T_A \le +70°C$

Versions [3, 4]		CHMOSIII-E						CHMOSII-E						Unit
	$V_{CC} \pm 5\%$	27C256-120V05		27C256-135V05 P27C256-135V05 N27C256-135V05		27C256-150V05 P27C256-150V05 N27C256-150V05		27C256-1 P27C256-1 N27C256-1		27C256-2 P27C256-2 N27C256-2		27C256 P27C256 N27C256		
	$V_{CC} \pm 10\%$			27C256-135V10 P27C256-135V10 N27C256-135V10		27C256-150V10 P27C256-150V10 N27C256-150V10				27C256-20 P27C256-20 N27C256-20		27C256-25 P27C256-25 N27C256-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to Output Delay		120		135		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		135		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		60		65		65		70		75		100	ns
t_{DF}[2]	$\overline{OE}$ High to Output High Z		30		35		45		55		55		60	ns
t_{OH}[2]	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	0		0		0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
   Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.
3. Package Prefixes: No Prefix = CERDIP; N = PLCC; P = Plastic DIP.
4. All products with the 6-digit speed identifier are produced on CHMOS III-E technology.

A.C. WAVEFORMS



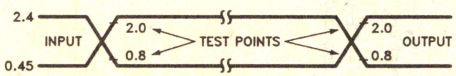
NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

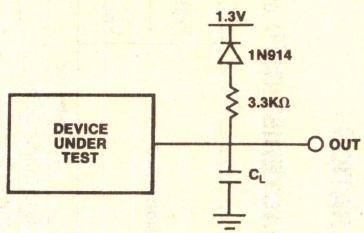
NOTE:
1. Sampled. Not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} (TTL) for a Logic "1" and V_{IL} (TTL) for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the 27C256 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier™ mode.

Table 1. Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(Note 6)	(Note 6)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(Note 6)	(Note 6)	D_{OUT}
Optional Program Verify	V_{IL}	V_{IL}	X	X	V_{CC} (Note 6)	(Note 6)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(Note 6)	(Note 6)	HIGH Z
int$_e$ligent Identifier (3) -Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H
int$_e$ligent Identifier (3, 4) -27C256-XX	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	8C H
int$_e$ligent Identifier (3, 5) -27C256-XXXVXX	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	8D H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ± 0.5V.
3. A_1–A_8, A_{10-12} = V_{IL}.
4. Device Identifier for CHMOS II-E product.
5. Device Identifier for CHMOS III-E product.
6. See Table 2 for V_{CC} and V_{PP} voltages during programming.
7. Both the 8C H and 8D H codes are recognized by EPROM programming equipment.

Read Mode: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

Standby Mode

The standby mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the standby mode places the outputs in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory-array devices and the system's READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in low-power standby mode.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in three supply current (ICC) issues—standby current levels, active current levels, and transient current peaks produced by falling and rising edges of Chip Enable. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

PROGRAMMING MODES

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" are programmed, the data word can contain both "1's" and "0's". Ultraviolet light erasure is the only way to change "0's" to "1's".

The programming mode is entered when V_{PP} is raised to its programming voltage (see Table 2). Data is programmed by applying an 8-bit word to the output pins (0–7). Pulsing $\overline{CE}$ to TTL-low while $\overline{OE}$ = V_{IH} will program data. TTL levels are required for address and data inputs.

Program Inhibit

The Program Inhibit mode allows parallel programming of multiple EPROMs with different data. With V_{PP} at its programming voltage, a $\overline{CE}$-low pulse programs the desired EPROM. $\overline{CE}$-high inputs inhibit programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

Program Verify

With V_{PP} and V_{CC} at their programming voltages, a verify (read) determines that bits are correctly programmed. The verify is performed with $\overline{CE}$ = V_{IH} and $\overline{OE}$ = V_{IL}. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Optional Program Verify

All 27C256s with V_{PP} = 12.75V and $\overline{OE}$ = V_{IL} present data on the bus independent of $\overline{CE}$. The optional verify allows parallel programming and verification when several devices share a common bus. It is performed with $\overline{CE}$ = $\overline{OE}$ = V_{IL} and V_{PP} = V_{CC} = 6.25V. The normal read mode is then used for program verify. Outputs will tri-state depending on $\overline{OE}$ and $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type. Programming equipment can automatically match a device with its proper programming algorithm.

This mode is activated when programming equipment forces 12V + 0.5V on the EPROM's A_9 address line. With A_1–A_8, A_{10}–A_{12} = V_{IL}, address line A_0 = V_{IL} will present the manufacturer's code and A_0 = V_{IH} the device code (see Table 1). This mode functions in the 25°C + 5°C ambient temperature range required while programming.

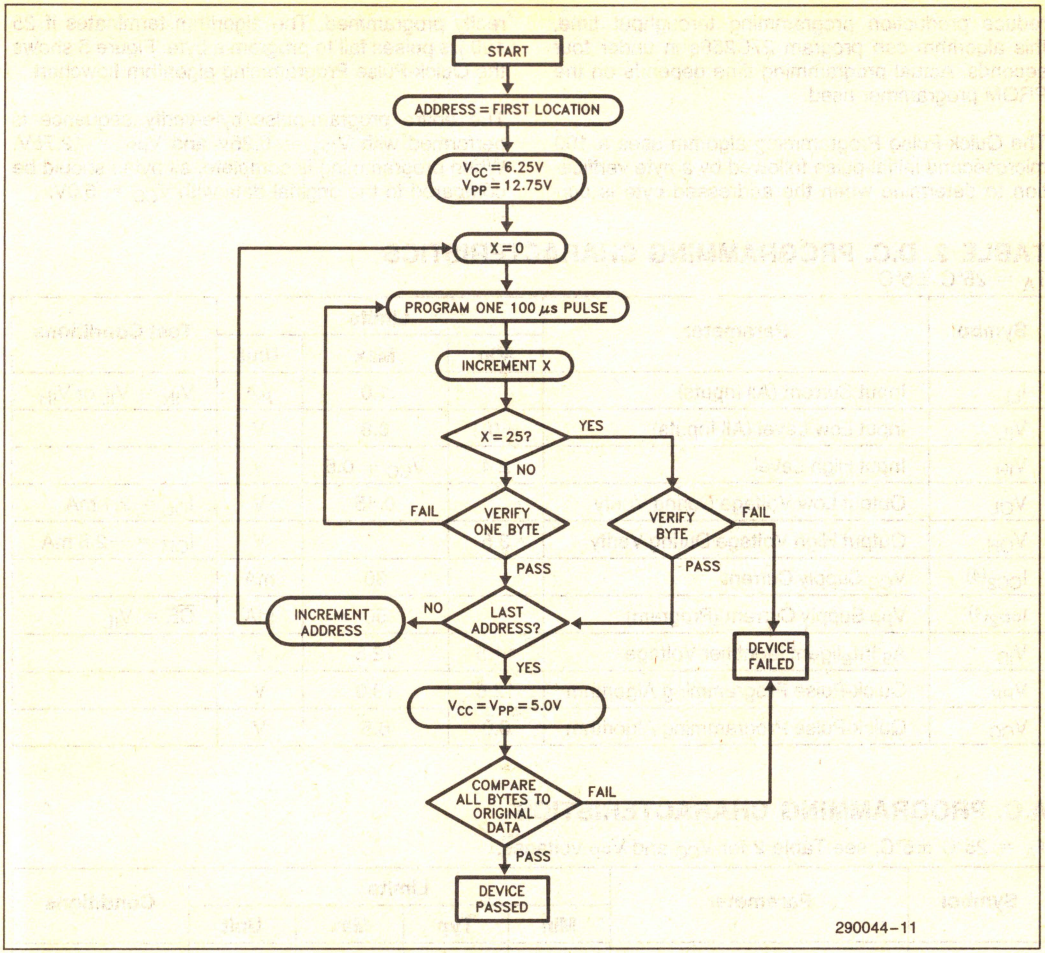


Figure 5. Quick-Pulse Programming™ Algorithm

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

Exposure to light of wavelength shorter than 4000 Angstroms (Å) begins EPROM erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000–4000Å range. Constant exposure to room-level fluorescent light can erase an EPROM in about 3 years (about 1 week for direct sunlight). Opaque labels over the window will prevent unintentional erasure under these lighting conditions.

The recommended erasure procedure is exposure to 2537Å ultraviolet light. The minimum integrated dose (intensity x exposure time) is 15 Wsec/cm. Erasure time using a 12000 μW/cm ultraviolet lamp is approximately 15 to 20 minutes. The EPROM should be placed about 1 inch from the lamp. The maximum integrated dose is 7258 Wsec/cm (1 week @ 12000 μW/cm). High intensity UV light exposure for longer periods can cause permanent damage.

CHMOS NOISE CHARACTERISTICS

System reliability is enhanced by Intel's CHMOS EPI-process techniques. Protection on each data and address pin prevents latch-up; even with 100 mA currents and voltages from −1V to V_{CC} + 1V. Additionally, the V_{PP} pin is designed to resist latch-up to the 14V maximum device limit.

Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming algorithm programs Intel's 27C256 EPROM. Developed to substantially

reduce production programming throughput time, this algorithm can program 27C256s in under four seconds. Actual programming time depends on the PROM programmer used.

The Quick-Pulse Programming algoritm uses a 100 microsecond initial-pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100 μs pulses fail to program a byte. Figure 5 shows the Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/byte-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. When programming is complete, all bytes should be compared to the original data with V_{CC} = 5.0V.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.4	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	3.5		V	I_{OH} = −2.5 mA
I_{CC2}(4)	V_{CC} Supply Current		30	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 Intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

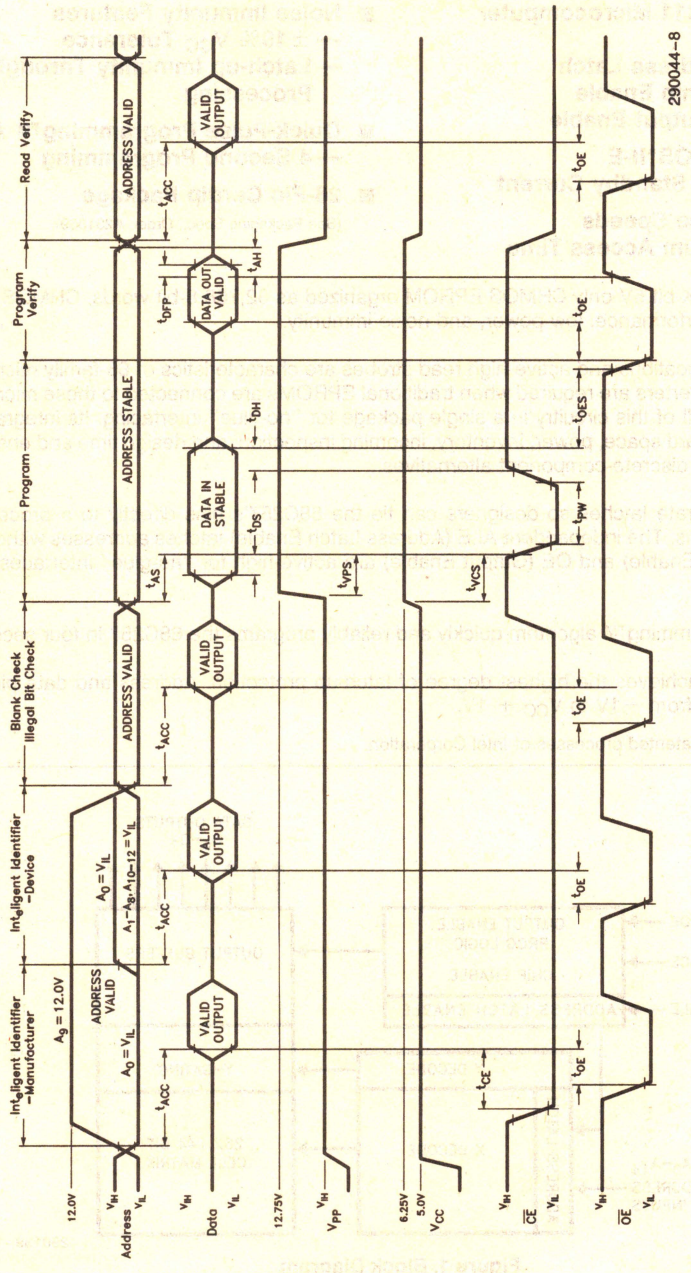
A.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C; see Table 2 for V_{CC} and V_{PP} voltages.

Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{PW}	$\overline{CE}$ Program Pulse Width	95	100	105	μs	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested.
3. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

68C257
256K (32K x 8) CHMOS UV ERASABLE PROM

- **6801, 6803, 68HC11 Microcomputer Compatible**
  - **— Integrated Address Latch**
  - **— Active-High Chip Enable**
  - **— Active-High Output Enable**
- **Low Power CHMOS*II-E**
  - **— 100 μA CMOS Standby Current**
- **High Performance Speeds**
  - **— 170 ns Maximum Access Time**
- **Noise Immunity Features**
  - **— $\pm$10% V_{CC} Tolerance**
  - **— Latch-up Immunity Through EPI Processing**
- **Quick-Pulse Programming™ Algorithm**
  - **— 4 Second Programming**
- **28-Pin Cerdip Package**
  (See Packaging Spec., Order #231369)

Intel's 68C257 is a 256K-bit 5V only CHMOS EPROM organized as 32,768 8-bit words. CHMOS*II-E circuitry provides high speed performance, low power, and noise immunity.

High-memory boot-up locations and active-high read strobes are characteristics of 68-family microcomputers. Address latches and inverters are required when traditional EPROMs are connected to these microcomputers. The 68C257 contains all of this circuitry in a single package for "no-glue" interfacing. Its integrated features reduce system cost, board space, power, inventory, incoming inspection, and design time and ensure performance that is superior to discrete-component alternatives.

Address inputs incorporate latches so designers can tie the 68C257's pins directly to a processor's multiplexed address/data pins. The independent ALE (Address Latch Enable) latches addresses without impacting access time. CE (Chip Enable) and OE (Output Enable) are active-high for "no-glue" interfaces to 68-family microcomputers.

The Quick-Pulse Programming™ algorithm quickly and reliably programs the 68C257 in four seconds or less.

Intel's EPI processing achieves the highest degree of latch-up protection. Address and data pins withstand stresses up to 100 mA from -1V to $V_{CC} + 1$V.

*HMOS and CHMOS are patented processes of Intel Corporation.

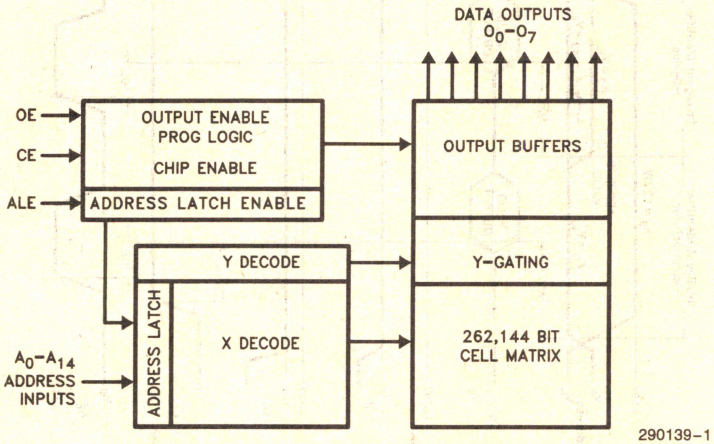


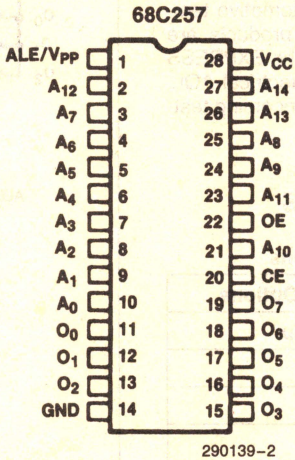
Figure 1. Block Diagram

October 1987
Order Number: 290139-002

Pin Names

A_0–A_{14}	ADDRESSES
O_0–O_7	OUTPUTS
OE, $\overline{OE}$	OUTPUT ENABLE
CE, $\overline{CE}$	CHIP ENABLE
ALE/V_{PP}	ADDRESS LATCH ENABLE/V_{PP}
N.C.	NO CONNECT
D.U.	DON'T USE

87C64	87C257
V_{PP}	ALE/V_{PP}
A_{12}	A_{12}
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0
O_0	O_0
O_1	O_1
O_2	O_2
Gnd	Gnd



87C257	87C64
V_{CC}	V_{CC}
A_{14}	$\overline{PGM}$
A_{13}	N.C.
A_8	A_8
A_9	A_9
A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}
$\overline{CE}$	ALE/$\overline{CE}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

Figure 2. DIP Pin Configuration

NOTE:
Intel "Universal Site"-Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent.

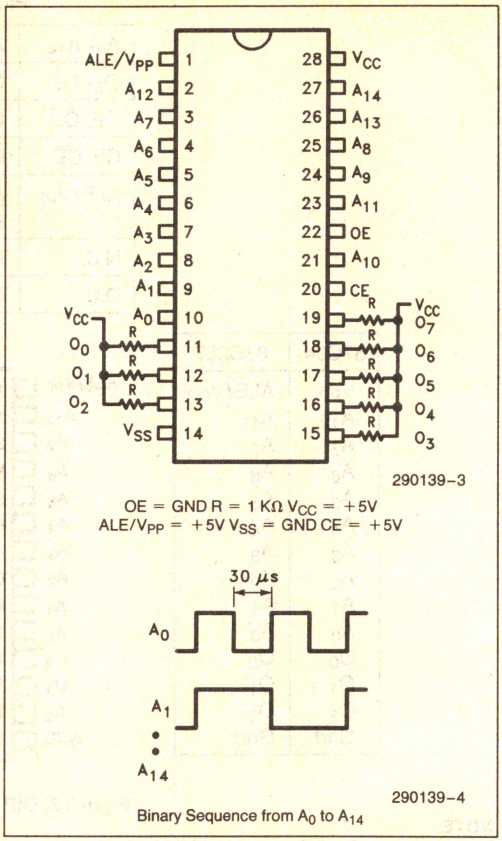
EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several EPROM densities allowing the appropriate memory size to match system applications. EXPRESS EPROMs are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process meets or exceeds most industry burn-in specifications. The standard EXPRESS EPROM operating temperature range is 0°C to +70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS and automotive temperature range (−40°C to +125°C) products are also available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

AUTOMOTIVE AND EXPRESS OPTIONS

Versions

Speed Versions	Packaging Options
	Cerdip
−200V05	A
−250V10	A
−250V05	A



Burn-In Bias and Timing Diagrams

AUTOMOTIVE AND EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ±8
A	−40°C to +125°C	NONE
B	−40°C to +125°C	168 ±8

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to + 70°C(2)
Temperature Under Bias ..... −10°C to +80°C(2)
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with Respect to Ground ..... −2V to +7V(1)
Voltage on A_9 with Respect to Ground ..... −2V to +13.5V(1)
V_{PP} Supply Voltage with Respect to Ground During Programming ..... −2V to +14.0V(1)
V_{CC} Supply Voltage with Respect to Ground ..... −2V to +7.0V(1)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS TTL and NMOS Inputs

Symbol	Parameter		Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby with Inputs—	Switching				10	mA	CE = V_{IL}, ALE = V_{IH}
		Stable				1.0	mA	CE = ALE = V_{IL}
I_{CC1}	V_{CC} Current Active		5			30	mA	CE = ALE = V_{IH} f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply)		1	−0.5		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)			2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			2.4			V	I_{OH} = −400 µA
I_{OS}	Output Short Circuit Current		6			100	mA	

D.C. CHARACTERISTICS CMOS Inputs

Symbol	Parameter		Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby with Inputs—	Switching	4			6	mA	CE = GND, ALE = V_{CC}
		Stable				100	µA	CE = ALE = GND
I_{CC1}	V_{CC} Current Active		5			15	mA	CE = ALE = V_{IH} f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply)			−0.2		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)			0.7 V_{CC}		V_{CC} + 0.2	V	
V_{OL}	Output Low Voltage					0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			V_{CC} − 0.8			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. CE and ALE are ±0.2V. All other inputs can have any value within spec.
5. Maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.

READ OPERATION

A.C. CHARACTERISTICS[1] $0°C \le T_A \le +70°C$

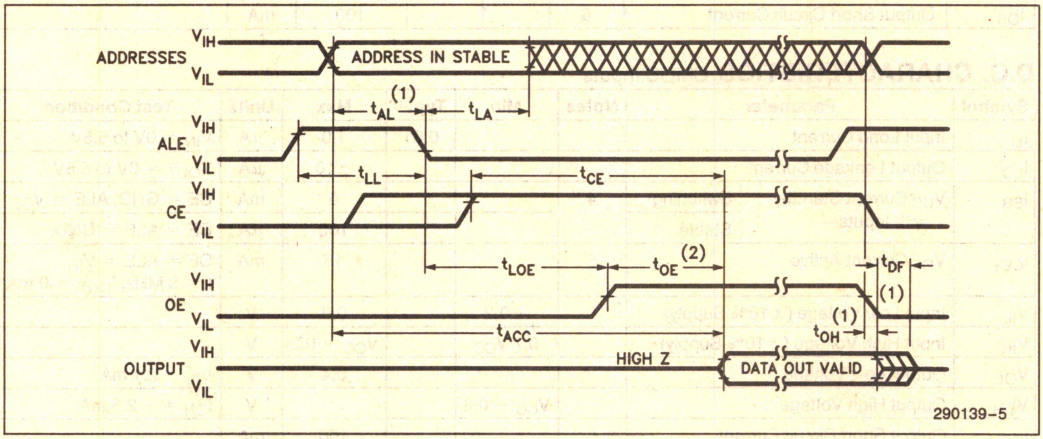
Versions[3]		$V_{CC} \pm 5\%$	68C257-170V05		68C257-200V05		68C257-250V05		Unit
		$V_{CC} \pm 10\%$			68C257-200V10		68C257-250V10		
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			170		200		250	ns
t_{CE}	CE to Output Delay			170		200		250	ns
t_{OE}	OE to Output Delay			70		75		100	ns
t_{DF}[2]	OE Low to Output High Z			35		40		55	ns
t_{OH}[2]	Output Hold from Addresses, CE or OE Change-Whichever is First		0		0		0		ns
t_{LL}	Latch Deselect Width		35		55		60		ns
t_{AL}[2]	Address to Latch Set-Up		7		15		25		ns
t_{LA}	Address Hold from LATCH		20		30		40		ns
t_{LOE}	ALE to Output Enable		20		30		40		ns

NOTES:
1. See A.C. Testing Input/Output Waveforms for timing measurements.
2. Guaranteed and sampled.
3. Model Number Prefixes: No Prefix = CERDIP.

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... V_{OL} to V_{OH}
Input Timing Reference Level 1.5V
Output Timing Reference Level ..... V_{IL} and V_{IH}

A.C. WAVEFORMS



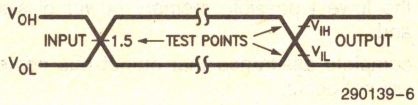
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. OE may be delayed up to $t_{CE} - t_{OE}$ after the rising edge of CE without impact on t_{CE}.

CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

NOTE:
1. Sampled. Not 100% tested.

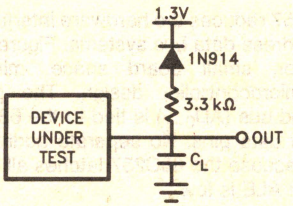
A.C. TESTING INPUT/OUTPUT WAVEFORM



290139-6

A.C. testing inputs are driven at V_{OH} for a Logic "1" and V_{OL} for a Logic "0". Timing measurements are made at V_{IH} for a Logic "1" and V_{IL} for a Logic "0".

A.C. TESTING LOAD CIRCUIT



290139-7

C_L = 100 pF
C_L Includes Jig Capacitance

DEVICE OPERATION

Table 1 lists 68C257 operating modes. Read mode requires a single 5V power supply. All input levels are TTL or CMOS except A9 in int$_e$ligent Identifier mode and V_{PP}.

Table 1. Mode Selection

Mode \ Pins	CE	OE	A_9	A_0	ALE/V_{PP}	V_{CC}	Outputs
Read	V_{IH}	V_{IH}	X(1)	X	X	5.0V	D_{OUT}
Output Disable	V_{IH}	V_{IL}	X	X	X	5.0V	High Z
Standby	V_{IL}	X	X	X	X	5.0V	High Z
Programming(5)	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify(5)	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{OUT}
Optional Program Verify	V_{IH}	V_{IH}	X	X	V_{CC} (Note 4)	(Note 4)	D_{OUT}
Program Inhibit(5)	V_{IH}	V_{IH}	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier(3, 5) -Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	X	V_{CC}	89 H
int$_e$ligent Identifier(3, 5) -68C257	V_{IL}	V_{IL}	V_H(2)	V_{IH}	X	V_{CC}	27 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ±0.5V.
3. A_1–A_8, A_{10-12} = V_{IL}, A_{13-14} = X.
4. See Table 2 for V_{CC} and V_{PP} programming voltages.
5. During Int$_e$ligent Identifier Mode (A_9 = V_H) and Programming Modes (ALE/V_{PP} = 12.75V), CE and OE default to active-low enables.

Read Mode

The 68C257 has two control functions; both must be logically active to obtain data at the outputs. Chip Enable (CE) is the power control and the device-select. Output enable (OE) gates data to the output pins by controlling the output buffer. When the address is stable (ALE = V_{IH}) or latched (ALE = V_{IL}), the address access time (t_{ACC}) equals the delay from CE to output (t_{CE}). Outputs display valid data t_{OE} after the rising edge of OE, assuming t_{ACC} and t_{CE} times are met.

The 68C257 reduces the hardware interface in multiplexed address-data bus systems. Figure 4 shows a low power, small board space, minimal chip 68C257/microcontroller design. The processor's multiplexed bus (AD_{0-7}) is tied to the 68C257's address and data pins. No separate address latch is needed because the 68C257 latches all address inputs when ALE is low.

The ALE input controls the 68C257's internal address latch. As ALE transitions from V_{IH} to V_{IL}, the last address present at the address pins is retained. The OE control can then enable EPROM data onto the bus.

The 68C257 is ideal for systems with program memory at high-address locations. Address decoders and "glue" chips can be eliminated by simply tying address line A_{15} to the active-high CE. The 68C257's active-high OE input connects directly to a 68-family microcomputer's active-high READ strobe ("E" clock output).

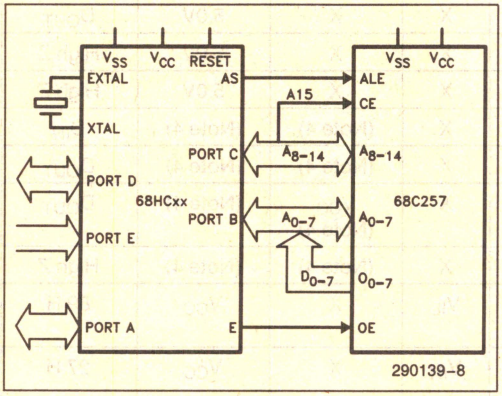


Figure 4. A Typical Microcomputer/68C257 System Configuration

Standby Mode

The standby mode substantially reduces V_{CC} current. When CE = V_{IL}, the standby mode places the outputs in a high impedance state, independent of the OE input.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two contol inputs to accommodate multiple memory connections. Two-line control provides for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder should enable CE, while OE should be connected to all memory-array devices and the system's active-high READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in low-power standby mode.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in three supply current (ICC) issues—standby current levels, active current levels, and transient current peaks produced by falling and rising edges of Chip Enable. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed between V_{CC} and GND at the array's power supply connection. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word

can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

The programming mode is entered when V_{PP} is raised to its programming voltage (see Table 2). Data is programmed by applying an 8-bit word to the output pins (O_{0-7}). Pulsing CE to TTL-low while OE = V_{IH} will program data. TTL levels are required for address and data inputs.

To simplify programming, CE and OE inputs default to active-low (as opposed to read modes active-high) enables when either $A_9 = V_H$ or ALE/V_{PP} is at its programming voltage (12.75V). This allows programming equipment to identify the 68C257 and program it with a standard programming algorithm. The 68C257 uses the same programming algorithm as the 87C257. Programming equipment that programs one device can also program its counterpart.

Program Inhibit

The Program Inhibit mode allows parallel programming of multiple EPROMs with different data. With V_{PP} at its programming voltage, a CE-low pulse programs the desired EPROM. CE-high inputs inhibit programming of non-targeted devices. Except for CE and OE, parallel EPROMs may have common inputs.

Program Verify

With V_{PP} and V_{CC} at their programming voltages, a verify (read) determines that bits are correctly programmed. The verify is performed with CE = V_{IH} and OE = V_{IL}. Valid data is available t_{OE} after OE falls low.

Optional Program Verify

The optional verify allows parallel programming and verification when several devices share a common bus. It is performed with CE = OE = V_{IH} and V_{PP} = V_{CC} = 6.25V. The normal read mode is then used for program verify. Outputs will tri-state depending on OE and CE.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type. Programming equipment can automatically match a device with its proper programming algorithm.

This mode is activated when programming equipment forces 12V ±0.5V on the EPROM's A_9 address line. With A_1–A_8, A_{10}–A_{12} = V_{IL} (A_{13-14} are don't-care), address line A_0 = V_{IL} will present the manufacturer's code and A_0 = V_{IH} the device code (see Table 1). When $A_9 = V_H$, CE and OE default to active-low and ALE need not be toggled to latch each identifier address. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

Exposure to light of wavelength shorter than 4000 Angstroms (Å) begins EPROM erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000–4000Å range. Constant exposure to room-level fluorescent light can erase an EPROM in about 3 years (about 1 week for direct sunlight). Opaque labels over the window will prevent unintentional erasure under these lighting conditions.

The recommended erasure procedure is exposure to 2537Å ultraviolet light. The minimum integrated dose (intensity x exposure time) is 15 Wsec/cm^2. Erasure time using a 12000 μW/cm^2 ultraviolet lamp is approximately 15 to 20 minutes. The EPROM should be placed about 1 inch from the lamp. The maximum integrated dose is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). High intensity UV light exposure for longer periods can cause permanent damage.

CHMOS NOISE CHARACTERISTICS

System reliability is enhanced by Intel's CHMOS EPI-process techniques. Protection on each data and address pin prevents latch-up; even with 100 mA currents and voltages from −1V to V_{CC} + 1V. Additionally, the V_{PP} pin is designed to resist latch-up to the 14V maximum device limit.

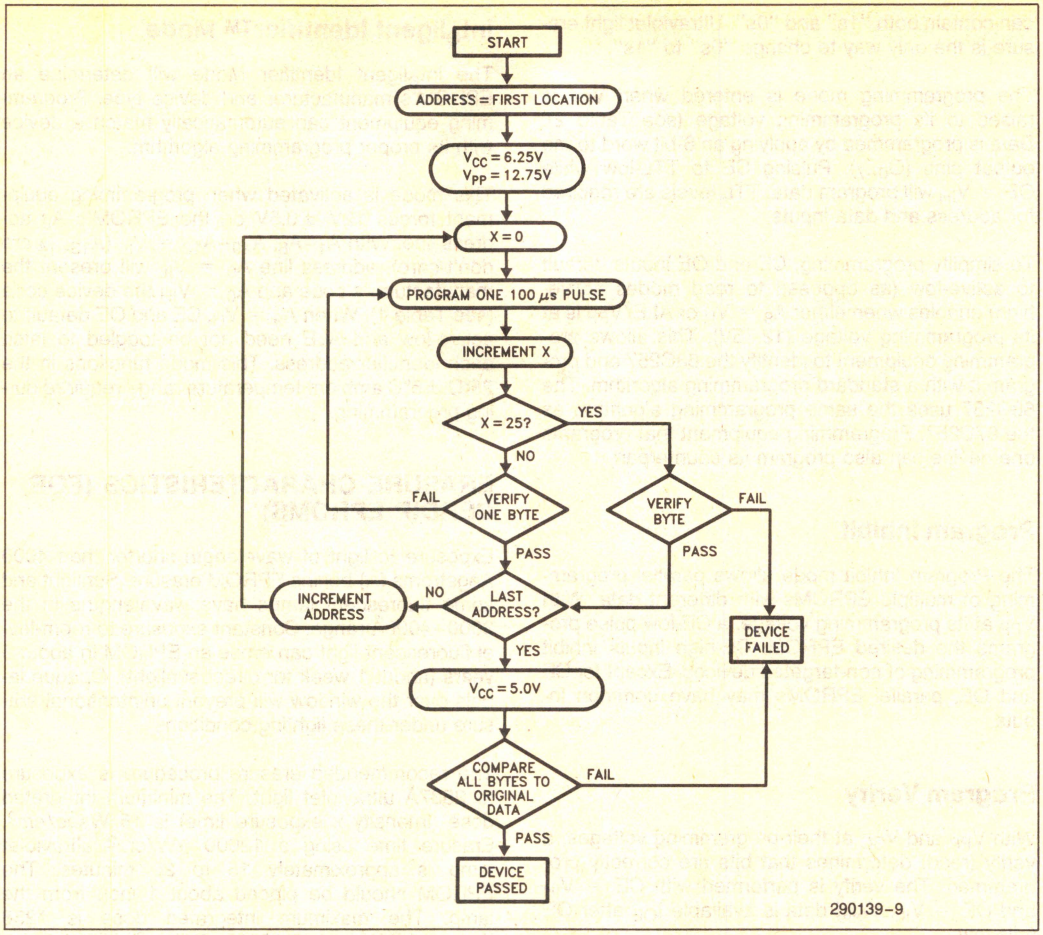


Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming algorithm programs Intel's 68C257 EPROM. Developed to substantially reduce production programming throughput time, this algorithm can program a 68C257 in under four seconds. Actual programming time depends on the PROM programmer used.

The Quick-Pulse Programming algorithm uses a 100 microsecond initial-pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100μs pulses fail to program a byte. Figure 5 shows the Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/byte-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. When programming is complete, all bytes should be compared to the original data with V_{CC} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.2	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	$V_{CC} - 0.8$		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current		30	mA	
I_{PP2}(3)	V_{PP} Supply Current (Program)		50	mA	$CE = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}(1)	Programming Voltage	12.5	13.0	V	
V_{CC}(1)	Supply Voltage During Programming	6.0	6.5	V	

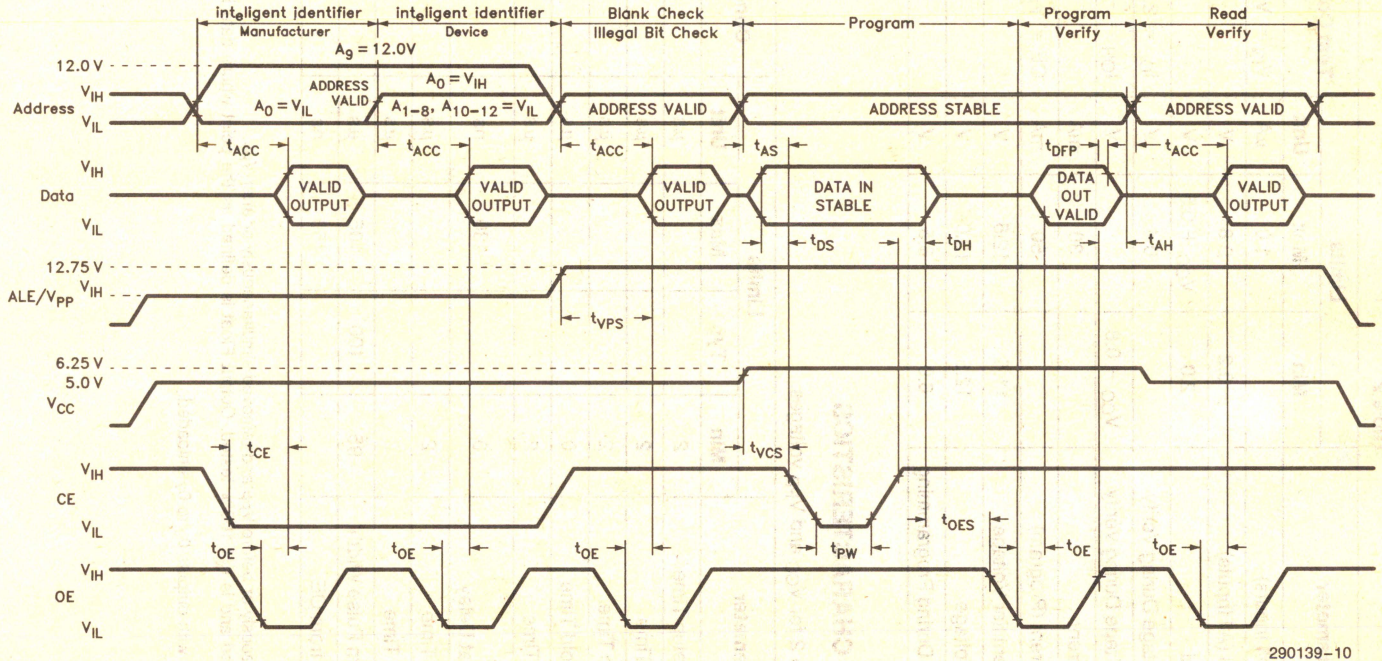
A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$; see Table 2 for V_{CC} and V_{PP} voltages.

Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	OE Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}(2)	OE High to Output Float Delay	0		130	ns	
t_{VPS}(1)	V_{PP} Setup Time	2			μs	
t_{VCS}(1)	V_{CC} Setup Time	2			μs	
t_{PW}	CE Program Pulse Width	95	100	105	μs	
t_{OE}	Data Valid from OE			150	ns	

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:

1. The input timing reference level is V_{IL} = 0.8V and V_{IH} = 2V.
2. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
3. To prevent device damage during programming, a 0.1 μF capacitor is required between V_{PP} and ground to suppress spurious voltage transients.
4. During programming, the address latch function is bypassed whenever V_{PP} = 12.75V or $A_9 = V_H$. When V_{PP} and A_9 are at TTL levels, the address latch function is enabled, and the device functions in read mode.
5. V_{PP} can be 12.75V during Blank Check and Final Verify; if so, CE must be V_{IH}.

87C257
256K (32K x 8) CHMOS UV ERASABLE PROM

- **CHMOS/NMOS Microcontroller and Microprocessor Compatible**
  - **87C257-Integrated Address Latch**
  - **Universal 28 Pin Memory Site, 2-line Control**
- **Low Power Consumption**
- **High Performance Speeds**
  - **170 ns Maximum Access Time**
- **Noise Immunity Features**
  - **$\pm$10% V_{CC} Tolerance**
  - **Maximum Latch-up Immunity Through EPI Processing**
- **New Quick-Pulse Programming™ Algorithm**
  - **4 Second Programming**
- **Available in 28-Pin Cerdip Package**
  (See Packaging Spec., Order #231369)

Intel's 87C257 CHMOS EPROM is a 256K-bit 5V only memory organized as 32,768 8-bit words. It employs advanced CHMOS*II-E circuitry for systems requiring low power, high speed performance, and noise immunity. The 87C257 is optimized for compatibility with multiplexed address/data bus microcontrollers such as Intel's 16 MHz 8051- and 8096- families.

The 87C257 incorporates latches on all address inputs to minimize chip count, reduce cost, and simplify design of multiplexed bus systems. The 87C257's internal address latch allows address and data pins to be tied directly to the processor's multiplexed address/data pins. Address information (inputs A_0–A_{14}) is latched early in the memory-fetch cycle by the falling edge of the ALE input. Subsequent address information is ignored while ALE remains low. The EPROM can then pass data (from pins O_0–O_7) on the same bus during the last part of the memory-fetch cycle.

The 87C257 is offered in a ceramic DIP package, providing flexibility in prototyping and R&D environments. The 87C257 employs the Quick-Pulse Programming™ Algorithm for fast and reliable programming.

Intel's EPI processing achieves the highest degree of latch-up protection. Address and data pin latch-up prevention is provided for stresses up to 100 mA from -1V to V_{CC} + 1V.

*HMOS and CHMOS are patented processes of Intel Corporation.

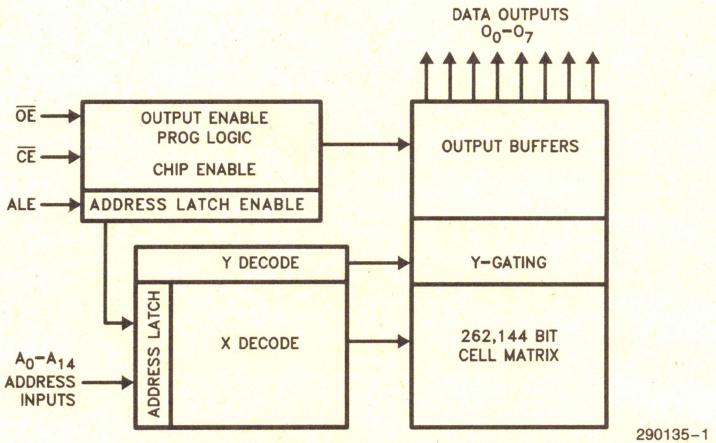


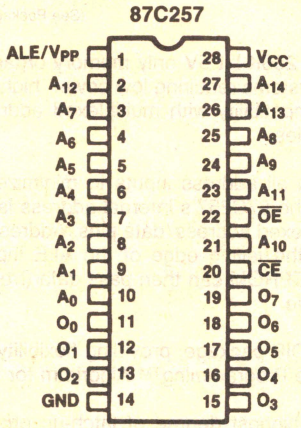
Figure 1. Block Diagram

October 1987
Order Number: 290135-002

Pin Names

A_0–A_{14}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
ALE/V_{PP}	Address Latch Enable/V_{PP}
N.C.	NO CONNECT

87C64
V_{PP}
A_{12}
A_7
A_6
A_5
A_4
A_3
A_2
A_1
A_0
O_0
O_1
O_2
Gnd



87C64
V_{CC}
$\overline{PGM}$
N.C
A_8
A_9
A_{11}
$\overline{OE}$
A_{10}
ALE/$\overline{CE}$
O_7
O_6
O_5
O_4
O_3

Figure 2. DIP Pin Configuration

NOTE:
Intel "Universal Site"-Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family receives additional processing to enhance product characteristics. EXPRESS processing is available for several EPROM densities allowing the appropriate memory size to match system applications. EXPRESS EPROMs are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process meets or exceeds most industry burn-in specifications. The standard EXPRESS EPROM operating temperature range is 0°C to +70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS and automotive temperature range (−40°C to +125°C) products are also available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

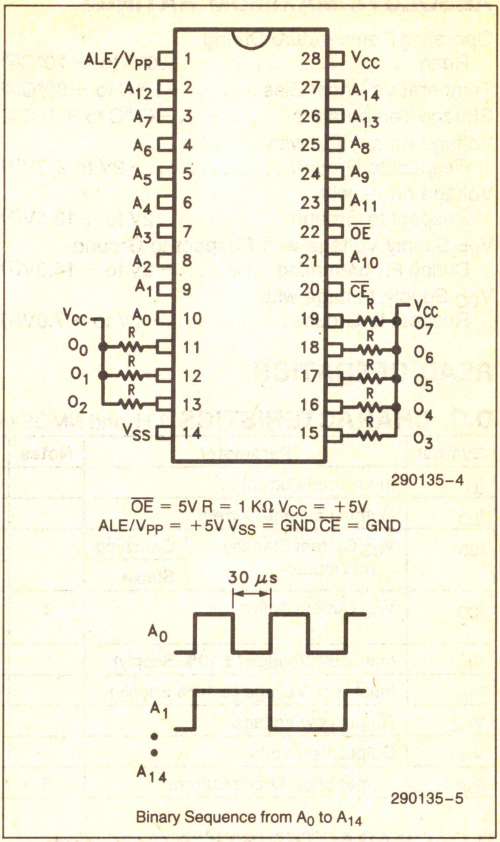
AUTOMOTIVE AND EXPRESS OPTIONS

Speed Versions	Packaging Options
	Versions
	Cerdip
−200V05	A
−250V10	A
−250V05	A

AUTOMOTIVE AND EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ±8
A	−40°C to +125°C	NONE
B	−40°C to +125°C	168 ±8



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to + 70°C(2)
Temperature Under Bias ..... −10°C to +80°C(2)
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with Respect to Ground ..... −2V to +7V(1)
Voltage on A_9 with Respect to Ground ..... −2V to +13.5V(1)
V_{PP} Supply Voltage with Respect to Ground During Programming ..... −2V to +14.0V(1)
V_{CC} Supply Voltage with Respect to Ground ..... −2V to +7.0V(1)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

D.C. CHARACTERISTICS TTL and NMOS Inputs

Symbol	Parameter		Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby with Inputs—	Switching				10	mA	$\overline{CE}$ = ALE = V_{IH}
		Stable				1.0	mA	$\overline{CE}$ = V_{IH}, ALE = V_{IL}
I_{CC_1}	V_{CC} Current Active		5			30	mA	$\overline{CE}$ = V_{IL}, ALE = V_{IH} f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply)		1	−0.5		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)			2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			2.4			V	I_{OH} = −400 µA
I_{OS}	Output Short Circuit Current		6			100	mA	

D.C. CHARACTERISTICS CMOS Inputs

Symbol	Parameter		Notes	Min	Typ(3)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	µA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	µA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby with Inputs—	Switching	4			6	mA	$\overline{CE}$ = ALE = V_{CC}
		Stable				100	µA	$\overline{CE}$ = V_{CC}, ALE = GND
I_{CC_1}	V_{CC} Current Active		5			15	mA	$\overline{CE}$ = V_{IL}, ALE = V_{IH} f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply)			−0.2		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)			0.7 V_{CC}		V_{CC} + 0.2	V	
V_{OL}	Output Low Voltage					0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			V_{CC} − 0.8			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Automotive versions.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within spec.
5. Maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.

READ OPERATION

A.C. CHARACTERISTICS(1) $0°C \le T_A \le +70°C$

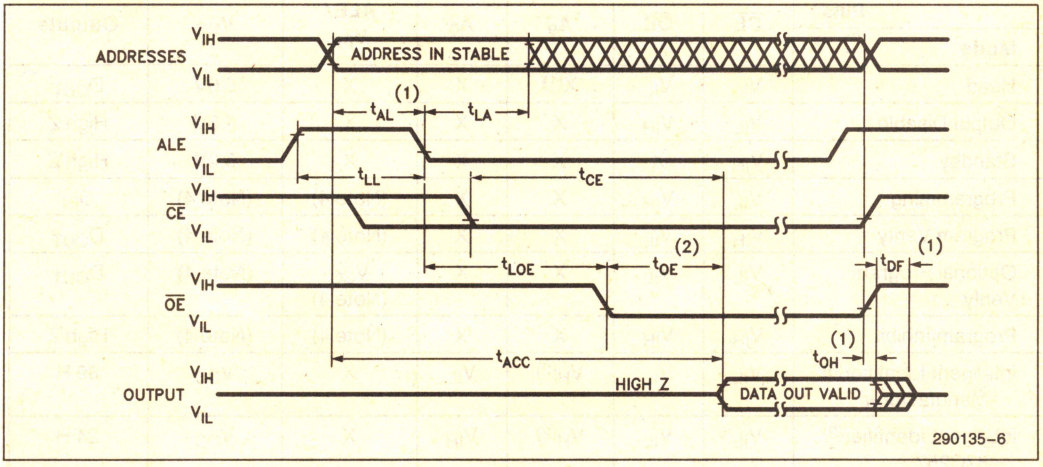
Versions(3)		$V_{CC} \pm 5\%$	87C257-170V05		87C257-200V05		87C257-250V05		Units
		$V_{CC} \pm 10\%$			87C257-200V10		87C257-250V10		
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay			170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay			70		75		100	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z			35		40		55	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First		0		0		0		ns
t_{LL}	Latch Deselect Width		35		55		60		ns
t_{AL}(2)	Address to Latch Set-Up		7		15		25		ns
t_{LA}	Address Hold from LATCH		20		30		40		ns
t_{LOE}	ALE to Output Enable		20		30		40		ns

NOTES:
1. See A.C. Testing Input/Output Waveforms for timing measurements.
2. Guaranteed and sampled.
3. Model Number Prefixes: No Prefix = CERDIP.

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... V_{OL} to V_{OH}
Input Timing Reference Level 1.5V
Output Timing Reference Level ..... V_{IL} and V_{IH}

A.C. WAVEFORMS



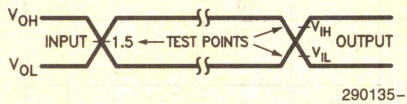
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE[1] T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

NOTE:
1. Sampled. Not 100% tested.

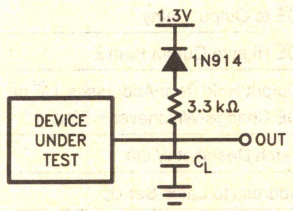
A.C. TESTING INPUT/OUTPUT WAVEFORM



290135-7

A.C. testing inputs are driven at V_{OH} for a Logic "1" and V_{OL} for a Logic "0". Timing measurements are made at V_{IH} for a Logic "1" and V_{IL} for a Logic "0".

A.C. TESTING LOAD CIRCUIT



290135-8

C_L = 100 pF
C_L Includes Jig Capacitance

DEVICE OPERATION

Table 1 lists 87C257 operating modes. Read mode requires a single 5V power supply. All input levels are TTL or CMOS except A9 in int$_e$ligent Identifier mode and V_{PP}.

Table 1. Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	A_9	A_0	ALE/V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X[1]	X	X	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{OUT}
Optional Program Verify	V_{IL}	V_{IL}	X	X	V_{CC} (Note 4)	(Note 4)	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier[3] -Manufacturer	V_{IL}	V_{IL}	V_H[2]	V_{IL}	X	V_{CC}	89 H
int$_e$ligent Identifier[3] -87C257	V_{IL}	V_{IL}	V_H[2]	V_{IH}	X	V_{CC}	24 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ±0.5V.
3. A_1–A_8, A_{10-12} = V_{IL}, A_{13-14} = X.
4. See Table 2 for V_{CC} and V_{PP} programming voltages.

Read Mode

The 87C257 has two control functions; both must be logically active to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and the device-select. Output enable ($\overline{OE}$) gates data to the output pins by controlling the output buffer. When the address is stable (ALE = V_{IH}) or latched (ALE = V_{IL}), the address access time (t_{ACC}) equals the delay from $\overline{CE}$ to output (t_{CE}). Outputs display valid data t_{OE} after the falling edge of $\overline{OE}$, assuming t_{ACC} and t_{CE} times are met.

The 87C257 reduces the hardware interface in multiplexed address-data bus systems. Figure 4 shows a low power, small board space, minimal chip 87C257/microcontroller design. The processor's multiplexed bus (AD_{0-7}) is tied to the 87C257's address and data pins. No separate address latch is needed because the 87C257 latches all address inputs when ALE is low.

The ALE input controls the 87C257's internal address latch. As ALE transitions from V_{IH} to V_{IL}, the last address present at the address pins is retained. The $\overline{OE}$ control can then enable EPROM data onto the bus.

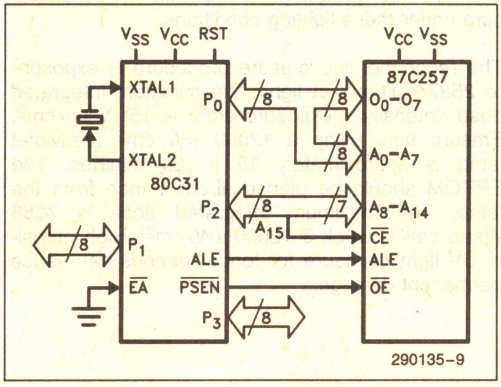


Figure 4. 80C31 with 87C257 System Configuration

Standby Mode

The standby mode substantially reduces V_{CC} current. When $\overline{CE}$ = V_{IH}, the standby mode places the outputs in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two contol inputs to accommodate multiple memory connections. Two-line control provides for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory-array devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in low-power standby mode.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in three supply current (ICC) issues—standby current levels, active current levels, and transient current peaks produced by falling and rising edges of Chip Enable. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed between V_{CC} and GND at the array's power supply connection. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word

can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

The programming mode is entered when V_{PP} is raised to its programming voltage (see Table 2). Data is programmed by applying an 8-bit word to the output pins (O_{0-7}). Pulsing $\overline{CE}$ to TTL-low while $\overline{OE} = V_{IH}$ will program data. TTL levels are required for address and data inputs.

Program Inhibit

The Program Inhibit mode allows parallel programming of multiple EPROMs with different data. With V_{PP} at its programming voltage, a $\overline{CE}$-low pulse programs the desired EPROM. $\overline{CE}$-high inputs inhibit programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

Program Verify

With V_{PP} and V_{CC} at their programming voltages, a verify (read) determines that bits are correctly programmed. The verify is performed with $\overline{CE} = V_{IH}$ and $\overline{OE} = V_{IL}$. Valid data is available t_{OE} after $\overline{OE}$ falls low.

Optional Program Verify

The optional verify allows parallel programming and verification when several devices share a common bus. It is performed with $\overline{CE} = \overline{OE} = V_{IL}$ and $V_{PP} = V_{CC} = 6.25V$. The normal read mode is then used for program verify. Outputs will tri-state depending on $\overline{OE}$ and $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type. Programming equipment can automatically match a device with its proper programming algorithm.

This mode is activated when programming equipment forces 12V ±0.5V on the EPROM's A_9 address line. With A_1-A_8, $A_{10}-A_{12} = V_{IL}$ (A_{13-14} are don't care), address line $A_0 = V_{IL}$ will present the manufacturer's code and $A_0 = V_{IH}$ the device code (see Table 1). When $A_9 = V_H$, ALE need not be toggled to latch each identifier address. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

Exposure to light of wavelength shorter than 4000 Angstroms (Å) begins EPROM erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000–4000Å range. Constant exposure to room-level fluorescent light can erase an EPROM in about 3 years (about 1 week for direct sunlight). Opaque labels over the window will prevent unintentional erasure under these lighting conditions.

The recommended erasure procedure is exposure to 2537Å ultraviolet light. The minimum integrated dose (intensity x exposure time) is 15 Wsec/cm^2. Erasure time using a 12000 μW/cm^2 ultraviolet lamp is approximately 15 to 20 minutes. The EPROM should be placed about 1 inch from the lamp. The maximum integrated dose is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). High intensity UV light exposure for longer periods can cause permanent damage.

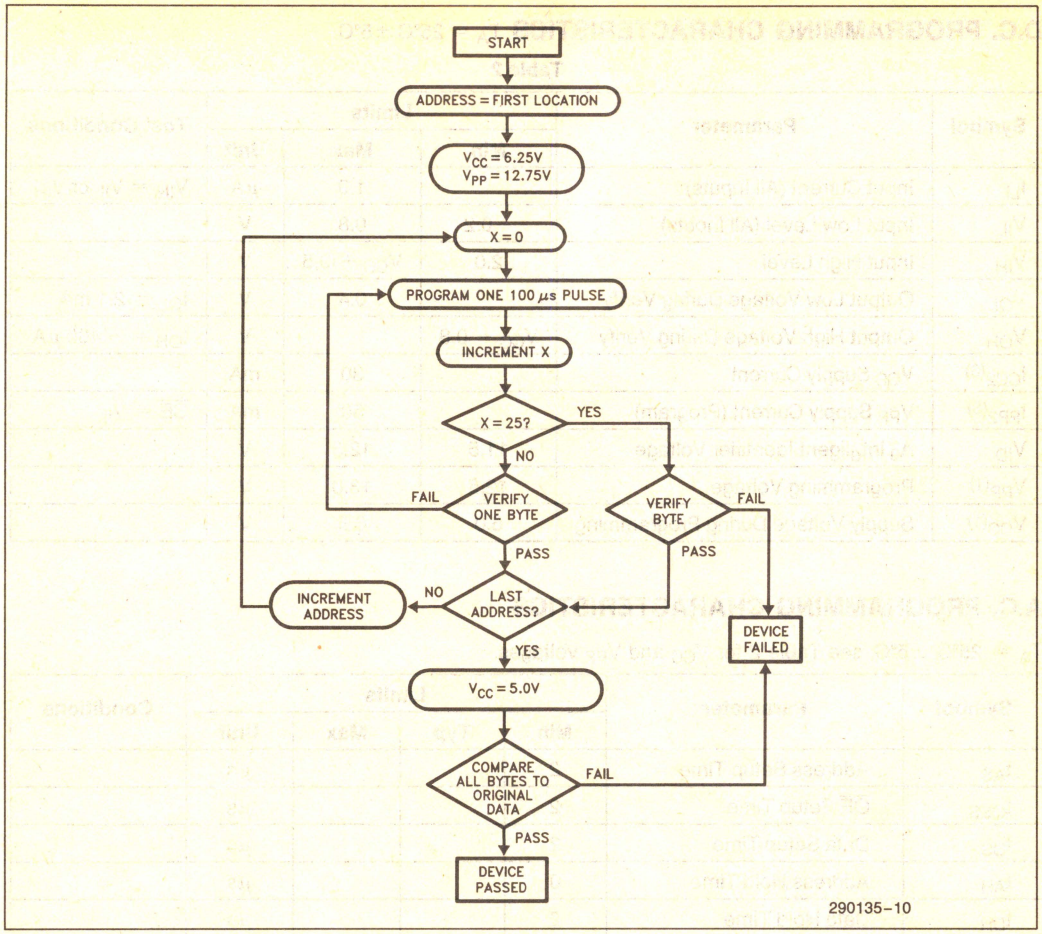


Figure 5. Quick-Pulse Programming™ Algorithm

CHMOS NOISE CHARACTERISTICS

System reliability is enhanced by Intel's CHMOS EPI-process techniques. Protection on each data and address pin prevents latch-up; even with 100 mA currents and voltages from $-1V$ to $V_{CC} + 1V$. Additionally, the V_{PP} pin is designed to resist latch-up to the 14V maximum device limit.

Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming algorithm programs Intel's 87C257 EPROM. Developed to substantially reduce production programming throughput time, this algorithm can program a 87C257 in under four seconds. Actual programming time depends on the PROM programmer used.

The Quick-Pulse Programming algorithm uses a 100 microsecond initial-pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100µs pulses fail to program a byte. Figure 5 shows the Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/byte-verify sequence is performed with $V_{CC} = 6.25V$ and $V_{PP} = 12.75V$. When programming is complete, all bytes should be compared to the original data with $V_{CC} = 5.0V$.

Alternate Programming

Intel's 27C256 and 27256 Quick-Pulse Programming algorithms will also program the 87C257. By overriding a check for the int$_e$ligent Identifier, older or non-upgraded PROM programmers can program the 87C257. See Intel's 27C256 and 27256 data sheets for programming waveforms of these alternate algorithms.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

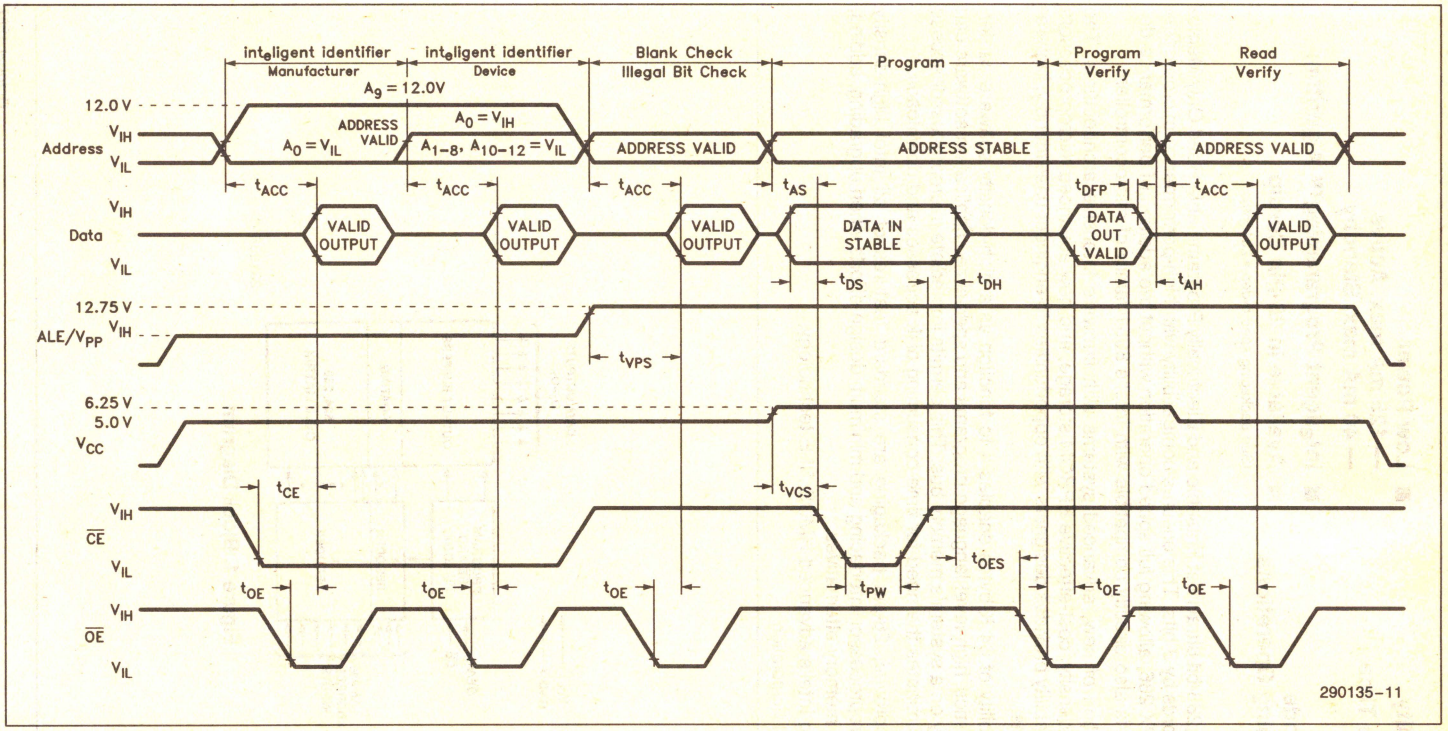
Symbol	Parameter	Limits			Test Conditions
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.2	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	$V_{CC} - 0.8$		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current		30	mA	
I_{PP2}(3)	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 inteligent Identifier Voltage	11.5	12.5	V	
V_{PP}(1)	Programming Voltage	12.5	13.0	V	
V_{CC}(1)	Supply Voltage During Programming	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$; see Table 2 for V_{CC} and V_{PP} voltages.

Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}(2)	$\overline{OE}$ High to Output Float Delay	0		130	ns	
t_{VPS}(1)	V_{PP} Setup Time	2			μs	
t_{VCS}(1)	V_{CC} Setup Time	2			μs	
t_{PW}	$\overline{CE}$ Program Pulse Width	95	100	105	μs	
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0 to O_7 unloaded.



NOTES:
1. The input timing reference level is V_{IL} = 0.8V and V_{IH} = 2V.
2. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
3. To prevent device damage during programming, a 0.1 μF capacitor is required between V_{PP} and ground to suppress spurious voltage transients.
4. During programming, the address latch function is bypassed whenever V_{PP} = 12.75V or $A_9 = V_H$. When V_{PP} and A_9 are at TTL levels, the address latch function is enabled, and the device functions in read mode.
5. V_{PP} can be 12.75V during Blank Check and Final Verify; if so, $\overline{CE}$ must be V_{IH}.

27512
512K (64K x 8) PRODUCTION AND UV ERASABLE PROM

- **Software Carrier Capability**
- **170 ns Maximum Access Time**
- **Two-Line Control**
- **int$_e$ligent Identifier™ Mode**
  — Automated Programming Operations
- **TTL Compatible**
- **Low Power**
  — 125 mA max. Active
  — 40 mA max. Standby
- **int$_e$ligent Programming™ Algorithm**
- **Available in 28-Pin Cerdip**
  (See packaging spec order #231369)

The Intel 27512 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K words by 8 bits. This ensures compatibility with high-performance microprocessors, such as the Intel 8 MHz iAPX 286, allowing full speed operation without the addition of performance-degrading WAIT states. The 27512 is also directly compatible with Intel's 8051 family of microcontrollers.

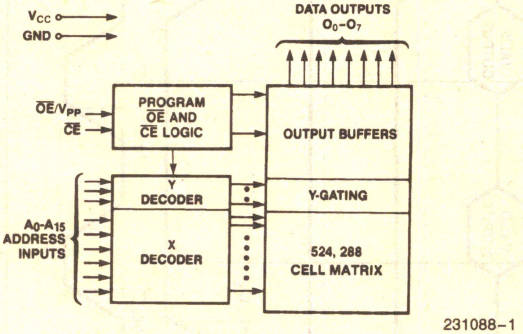
The 27512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27512's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabyte addressing capability provides designers with opportunities to engineer user-friendly, high-reliability, high-performance systems.

The 27512's large storage capability of 64 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27512 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27512 is manufactured using Intel's advanced HMOS *II-E technology.

*HMOS is a patented process of Intel Corporation.



231088–1

Figure 1. Block Diagram

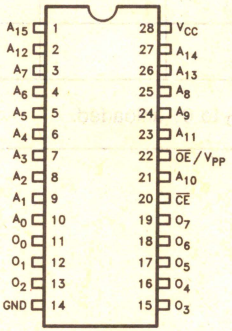
October 1987
Order Number: 231088-006

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Outputs Enable/V_{PP}
O_0–O_7	Outputs
D.U.	Don't Use

27513	27256 27C256 87C256	27128 27128A	2764 2764A 27C64 87C64
D.U.	V_{PP}	V_{PP}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
D_0/O_0	O_0	O_0	O_0
D_1/O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

27512



231088-2

2764 2764A 27C64 87C64	27128 27128A	27256 27C256 87C256	27513
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{PGM}$	A_{14}	$\overline{WE}$
N.C.	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$	$\overline{CE}$ ALE/$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

Figure 2. Pin Configurations

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hours, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27512 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-170V05	Q
-200V05, -200V10	Q, L
-STD, -25, -250V10	Q, T, L
-3, -30	Q, T, L

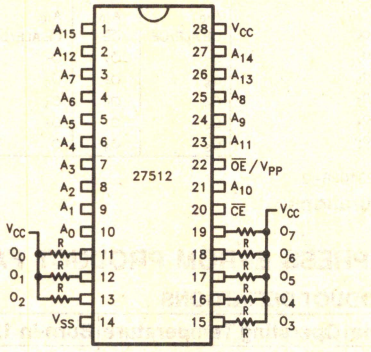
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

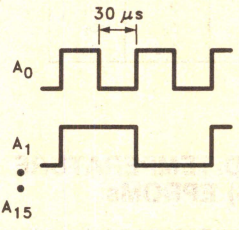
Symbol	Parameter	TD27512 LD27512		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE}/V_{PP} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		150	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



231088-3

$\overline{OE}/V_{PP}$ = +5V R = 1 KΩ V_{CC} = +5V
V_{SS} = GND $\overline{CE}$ = GND



231088-4

Binary sequence from A_0 to A_{15}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature during Read . . . . 0°C to 70°C
Temperature Under Bias . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . −0.6V to +6.5V
Voltage on Pin 24 with Respect to Ground . . . . . −0.6V to +13.5V
$\overline{OE}/V_{PP}$ Supply Voltage with Respect to Ground . . . . . −0.6V to +14.0V
V_{CC} Supply Voltage with Respect to Ground . . . . . −0.6V to +7.0V

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{SB}(4)	V_{CC} Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC_1}(4)	V_{CC} Current Active		90	125	mA	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

A.C. CHARACTERISTICS $0°C \leq T_A \leq +70°C$

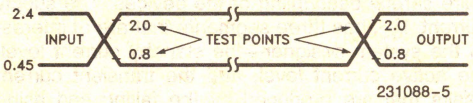
Versions(5, 6)	$V_{CC} \pm 5\%$	27512-170V05		27512-2 27512-200V05		27512 27512-250V05		27512-3		Units	Test Conditions
	$V_{CC} \pm 10\%$			27512-20 27512-200V10		27512-25		27512-30			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
t_{ACC}	Address to Output Delay		170		200		250		300	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		170		200		250		300	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay		60		75		100		120	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}/V_{PP}$ High to Output Float	0	50	0	55	0	60	0	105	ns	$\overline{CE} = V_{IL}$
t_{OH}(3)	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}/V_{PP}$ Whichever Occurred First	0		0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.
5. Packaging options: No prefix = Cerdip.
6. All products with the 6-digit speed identifier are produced on compacted HMOS II-E technology.

CAPACITANCE[2] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ[1]	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
$C_{\overline{OE}}/V_{PP}$	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	V_{IN} = 0V

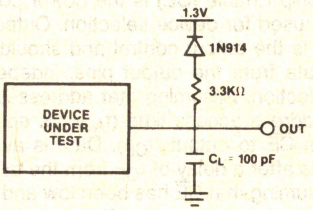
A.C. TESTING INPUT/OUTPUT WAVEFORM



231088-5

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

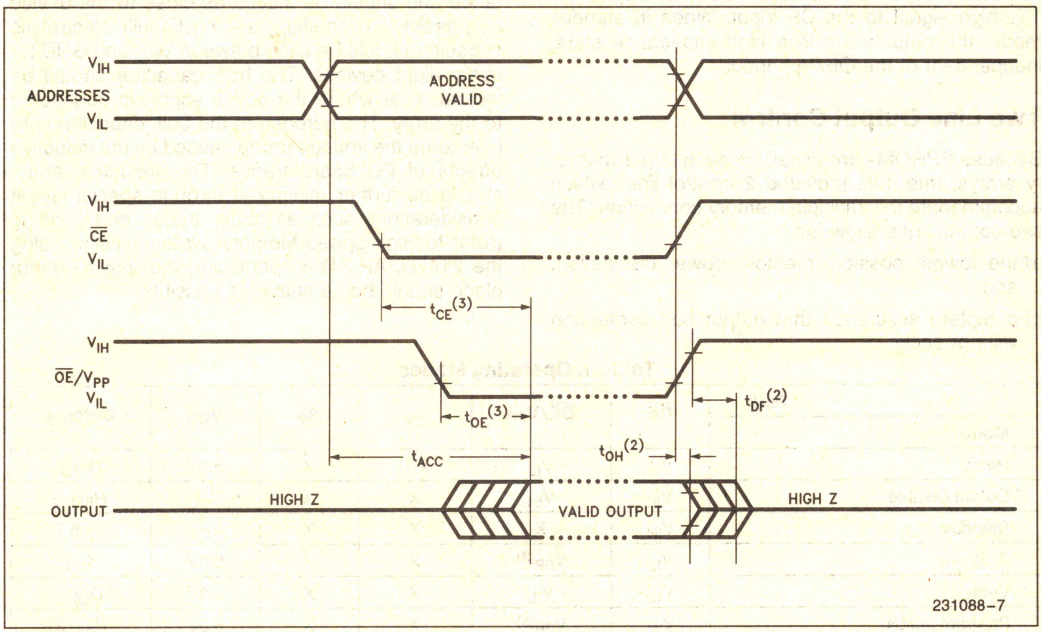
A.C. TESTING LOAD CIRCUIT



231088-6

C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS



231088-7

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27512 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for int$_e$ligent identifier mode.

Read Mode

The 27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The 27512 has a standby mode which reduces the maximum active current from 125 mA to 40 mA. The 27512 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	X	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}(3)	X	X	6.0V	D_{IN}
Verify	V_{IL}	V_{IL}	X	X	6.0V	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(3)	X	X	6.0V	High Z
Int$_e$ligent —Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	5.0V	89H
Identifier(4) —Device	V_{IL}	V_{IL}	V_H(2)	V_{IH}	5.0V	0DH

NOTES:
1. X can be V_{IH} or V_{IL}.
2. V_H = 12.0V ±0.5V.
3. V_{PP} = 12.5 ±0.5V.
4. A_1–A_8, A_{10}–A_{13} = V_{IL}; A_{14}, A_{15} = V_{IH}.

PROGRAMMING MODES

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ input is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 25712s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27512s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27512s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at its programming voltage will program the selected 27512.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode, except for A14 and A15 which should be held high.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

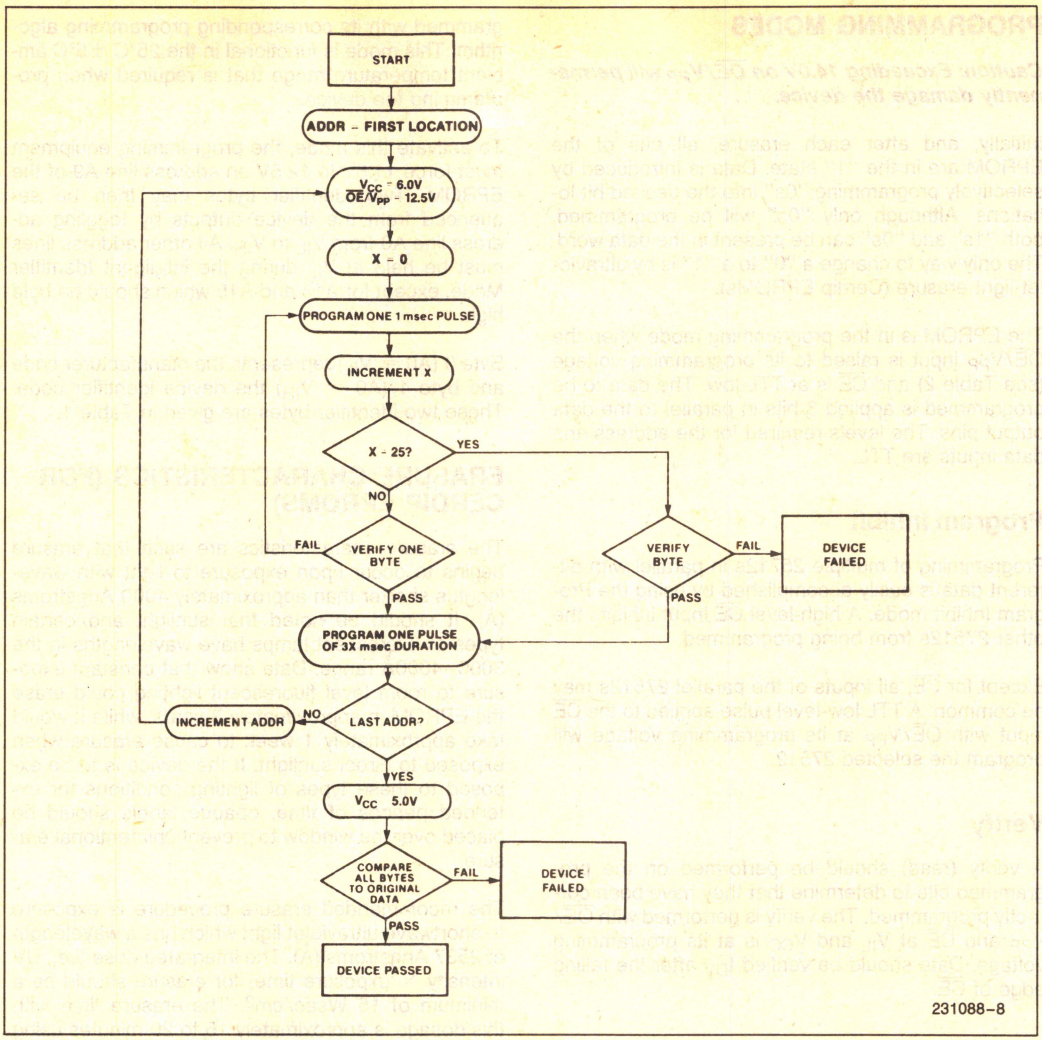


Figure 5. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm programs Intel EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming time for individual devices are on the order of six minutes. Actual programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 4.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied. ***The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V.*** When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5°C$

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(4)	V_{CC} Supply Current (Program & Verify)		125	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	intelligent Programming Algorithm	12.0	13.0	V	
V_{CC}	intelligent Programming Algorithm	5.75	6.25	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25 \pm 5°C$

Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 3)
t_{VCS}	V_{CC} Setup Time	2			μs	(Note 1)
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	intelligent Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			μs	
t_{DV}	Data Valid from $\overline{CE}$			1	μs	
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			μs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

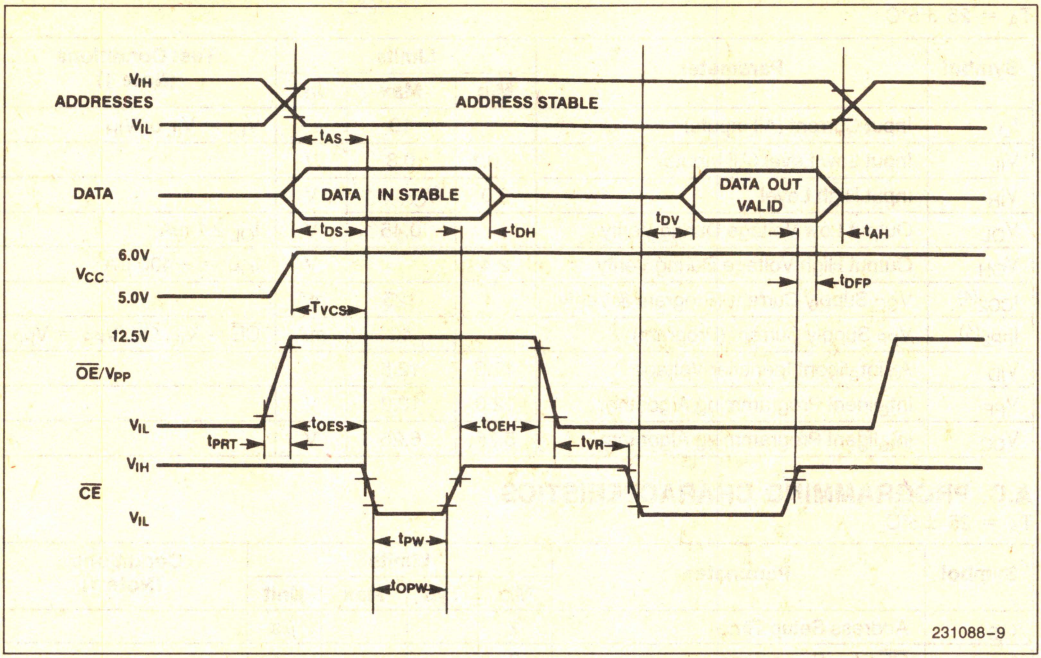
***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse (intelligent Programming Algorithm) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

27513
PAGE-ADDRESSED 512K (4 x 16K x 8) UV ERASABLE PROM

- **Paged Organization**
  - **— Reduced Physical Address Requirement**
  - **— No Bank Switching Logic Needed**
- **Software Carrier Capacity**
- **Automatic Page Clear**
  - **— Resets to Page 0 on Power Up and On Demand with $\overline{RST}$ Signal(1)**
- **TTL and CMOS Compatible**
- **170 ns Access Time**
- **Two Line Control**
- **Low Power**
  - **— 125 mA max. Active**
  - **— 40 mA max. Standby**
- **Compatible with Industry Standard EPROM Pinouts**
  - **— Direct 27128A Compatibility**
  - **— 28-Pin Cerdip**

The Intel 27513 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Memory. It is organized as 4 pages of 16K 8-bit words. The 27513's paged organization brings 64 K-byte storage capacity to existing 128K EPROM-based designs and to popular 8-bit microprocessor or microcontroller systems that have 64 K-byte total addressing capability. The 27513 provides an ideal means of quadrupling current 16 K-byte code space.

The 27513's large storage capability of 64 K-bytes and 170 ns access time enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27513 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

The 27513 has an automatic page clear circuit for ease of use of the page-addressed organization. The page-select latch is automatically cleared to the lowest order page upon system power up.

Two-line control and industry standard 28-pin packaging are features common to all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27513 is manufactured using Intel's Compacted HMOS* II technology.

NOTE:
1. $\overline{RST}$ feature only available on devices with 6-digit suffix.

November 1987
Order Number: 231113-006

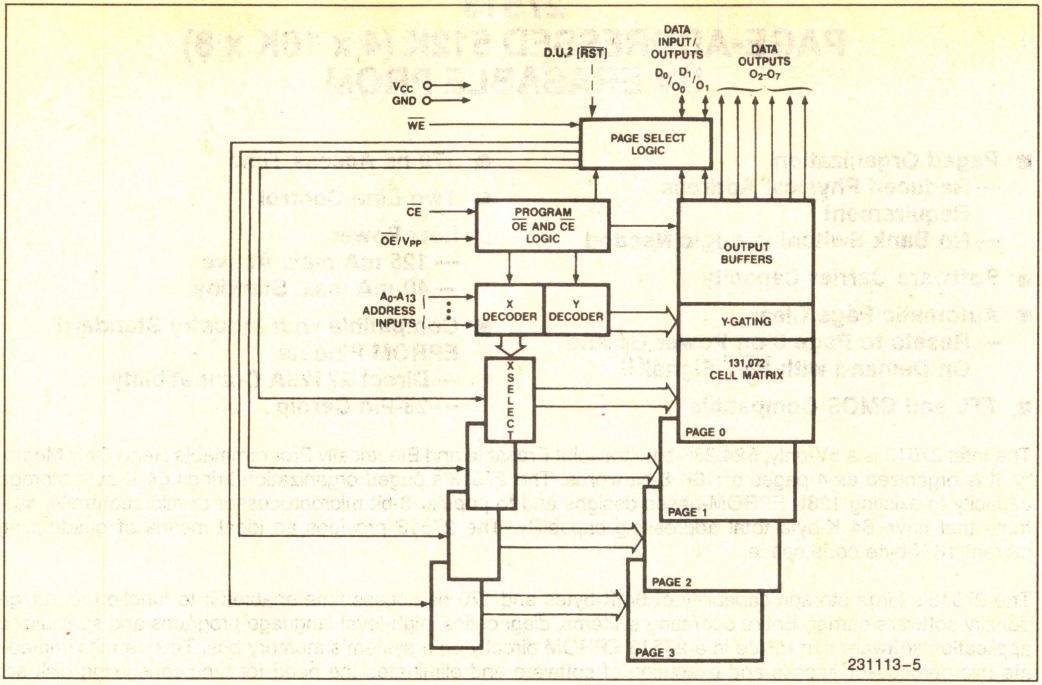
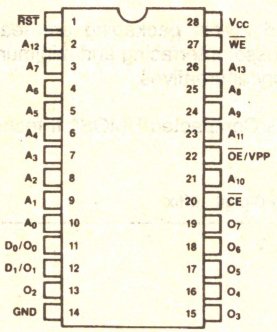


Figure 1. Block Diagram

2732A	2764A	27128A	27256	27512
	V_{PP}	V_{PP}	V_{PP}	A_{15}
	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27513



27512	27256	27128A	2764A	2732A
V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A_{14}	A_{14}	$\overline{PGM}$	$\overline{PGM}$	
A_{13}	A_{13}	A_{13}	N.C.	V_{CC}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. Pin Configuration

NOTES:
1. Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27513 pins.

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
$\overline{WE}$	Page-Select Write Enable
O_2–O_7	Outputs
D_0/O_0,D_1/O_1	Input/Outputs
$\overline{RST}$	Page Reset(1)

NOTE:
1. $\overline{RST}$ feature only available on devices with 6-digit suffix.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.15 electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27513 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-170V05	Q
-200V05, -200V10, -2	Q, L
-250V05, -250V10, -25, STD	Q, T, L

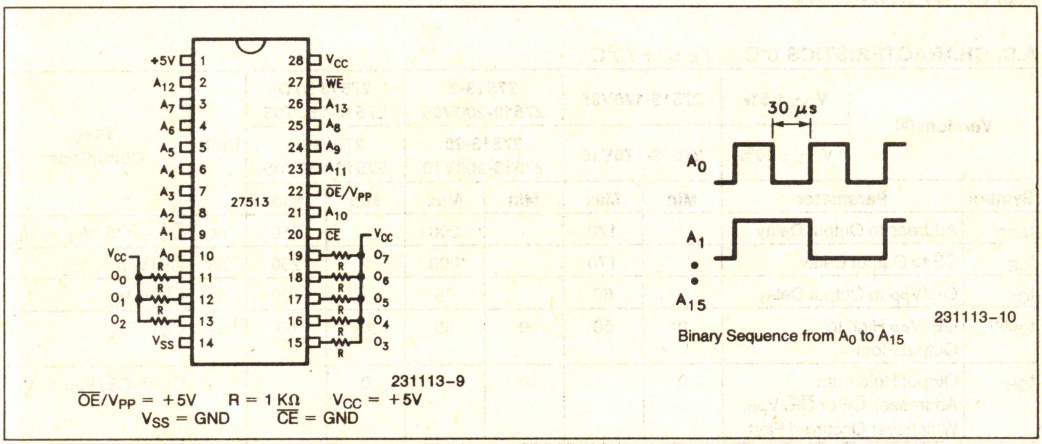
READ OPERATION

D.C. CHARACTERISTICS

Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27513 LD27513 Min	TD27513 LD27513 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE}/V_{PP} = V_{IL}$
I_{CC1} (1)	V_{CC} Active Current (mA)		150	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground† ..... −0.6V to +6.5V
Voltage on Pin 24 with
Respect to Ground ..... −0.6V to +13.5V
$\overline{OE}/V_{PP}$ Supply Voltage with
Respect to Ground ..... −0.6V to +14.0V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7.0V

† includes Don't Connect (pin 1)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ AND PAGE-SELECT WRITE OPERATIONS

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{SB}(4)	V_{CC} Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(4)	V_{CC} Current Active		90	125	mA	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage		3.5	4.0	V	

READ OPERATION

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions(5)		$V_{CC} \pm 5\%$	27513-170V05		27513-2 27513-200V05		27513 STD 27513-250V05		Units	Test Conditions
		$V_{CC} \pm 10\%$	27513-170V10		27513-20 27513-200V10		27513-25 27513-250V05			
Symbol	Parameter		Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay			170		200		250	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			170		200		250	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay			60		75		100	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}/V_{PP}$ High to Output Float		0	50	0	55	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}/V_{PP}$, Whichever Occurred First		0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

PAGE-SELECT WRITE AND PAGE-RESET OPERATION

A.C. CHARACTERISTICS

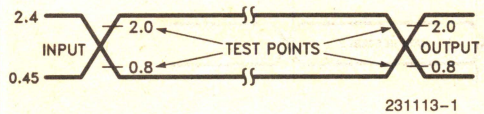
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	180		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE}/V_{PP} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time	55		ns	
t_{RST}	Reset Low Time	250		ns	
t_{RAV}	Reset to Address Valid	250		ns	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0–O_7 unloaded.
5. Packaging Options: No prefix = Cerdip; P = Plastic DIP; N = PLCC.
6. $\overline{RST}$ function is available only on parts with 6-digit suffix.

CAPACITANCE(2) $T_A = +25°C$, f = 1 MHz

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
$C_{\overline{OE}/V_{PP}}$	$\overline{OE}/V_{PP}$ Capacitance	18	25	pF	$V_{IN} = 0V$

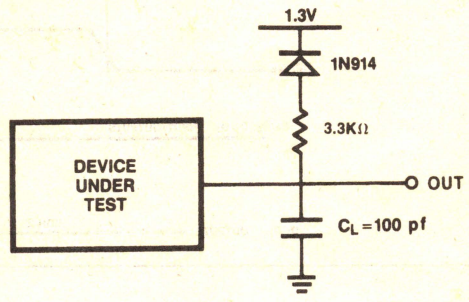
A.C. TESTING INPUT/OUTPUT WAVEFORM



231113-1

AC Testing inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

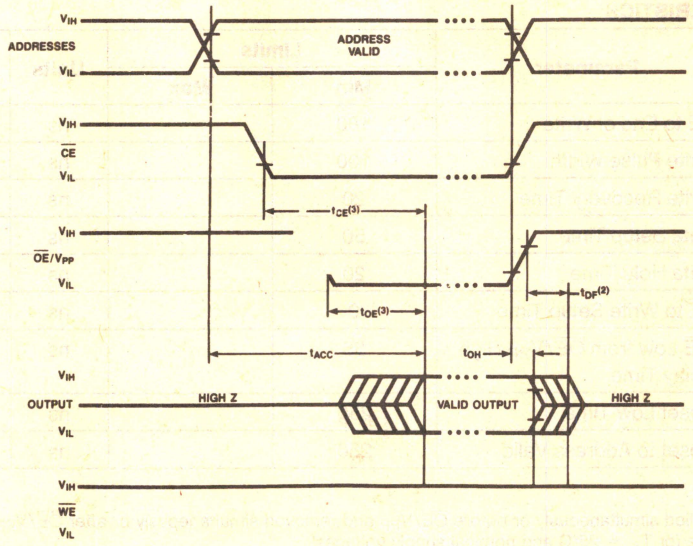
A.C. TESTING LOAD CIRCUIT



231113-2

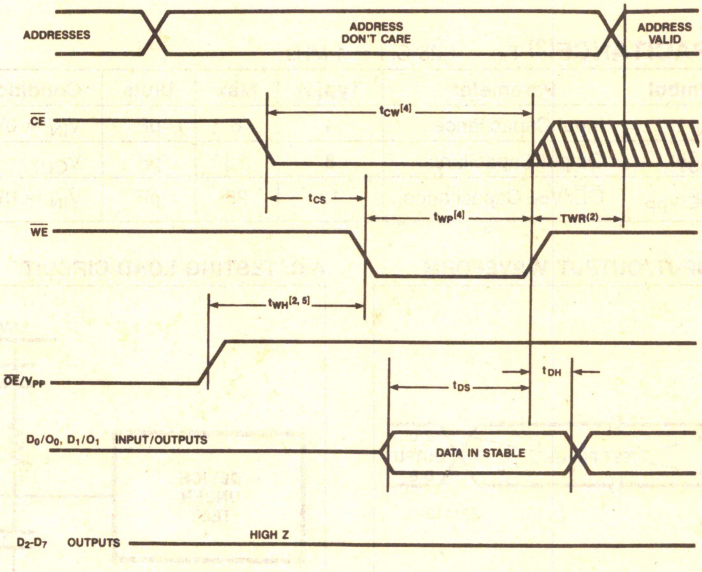
C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS FOR READ OPERATION



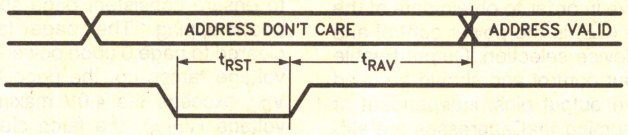
231113-3

A.C. WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



231113-4

A.C. WAVEFORMS FOR PAGE-RESET OPERATIONS



NOTES:
1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}/V_{PP}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27513 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for int$_e$ligent Identifier mode.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	$\overline{RST}$	A_9	A_0	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X(1)	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	V_{IH}	X	X	V_{CC}	High Z	High Z
Programming	V_{IL}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	(Note 3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}(3)	V_{IH}	V_{IH}	X	X	(Note 3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	V_{CC}(5)	High Z	Page(2) D_{IN}
Page-Reset	X	X	X	V_{IL}	X	X	V_{CC}(5)	High Z	X
int$_e$ligent(4) —Manufacturer Identifier —Device	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IL}	5.0V	89H	89H
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H(7)	V_{IH}	5.0V	0FH(6)	0FH(6)

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 2 for V_{CC} and V_{PP} voltages.
4. A_1-A_8, $A_{10}-A_{13}$, $= V_{IL}$.
5. Page 0 is automatically selected at power-up ($V_{CC} < 4.0V$).
6. 27513s before 2H/86 have a device identifier of 0DH. 27513s after 2H/86 will have a device identifier of 0FH.
7. $V_H = 12.0V \pm 0.5\%$.

Read Mode

The 27513 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. $\overline{WE}$ is held high during read operations.

Standby Mode

The 27513 has a standby mode which reduces the maximum active current from 125 mA to 40 mA. The 27513 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27513 is addressed by first selecting one of four 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0-A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0 and D_1/O_1. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output (Pin) Page Selection	D_1/O_1 (12)	D_0/O_0 (11)
Select Page 0	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IH}
Select Page 2	V_{IH}	V_{IL}
Select Page 3	V_{IH}	V_{IH}

Page Reset

The 27513 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case -10% V_{CC} supply condition) against spurious page latch clearing.

27513 parts with 6-digit suffixes also have a page reset pin: $\overline{RST}$. This pin should be tied to an active low system reset signal. These 27513s will be reset to page 0 when this line is brought to TTL Low (V_{IL}).

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27513s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by

properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ will permanently damage the 27513.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the $\overline{OE}/V_{PP}$ input is raised to its programming voltage (see Table 2) and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27513s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27513s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27513s may be common. A TTL low-level pulse applied to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at its programming voltage will program the selected 27513.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm (for plastic and PLCC EPROMs), the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPs makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intelec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

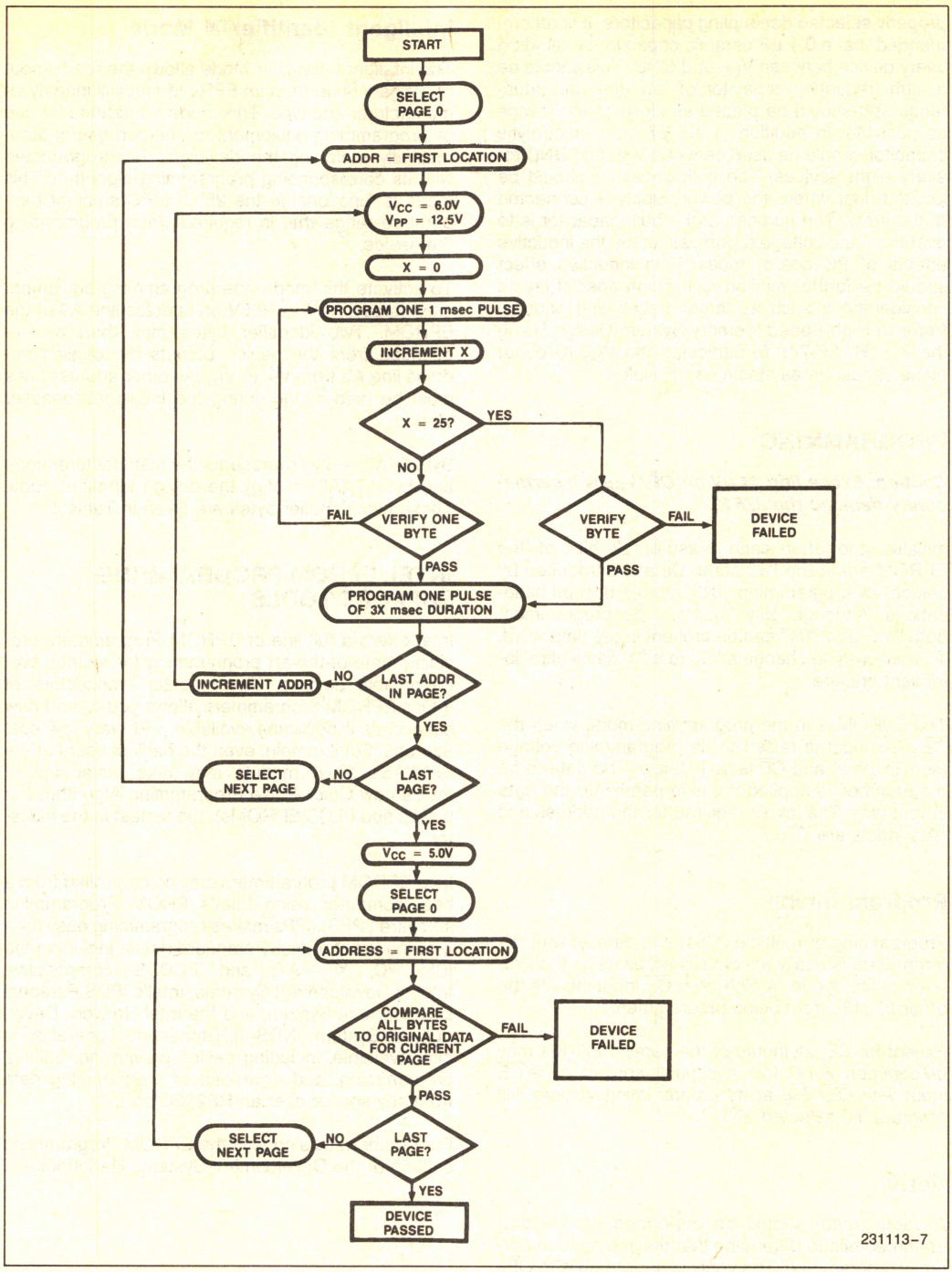


Figure 5. 27513 int$_e$ligent Programming™ Flowchart

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

int$_e$ligent Programming™ ALGORITHM

The int$_e$ligent Programming Algorithm programs Intel EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of six minutes. Actual Programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the 27513 int$_e$ligent Programming Algorithm is shown in Figure 3. The only difference between the 27513 and other EPROM int$_e$ligent Programming is that the 27513 is programmed one 16 K-byte page at a time.

TABLE 2. D.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400 μA
I_{CC2}(2)	V_{CC} Supply Current (Program and Verify)		125	mA	
I_{PP2}(2)	V_{PP} Supply Current (Program)		40	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PP}$
V_{ID}	A_9 int$_e$ligent Identifier Voltage	11.5	12.5	V	
V_{PP}	int$_e$ligent Programming Algorithm	12.0	13.0	V	
V_{CC}	int$_e$ligent Programming Algorithm	5.75	6.25	V	

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The maximum current value is with outputs O_0–O_7 unloaded.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied. ***The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V.*** When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

A.C. PROGRAMMING CHARACTERISTICS

T_A = 25°C ±5°C

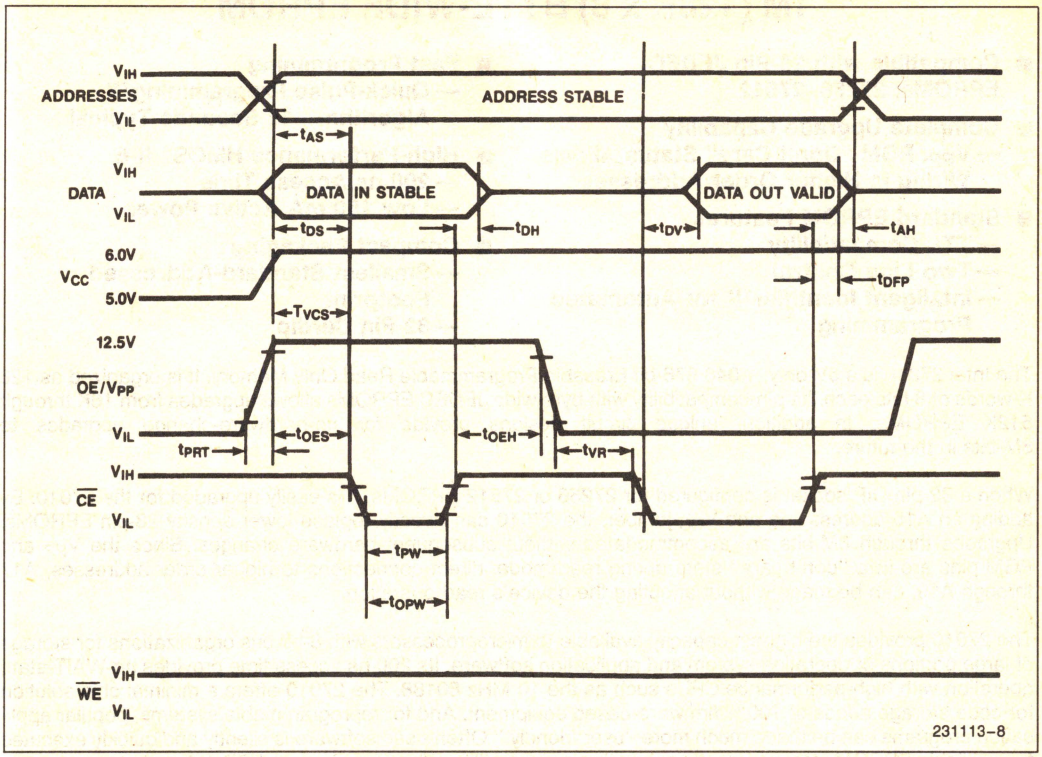
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	Output Enable to Output Float Delay	0		130	ns	(Note 3)
t_{VCS}	V_{CC} Setup Time	2			µs	(Note 1)
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms	int$_e$ligent Programming
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2			µs	
t_{DV}	Data Valid from $\overline{CE}$			1	µs	
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2			µs	
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	50			ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse (int$_e$ligent Programming Algorithm only) may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 K-byte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

27010
1M (128K x 8) BYTE-WIDE EPROM

- **Compatible with 28-Pin JEDEC EPROMs: 27256, 27512**
- **Complete Upgrade Capability**
  - **— V_{PP}, PGM "Don't Care" Status Allows Wiring in Higher Order Addresses**
- **Standard EPROM Features**
  - **— TTL Compatibility**
  - **— Two Line Control**
  - **— int$_e$ligent Identifier™ for Automated Programming**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm—15 Seconds Typical**
- **High-Performance HMOS* II-E**
  - **— 200 ns Access Time**
  - **— Low 150 mA Active Power**
- **Compact Packaging**
  - **— Smallest Standard-Addressed Footprint**
  - **— 32-Pin Cerdip**

The Intel 27010 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 128 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs allows upgrades from 16K through 512K EPROMs. In addition, unique circuit designs provide for no-hardware-change upgrades to 8M-bits in the future.

When a 32-pin DIP socket is configured for 27256 or 27512 EPROMs, it is easily upgraded for the 27010. By adding an A16 address line and V_{CC} jumper, the 27010 can directly replace lower density 28-pin EPROMs. Upgrades through 8M-bits are accommodated without subsequent hardware changes. Since the V_{PP} and PGM pins are in a "don't care" state during read mode, direct connections to higher order addresses, A17 through A19, can be made without affecting the device's read operation.

The 27010 provides the highest capacity available to microprocessors with 8-bit bus organizations for storage of large portions of operating system and application software. Its 200 ns access time provides no-WAIT-state operation with high-performance CPUs such as the 10 MHz 80188. The 27010 offers a minimal chip solution for code storage needs of 100% firmware-based equipment. And for reprogrammable systems, popular application programs can be made much more "user friendly." Often-used software is silently and quickly executed from reliable EPROM storage, greatly enhancing system utility. When two or more EPROM sockets are used in 16-bit or 32-bit systems, the compact 32-pin DIP package requires the smallest board space of any high density memory without utilizing paged or multiplexed addressing schemes.

The 27010 is part of a three-product megabit EPROM family. Other family members are the 27011 and 27210. The 8 x 16K x 8 27011 utilizes page-addressing, allowing "drop-in" replacement of the 512 K-bit 27513 and continued no-hardware-change upgrades to 32 M-bits in the same JEDEC-compatible 28-pin site. The 40-pin packaged 27210 is organized as 64K x 16, for systems in which word-wide memories are preferred.

The 27010 shares several features with standard JEDEC EPROMs, including two-line output control for simplified interfacing and the int$_e$ligent Identifier™ feature for automated programming. It can also be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 15 seconds.

The 27010 is manufactured using an advanced version of Intel's HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

November 1987
Order Number: 290105-003

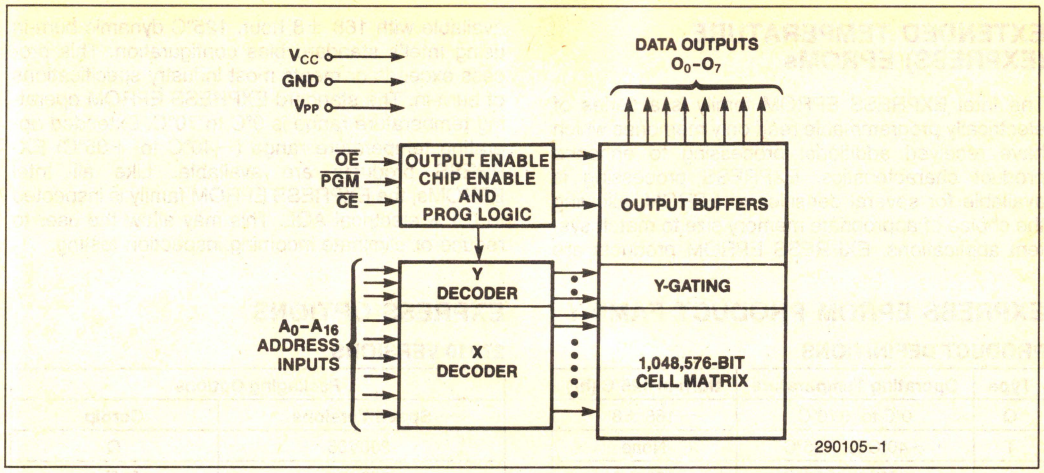


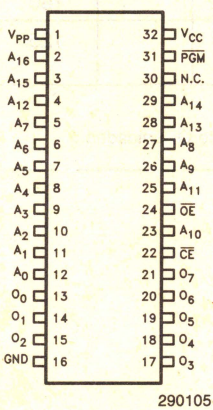
Figure 1. Block Diagram

Pin Names

A_0–A_{19}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT

8Mbit	4Mbit	2Mbit	27512	27256
A_{19}	V_{PP}	V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27010



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27256	27512	2Mbit	4Mbit	8Mbit
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Figure 2. Cerdip DIP Pin Configurations

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27010 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-200V05	Q
-250V05	Q, T, L
-250V10	Q, T, L
-300V05	Q, T, L
-300V10	Q, T, L

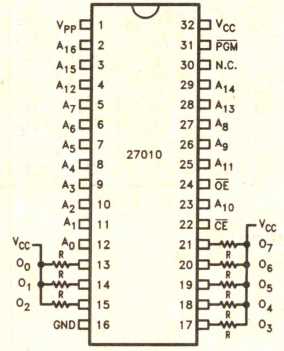
READ OPERATION

D.C. CHARACTERISTICS

Electrical parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

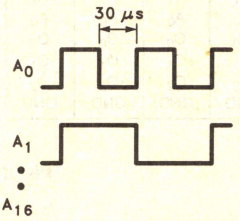
Symbol	Parameter	TD27010 LD27010		Test Conditions
		Min	Max	
I_{CC1}(1)	V_{CC} Active Current (mA)		160	$\overline{OE} = \overline{CE} = V_{IL}$, $T_{Ambient} = -40°C$
	V_{CC} Active Current at High Temperature (mA)		125	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with outputs O_0 to O_7 unloaded.



290105-4

$\overline{OE}$ = +5V R = 1 KΩ V_{CC} = +5V
V_{PP} = +5V GND = 0V $\overline{CE}$ = GND
PGM = +5V



290105-5

Binary Sequence from A_0 to A_{16}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with Respect to Ground ..... −0.6V to +6.5V

Voltage on A_9 with Respect to Ground ..... −0.6V to +13.5V

V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits				Conditions
		Min	Typ(2)	Max	Units	
I_{LI}	Input Load Current			1	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{PP1}(1)	V_{PP} Load Current			1	μA	$V_{PP} \le V_{CC}$
I_{SB}	V_{CC} Current Standby			50	mA	$\overline{CE} = V_{IH}$
I_{CC1}(1)	V_{CC} Current Active			150	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA
V_{PP}(1)	V_{PP} Read Voltage	−0.1		$V_{CC}+1$	V	$V_{CC} = 5.0V \pm 0.25$

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

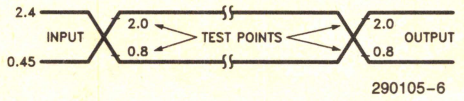
Versions	$V_{CC} \pm 5\%$	27010-200V05		27010-250V05		27010-300V05		Unit	Test Conditions
	$V_{CC} \pm 10\%$			27010-250V10		27010-300V10			
Symbol	Characteristics	Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		85		100		120	ns	$\overline{CE} = V_{IL}$
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	60	0	60	0	105	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

NOTES:
1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

CAPACITANCE[2] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Capacitance	18	25	pF	V_{PP} = 0V

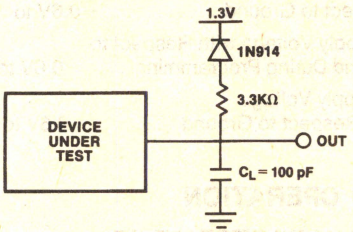
A.C. TESTING INPUT/OUTPUT WAVEFORM



290105-6

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

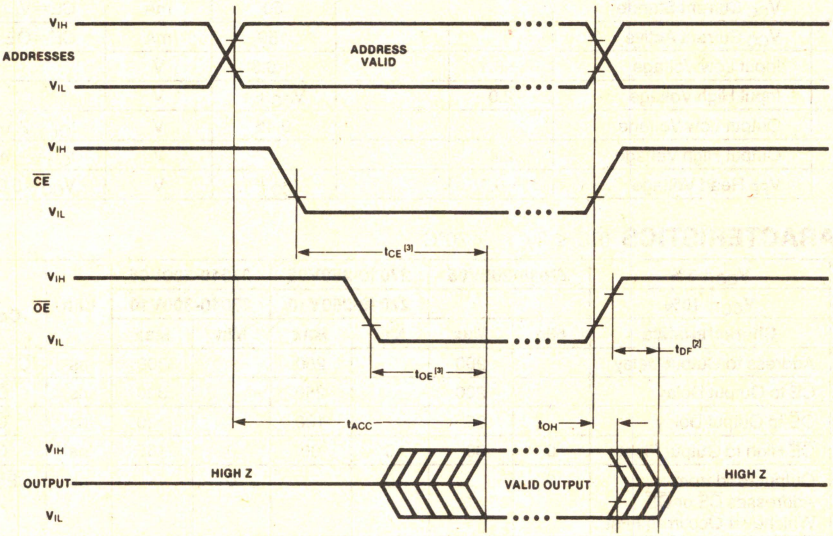
A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

290105-7

A.C. WAVEFORMS



290105-8

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27010 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for inteligent Identifier.

Table 1. Modes Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X(1)	X	X	X	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
inteligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IL}	X	5.0V	89 H
	Device(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IH}	X	5.0V	05 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1–A_8, A_{10}–$A_{16} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27010 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Upgrade Path

Future upgrades to 8M-bits are easily accomplished due to the standardized pin configuration of the 27010. When the 27010 is in the Read Mode ($V_{PP} \leq V_{CC}$) the $\overline{PGM}$, N.C., and the V_{PP} inputs become non-functional and may be either V_{IL} or V_{IH}. This allows address lines A17–A19 to be routed directly to these inputs in anticipation of future density upgrades. Systems designed for 1M-bit program memories today can be upgraded to higher densities (8M-bit) in the future with no circuit board changes.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

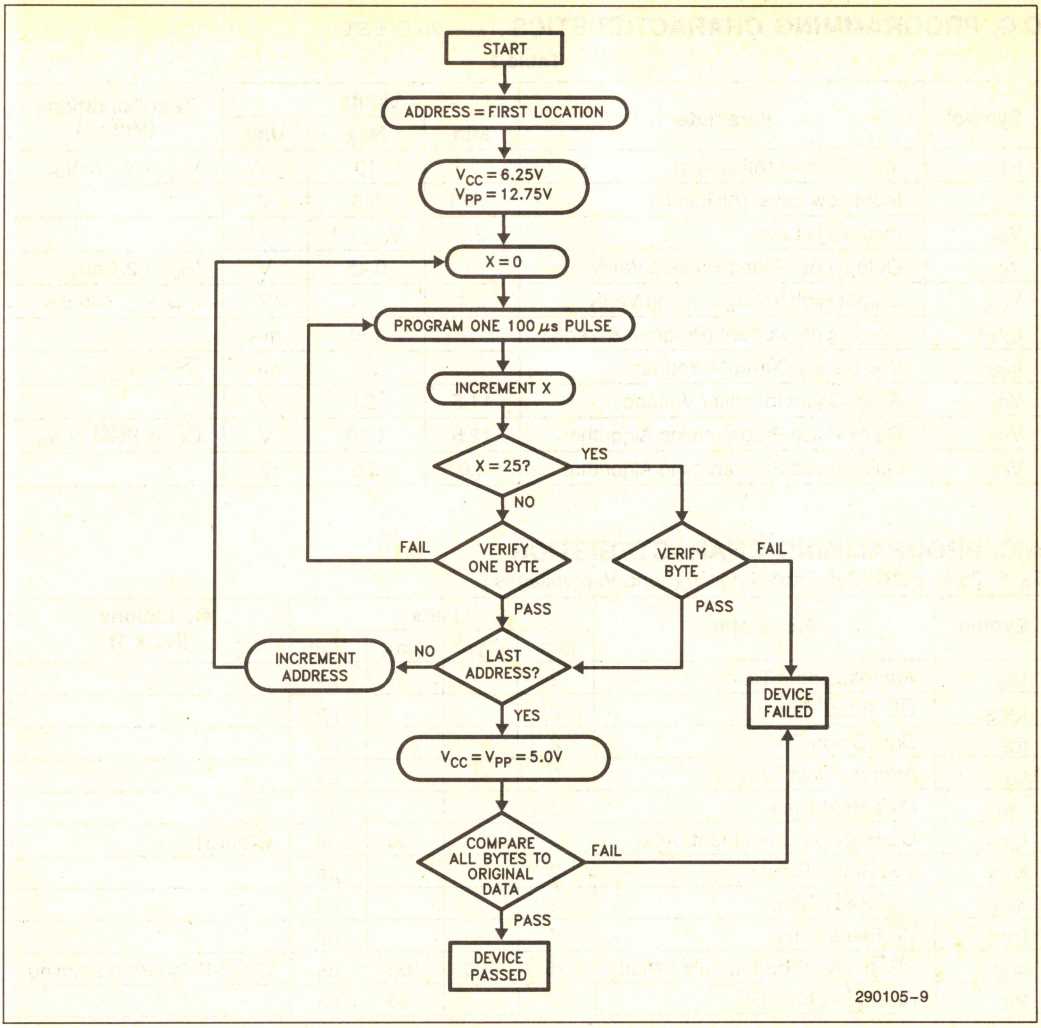


Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27010 EPROM can be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under 15 seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 μs pulses per byte are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V ($V_{PP} \leq V_{CC}$).

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current (Program & Verify)		150	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

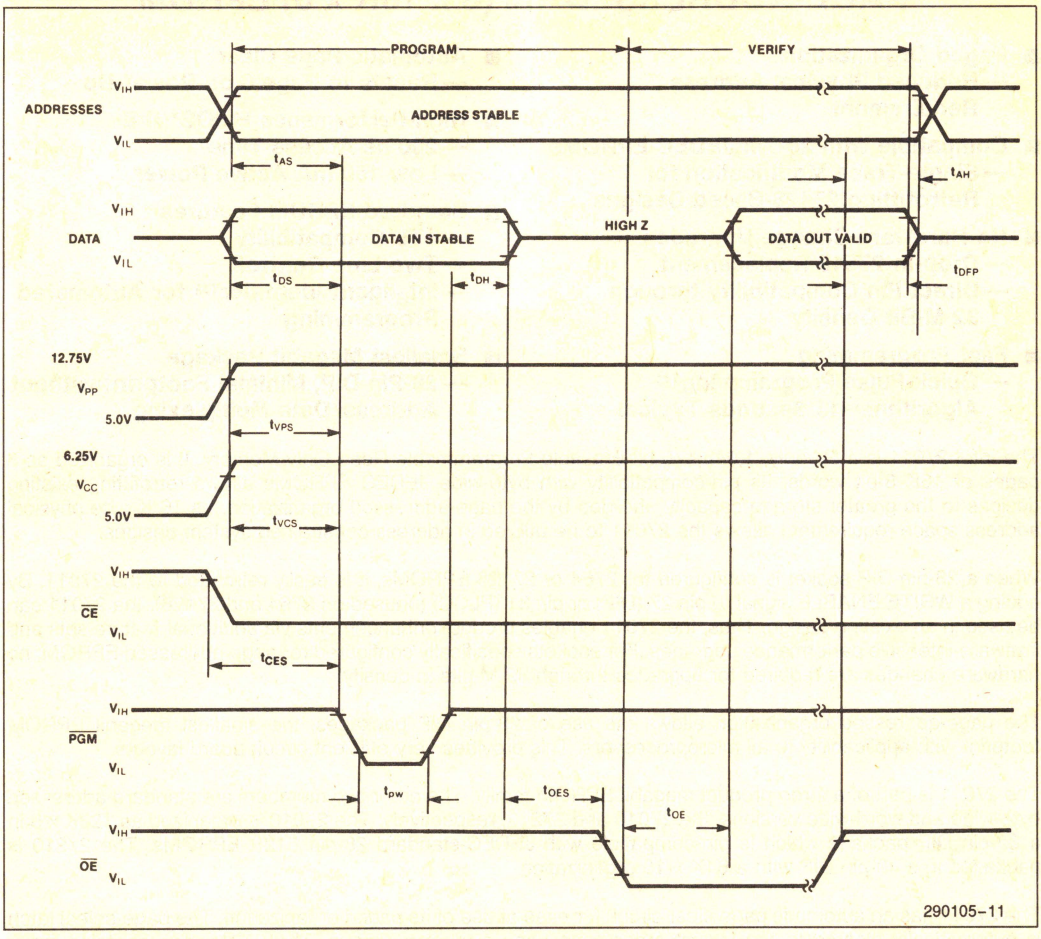
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27010, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

27011
PAGE-ADDRESSED 1M (8 x 16K x 8) EPROM

- **Paged Organization**
  - **— Reduced Physical Address Requirement**
- **Compatible with 28-Pin JEDEC EPROMs**
  - **— Single-Trace Modification for Retrofitting 27128-Based Designs**
- **No-Hardware-Change Upgrades**
  - **— Drop-In 27513 Replacement**
  - **— Direct Pin Compatibility through 32 M-Bit Density**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm—15 Seconds Typical**
- **Automatic Page Clear**
  - **— Resets to Page 0 on Power-Up**
- **High-Performance HMOS* II-E**
  - **— 200 ns Access Time**
  - **— Low 150 mA Active Power**
- **Standard EPROM Features**
  - **— TTL Compatibility**
  - **— Two Line Control**
  - **— int$_e$ligent Identifier™ for Automated Programming**
- **Smallest Megabit Package**
  - **— 28-Pin DIP, Minimal Footprint without Address/Data Multiplexing**

The Intel 27011 is a 5V-only, 1,048,576-bit Erasable Programmable Read Only Memory. It is organized as 8 pages of 16K 8-bit words. Its pin-compatibility with byte-wide JEDEC EPROMs allows retrofitting existing designs to the greater storage capacity afforded by the page-addressed organization. Its 16 K-byte physical address space requirement allows the 27011 to be utilized in address-constrained system designs.

When a 28-pin DIP socket is configured for 2764 or 27128 EPROMs, it is easily retrofitted to the 27011. By adding a WRITE ENABLE signal to pin 27 (DIP) or pin 31 (PLCC) (unused on 2764 and 27128), the 27011 can be used in an existing design. Thus, the 27011 enables product enhancements via additional feature sets and firmware-intensive performance upgrades. For sockets specifically configured for page-addressed EPROM, no hardware changes are required for upgrades through 32 M-bits in density!

The page-addressed organization allows the use of 28-pin DIP packages, the smallest megabit EPROM footprint with applicability to all microprocessors. This provides very efficient circuit board layouts.

The 27011 is part of a three-product megabit EPROM family. The other two members are standard-addressed byte-wide and word-wide versions, the 27010 and 27210, respectively. The 27010 is organized as 128K x 8 in a 32-pin DIP package which is pin-compatible with JEDEC-standard 28-pin 512K EPROMs. The 27210 is packaged in a 40-pin DIP with a 64K x 16 organization.

The 27011 has an automatic page clear circuit for ease of use of its paged organization. The page-select latch is automatically cleared to the lowest order page upon system power-up. The 27011 also contains many industry-standard features such as two-line output control for simple interfacing and the int$_e$ligent Identifier™ feature for automated programming. It also can be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 15 seconds.

The 27011 is manufactured using an advanced version of Intel's HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

November 1987
Order Number: 290107-003

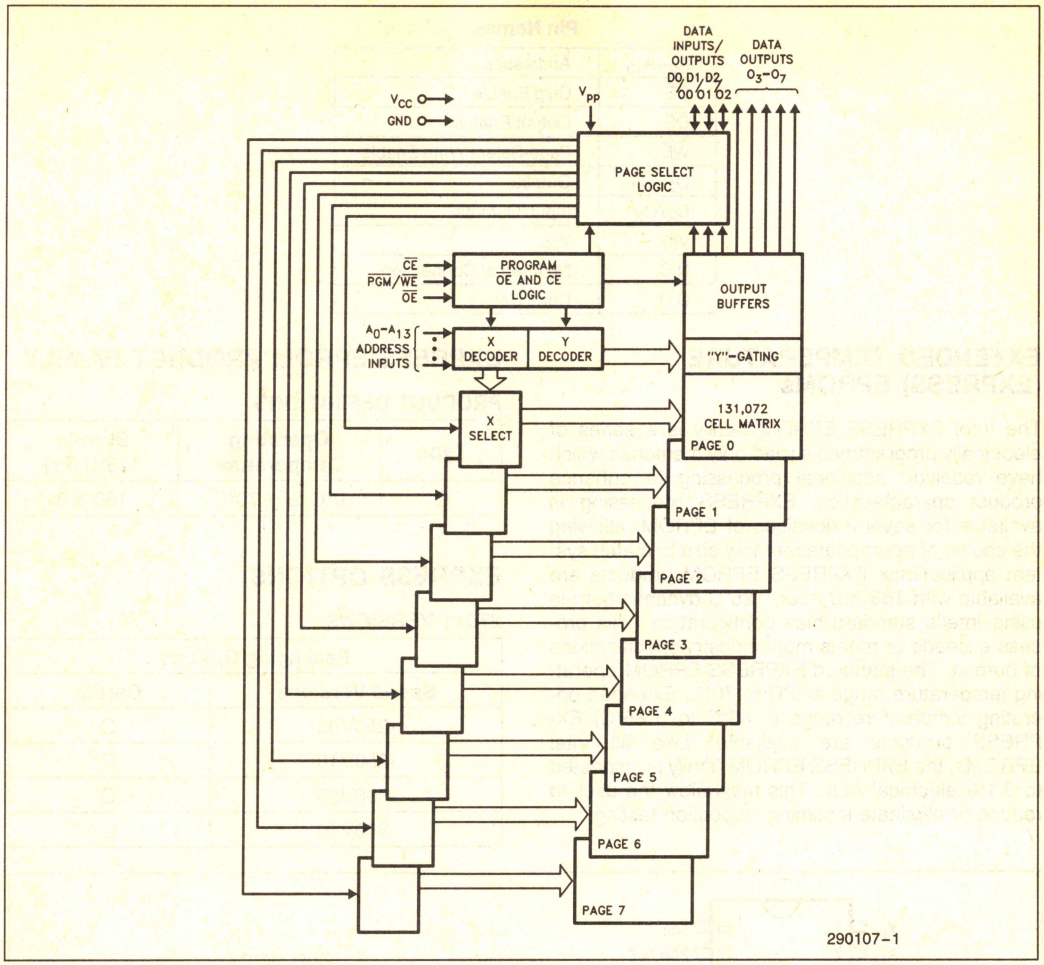
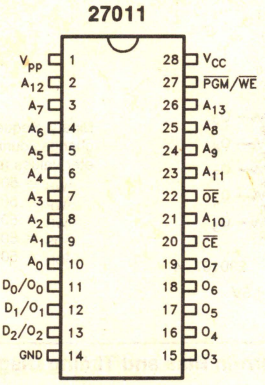


Figure 1. Block Diagram

4 M-bit	2 M-bit	27513	27128A
$V_{PP}/\overline{RST}$	$V_{PP}/\overline{RST}$	$\overline{RST}$(2)	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
D_0/O_0	D_0/O_0	D_0/O_0	O_0
D_1/O_1	D_1/O_1	D_1/O_1	O_1
D_2/O_2	D_2/O_2	O_2	O_2
GND	GND	GND	GND



27128A	27513	2 M-bit	4 M-bit
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{WE}$	$\overline{PGM/WE}$	$\overline{WE}$
A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	D_4/O_4
O_3	O_3	D_3/O_3	D_3/O_3

Figure 2. Pin Configuration

Pin Names

A_0–A_{13}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Page-Select Write Enable
O_2–O_7	Outputs
D_X/O_X	Input/Outputs
V_{PP}	V_{PP}
N.C.	No Internal Connection
D.U.	Don't Use

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

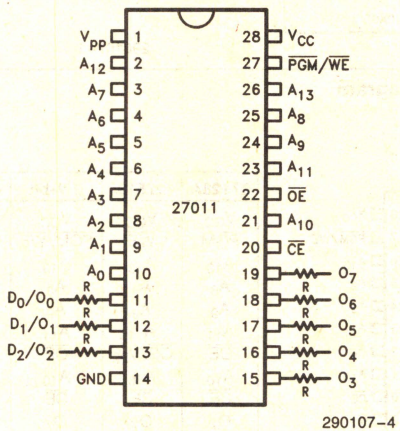
PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-In 125°C (hr)
Q	0°C to +70°C	168 ±8

EXPRESS OPTIONS

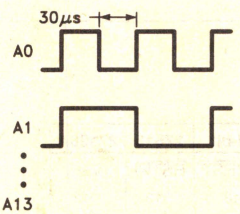
27011 VERSIONS

Packaging Options	
Speed Versions	**Cerdip**
-250V05	Q
-250V10	Q
-300V05	Q
-300V10	Q



290107-4

V_{PP} = +5V R = 1 KΩ V_{CC} = +5V
GND = 0V $\overline{CE}$ = GND



290107-5

Binary Sequence from A_0 to A_{13} required for each page. Page changes during burn-in require the following minimum timing parameter values (see Page-Select A.C. Characteristics):

t_{WH} = 500 ns
t_{WP} = 500 ns
t_{WR} = 500 ns
t_{DS} = 500 ns
t_{DH} = 500 ns

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
Read ..... 0°C to +70°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground† ..... −0.6V to +6.25V
Voltage on A_9 with
Respect to Ground ..... −0.6V to +13.5V
V_{PP} Supply Voltage with Respect to
Ground During Programming .... −0.6V to +14V
V_{CC} Supply Voltage
with Respect to Ground ..... −0.6V to +7.0V

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			1	µA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = 5.5V$
I_{PP1}(1)	V_{PP} Load Current			500	µA	$V_{PP} \le V_{CC}$
I_{SB}	V_{CC} Current Standby			50	mA	$\overline{CE} = V_{IH}$
I_{CC1}(5)	V_{CC} Current Active			150	mA	$\overline{CE} = OE = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA
V_{CLR}	Page Latch Clear—V_{CC}		3.5	4.0	V	

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Versions (5)	$V_{CC} \pm 5\%$	27011-200V05		27011-250V05		27011-300V05		Units
	$V_{CC} \pm 10\%$			27011-250V10		27011-300V10		
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		85		100		120	ns
t_{DF}(3)	$\overline{OE}$ High to Output Float	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		ns

NOTES:
1. V_{PP} should be at a TTL V_{IH} level except during programming.
2. Typical values are for $T_A = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. Packaging options: No prefix = Cerdip; Plastic DIP = P; PLCC = N.
5. The maximum current value is with outputs O_0 to O_7 unloaded.

PAGE-SELECT WRITE OPERATION

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

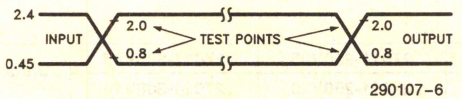
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{CW}	$\overline{CE}$ to End of Write	180		ns	$\overline{OE} = V_{IH}$
t_{WP}	Write Pulse Width	100		ns	$\overline{OE} = V_{IH}$
t_{WR}	Write Recovery Time	20		ns	
t_{DS}	Data Setup Time	50		ns	$\overline{OE} = V_{IH}$
t_{DH}	Data Hold Time	20		ns	$\overline{OE} = V_{IH}$
t_{CS}	$\overline{CE}$ to Write Setup Time	0		ns	$\overline{OE} = V_{IH}$
t_{WH}	$\overline{WE}$ Low from $\overline{OE}$ High Delay Time	55		ns	

CAPACITANCE(1) $T_A = +25°C$, f = 1 MHz

Symbol	Parameter	Typ(1)	Max	Units	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
C_{VPP}	V_{PP} Capacitance	18	25	pF	$V_{IN} = 0V$

1. Sampled. Not 100% tested.

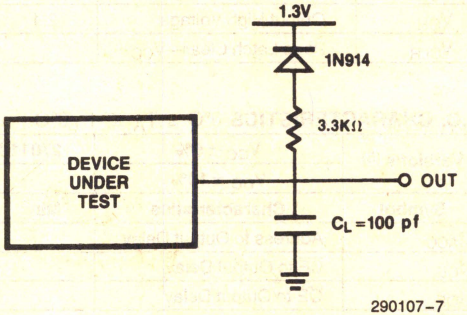
A.C. TESTING INPUT/OUTPUT WAVEFORM



290107-6

AC Testing inputs are driven at 2.4V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for a logic 0.

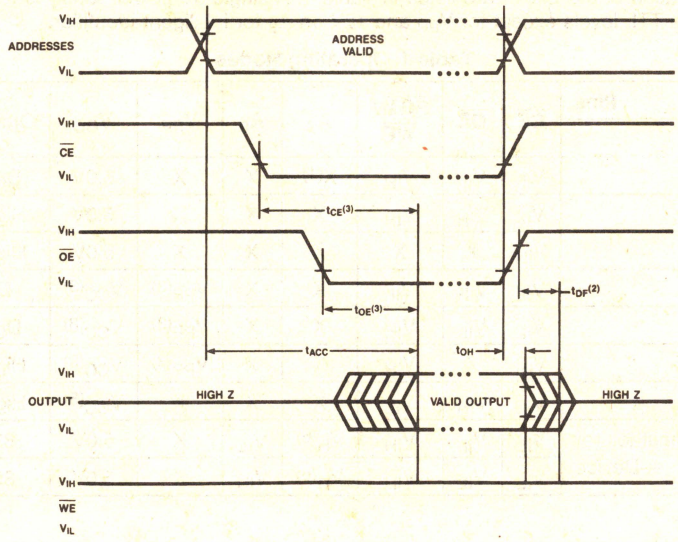
A.C. TESTING LOAD CIRCUIT



290107-7

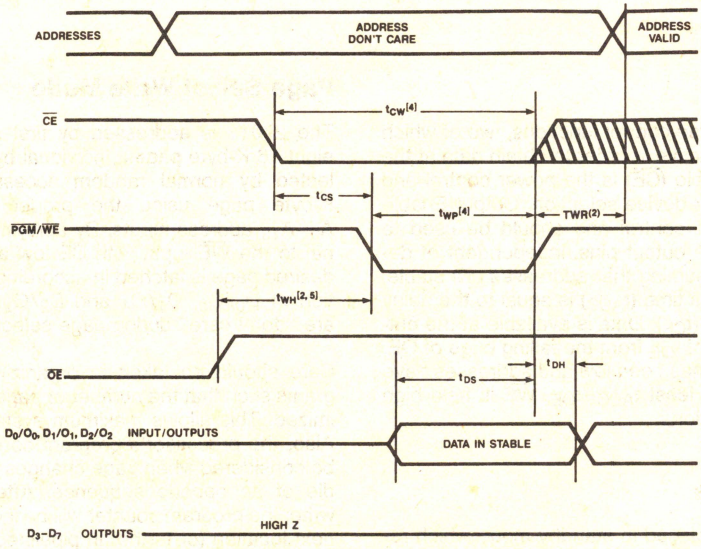
C_L = 100 pF
C_L Includes Jig Capacitance

A.C. WAVEFORMS FOR READ OPERATION



290107-8

A.C. WAVEFORMS FOR PAGE-SELECT WRITE OPERATION



290107-9

NOTES:
1. Typical values are for $T_A = +25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. Write may be terminated by either $\overline{CE}$ or $\overline{WE}$, providing that the minimum t_{CW} requirement is met before bringing $\overline{WE}$ high or that the minimum t_{WP} requirement is met before bringing $\overline{CE}$ high.
5. $\overline{OE}$ must be high during write cycle.

DEVICE OPERATION

The modes of operation of the 27011 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Operating Modes

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$/$\overline{WE}$	A_9	A_0	V_{PP}	V_{CC}	Outputs	Input/ Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	X	5.0V	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	5.0V	High Z	High Z
Standby	V_{IH}	X	X	X	X	X	5.0V	High Z	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}(3)	V_{CC}(3)	D_{IN}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	D_{OUT}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{IH}	X	X	V_{PP}(3)	V_{CC}(3)	High Z	High Z
Page-Select Write	V_{IL}	V_{IH}	V_{IL}	X	X	X	V_{CC}(5)	High Z	Page D_{IN}
int$_e$ligent —Manufacturer Identifier —Device	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IL}	X	5.0V	89H	89H
	V_{IL}	V_{IL}	V_{IH}	V_H(6)	V_{IH}	X	5.0V	85H	85H

NOTES:
1. X can be V_{IH} or V_{IL}.
2. Addresses are don't care for page selection. See Table 2 for D_{IN} values.
3. See Table 3 for V_{CC} and V_{PP}.
4. A_1–A_8, A_{10}–A_{13}, = V_{IL}.
5. Page 0 is automatically selected at power-up (V_{CC} < 4.0V).
6. V_H = 12.0V ±0.5%.

Read Mode

The 27011 has three control functions, two of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}–t_{OE}. $\overline{WE}$ is held high during read operations.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ and $\overline{WE}$ inputs.

Page-Select Write Mode

The 27011 is addressed by first selecting one of eight 16 K-byte pages. Individual bytes are then selected by normal random access within the 16 K-byte page using the proper combination of A_0–A_{13} address inputs. By applying a TTL low signal to the $\overline{WE}$ input with $\overline{CE}$ low and $\overline{OE}$ high, the desired page is latched in according to the combination of D_0/O_0, D_1/O_1 and D_2/O_2. Address inputs are "don't care" during page selection.

Care should be taken in organizing software programs such that the number of page changes is minimized. This allows maximum system performance. Also, the processor's program counter status must be considered when page changes occur in the middle of an opcode sequence. After a page-select write, the program counter will be incremented to the next location (or further in pipelined systems) in the new page relative to that of the page-select write opcode in the previous page.

Table 2. Page Selection Data

Input/Output Page Selection	D_2/O_2	D_1/O_1	D_0/O_0
Select Page 0	V_{IL}	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IL}	V_{IH}
Select Page 2	V_{IL}	V_{IH}	V_{IL}
Select Page 3	V_{IL}	V_{IH}	V_{IH}
Select Page 4	V_{IH}	V_{IL}	V_{IL}
Select Page 5	V_{IH}	V_{IL}	V_{IH}
Select Page 6	V_{IH}	V_{IH}	V_{IL}
Select Page 7	V_{IH}	V_{IH}	V_{IH}

Automatic Page Latch Clear

The 27011 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latch is automatically cleared to page 0 upon power-up. As the V_{CC} supply voltage ramps up, the page latch is cleared. After V_{CC} exceeds the 4.0V maximum page latch clear voltage (V_{CLR}), the latch clear circuit is disabled. This ensures an adequate safety margin (500 mV of system noise below the worst case −10% V_{CC} supply condition) against spurious page latch clearing.

Two Line Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 output control lines which accommodate this multiple memory connection. The two control lines for read operation allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

Similarly, $\overline{CE}$ deselects other 27011s or RAMs during page select write operation while $\overline{WE}$ is in common with other devices in the array. $\overline{WE}$ is connected to the $\overline{WRITE}$ system control line.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be as stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on V_{PP} will permanently damage the 27011.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 27011 is in the programming mode when the V_{PP} input is at its programming voltage and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple 27011s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits the other 27011s from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27011s may be common. A TTL low-level pulse applied to the $\overline{PGM}/\overline{WE}$ input with V_{PP} at its programming voltage will program the selected 27011.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and V_{CC} is at its programming voltage. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufcturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for all Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPs makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT, and PCDOS compatibles, Intellec Development Systems, Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMs)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 $Wsec/cm^2$ (1 week @ 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

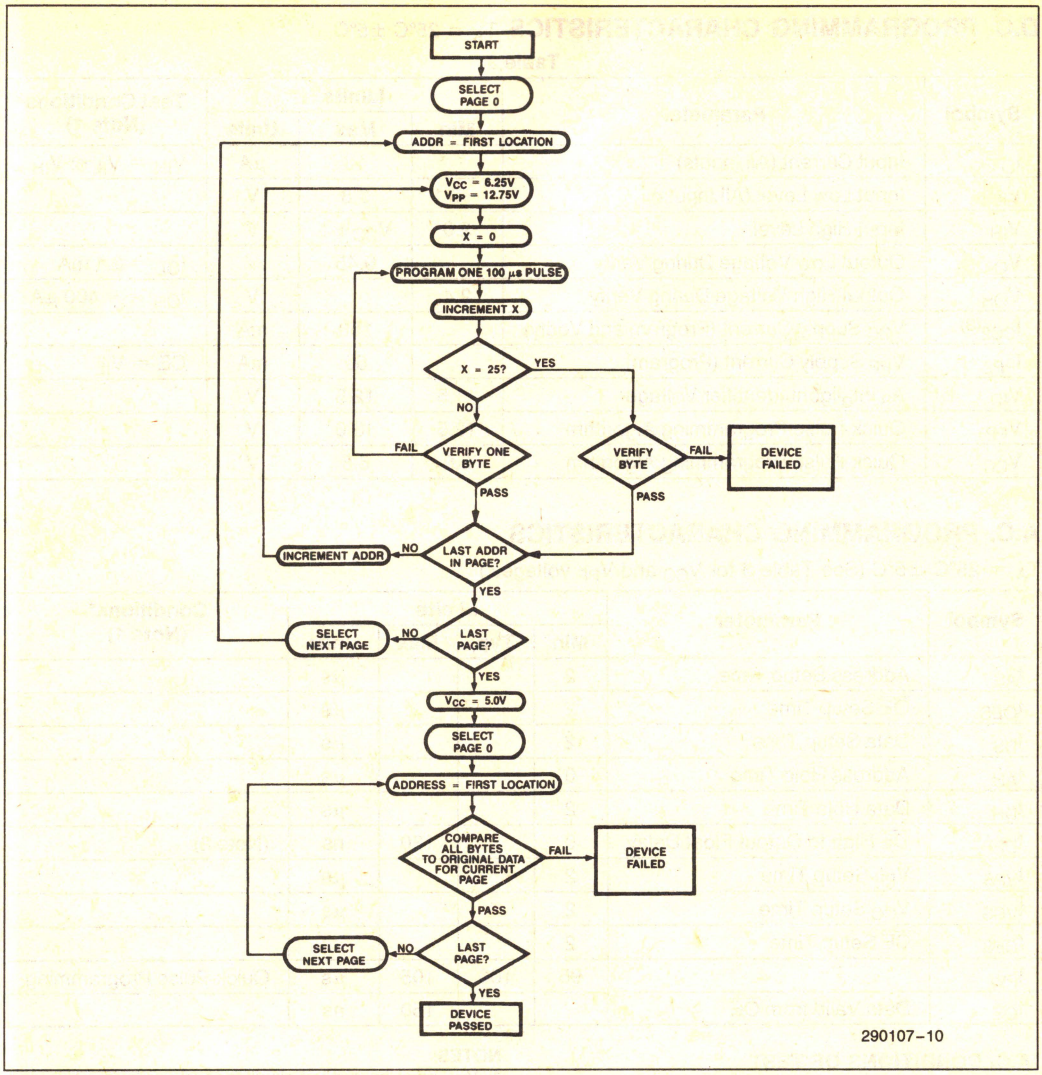


Figure 4. 27011 Quick-Pulse Programming™ Flowchart

Quick Pulse Programming™ Algorithm

Intel's 27011 EPROM can be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under fourteen seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 3

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Units	
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current (Program and Verify)		150	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 3 for V_{CC} and V_{PP} voltages.)

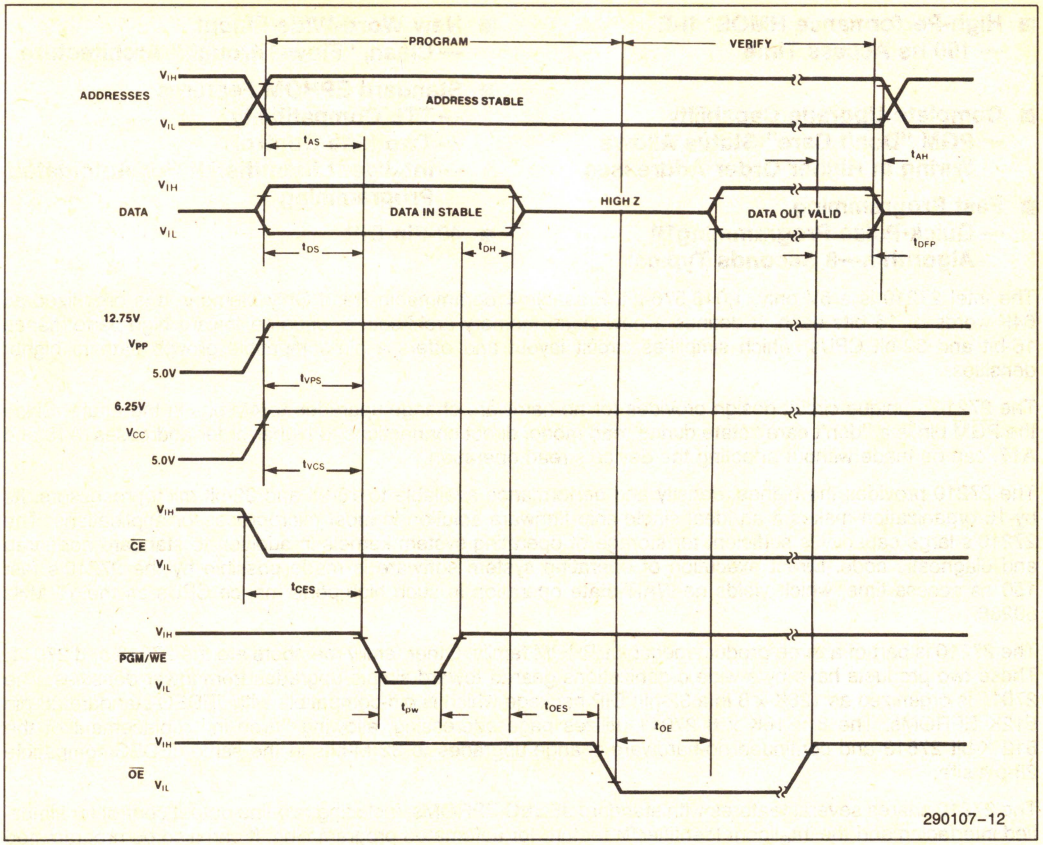
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Units	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}		95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page-select write operation prior to programming each of the four 16 Kbyte pages. See Page Select Write AC and DC Characteristics for information on page selection operations.

27210
1M (64K x 16) WORD-WIDE EPROM

- **High-Performance HMOS* II-E**
  — 150 ns Access Time
- **Complete Upgrade Capability**
  — PGM "Don't Care" Status Allows Wiring in Higher Order Addresses
- **Fast Programming**
  — Quick-Pulse Programming™ Algorithm—8 Seconds Typical
- **New Word-Wide Pinout**
  — Clean, "Flow-Through" Architecture
- **Standard EPROM Features**
  — TTL Compatibility
  — Two Line Control
  — int$_e$ligent Identifier™ For Automated Programming
- **40-Pin DIP**

The Intel 27210 is a 5V only, 1,048,576-bit, Erasable Programmable Read Only Memory. It is organized as 64K-words of 16 bits each. It defines a new-clean memory architecture, oriented toward high-performance 16-bit and 32-bit CPUs, which simplifies circuit layout and offers a pin-compatible growth path to higher densities.

The 27210's unique circuit design provides for no-hardware-change upgrades to 4M-bits in the future. Since the $\overline{PGM}$ pin is a "don't care" state during read mode, direct connections to higher order addresses, A16 and A17, can be made without affecting the device's read operation.

The 27210 provides the highest density and performance available to 16-bit and 32-bit microprocessors. Its by-16 organization makes it an ideal single-chip firmware solution in most microprocessor applications. The 27210's large capacity is sufficient for storage of operating system kernels in addition to standard bootstrap and diagnostic code. Direct execution of operating system software is made possible by the 27210's fast 150 ns access time, which yields no-WAIT-state operation in such high-performance CPUs as the 10 MHz 80286.

The 27210 is part of a three-product megabit EPROM family. Other family members are the 27010 and 27011. These two products have byte-wide organizations geared toward simple upgrades from lower densities. The 27010 is organized as 128K x 8 in a 32-pin DIP package which is pin-compatible with JEDEC-standard 28-pin 512K EPROMs. The 8 x 16K x 8 27011 utilizes page addressing, allowing "drop in" replacement of the 512 K-bit 27513 and continued no-hardware-change upgrades to 32 M-bits in the same JEDEC-compatible 28-pin site.

The 27210 shares several features with standard JEDEC EPROMs, including two-line output control for simplified interfacing and the int$_e$ligent Identifier™ feature for automated programming. It can also be programmed rapidly using Intel's Quick-Pulse Programming™ Algorithm, typically within 8 seconds.

The 27210 is manufactured using a scaled version of Intel's advanced HMOS* II-E process which assures highest reliability and manufacturability.

*HMOS is a patented process of Intel Corporation.

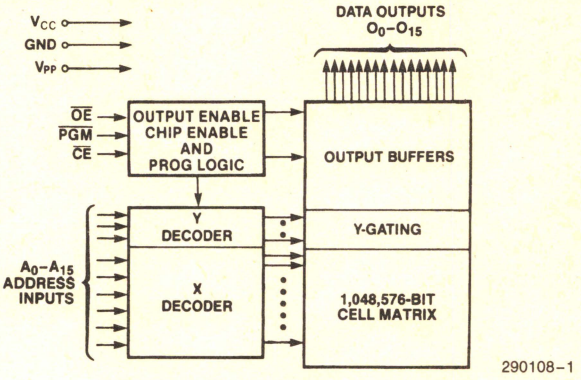
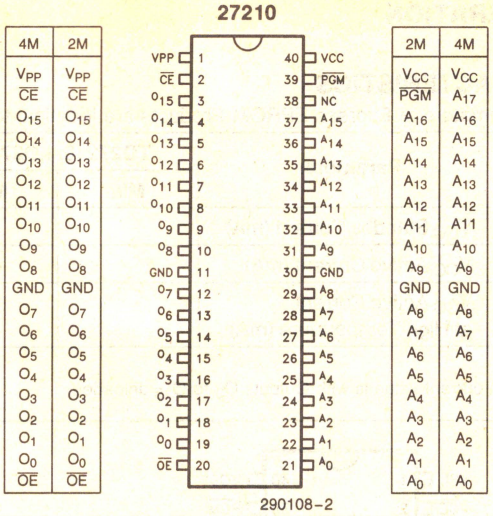


Figure 1. Block Diagram

November 1987
Order Number: 290108-003

Pin Names

A_0–A_{17}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_{15}	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO INTERNAL CONNECT
D.U.	DON'T USE



290108-2

NOTE: Compatible HIgher Density Word Wide EPROM Pin Configurations are Shown in the Blocks Adjacent to the 27210 Pins

Figure 2. Cerdip/Plastic(P) DIP Pin Configurations

EXTENDED TEMPERATURE (EXPRESS) EPROMS

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM PRODUCT FAMILY

PRODUCT DEFINITIONS

Type	Operating Temperature	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

27210 Versions

Packaging Options	
Speed Versions	**Cerdip**
-170V05	Q
-200V05	T, L, Q
-250V05	T, L, Q
-200V10	Q
-250V10	T, L, Q

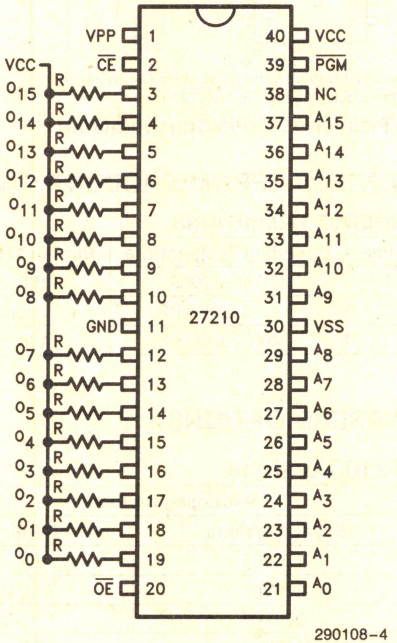
READ OPERATION

D.C. CHARACTERISTICS

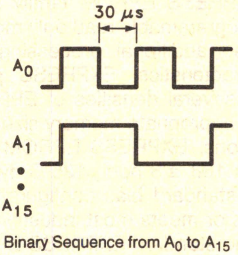
Electrical Parameters of Express EPROM Products are identical to standard EPROM parameters except for:

Symbol	Parameter	TD27210, LD27210		Test Conditions
		Min	Max	
I_{SB}	V_{CC} Standby Current (mA)		50	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC1}(1)	V_{CC} Active Current (mA)		195	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature (mA)		175	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $T_{Ambient} = 85°C$

NOTE:
1. The maximum current value is with Outputs O_0 to O_{15} unloaded.



$\overline{OE}$ = +5V R = 1 kΩ V_{CC} = +5V
V_{PP} = +5V GND = 0V $\overline{CE}$ = GND



Binary Sequence from A_0 to A_{15}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

All Input or Output Voltages with Respect to Ground ..... −0.6V to +6.25V

Voltage on A_9 with Respect to Ground ..... −0.6V to +13.0V

V_{PP} Supply Voltage with Respect to Ground During Programming .... −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7.0V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

READ OPERATION

D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter	Limits				Conditions
		Min	Typ(3)	Max	Units	
I_{LI}	Input Load Current			1	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			1	μA	$V_{OUT} = 5.5V$
I_{PP1}(2)	V_{PP} Load Current Read			1	μA	$V_{PP} = 5.5V$
I_{SB}	V_{CC} Current Standby			40	mA	$\overline{CE} = V_{IH}$
I_{CC1}(2)	V_{CC} Current Active			175(6)	mA	$\overline{CE} = OE = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

A.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

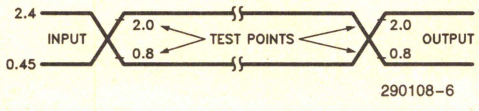
Versions(5)	$V_{CC} \pm 5\%$	27210-150V05		27210-170V05		27210-200V05		27210-250V05		Unit
	$V_{CC} \pm 10\%$			27210-170V10		27210-200V10		27210-250V10		
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		65		70		75		100	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	0	50	0	55	0	60	0	60	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The maximum current value is with Outputs O_0 to O_{15} unloaded.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
5. Both GND pins should be connected to the ground trace on circuit boards.
6. V_{CC} Active Current specification has recently been increased from 150 mA to 175 mA, max.

CAPACITANCE[2] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ[1]	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V
C_{VPP}	V_{PP} Input Capacitance		25	pF	V_{PP} = 0V

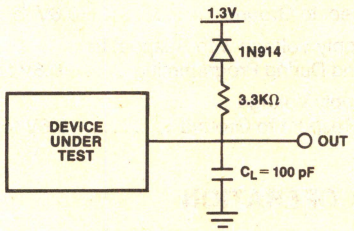
A.C. TESTING INPUT/OUTPUT WAVEFORM



290108-6

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

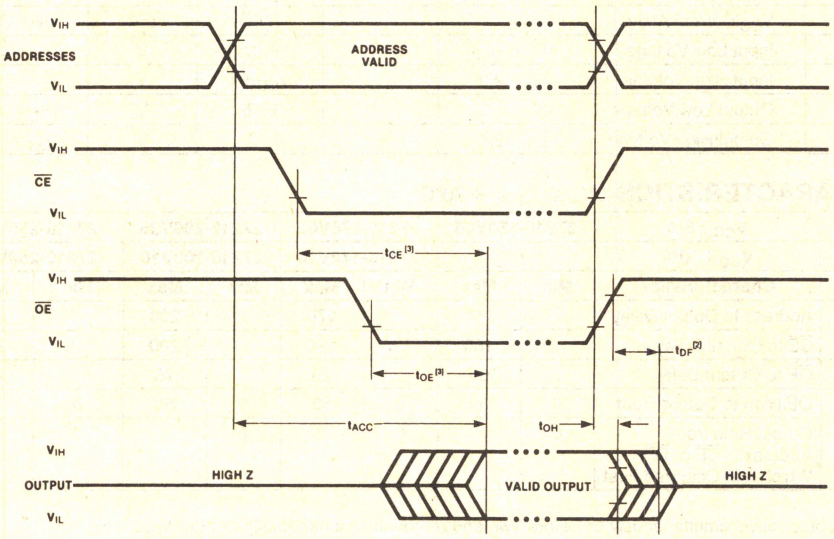
A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L Includes Jig Capacitance

290108-7

A.C. WAVEFORMS



290108-8

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE}—t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

DEVICE OPERATION

The modes of operation of the 27210 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for int$_e$ligent Identifier.

Table 1. Modes Selection

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read		V_{IL}	V_{IL}	X	X(1)	X	X	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier	Manufacturer(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IL}	V_{CC}	5.0V	0089 H
	Device(3)	V_{IL}	V_{IL}	X	V_H(2)	V_{IH}	V_{CC}	5.0V	00FFH

NOTES:
1. X can be V_{IL} or V_{IH}
2. $V_H = 12.0V \pm 0.5V$
3. A_1–A_8, A_{10}–$A_{15} = V_{IL}$
4. See Table 2 for V_{CC} and V_{PP} voltages.

Read Mode

The 27210 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

EPROMs can be placed in standby mode which reduces the maximum current of the device by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur

To use these two control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure (Cerdip EPROMs).

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ and $\overline{PGM}$ are both at TTL low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other devices from being programmed.

Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ at TTL-Low will program the selected device.

Program Verify

A verify should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} and V_{CC} at their programming voltages.

inteligent Identifier™ Mode

The inteligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the inteligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming software (iPPS). iPPS makes programming easy for a growing list of industry standard hosts, including the IBM PC, XT, AT and PCDOS compatibles, Intellec Development Systems. Intel's iPDS Personal Development System, and the Intel Network Development System (iNDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

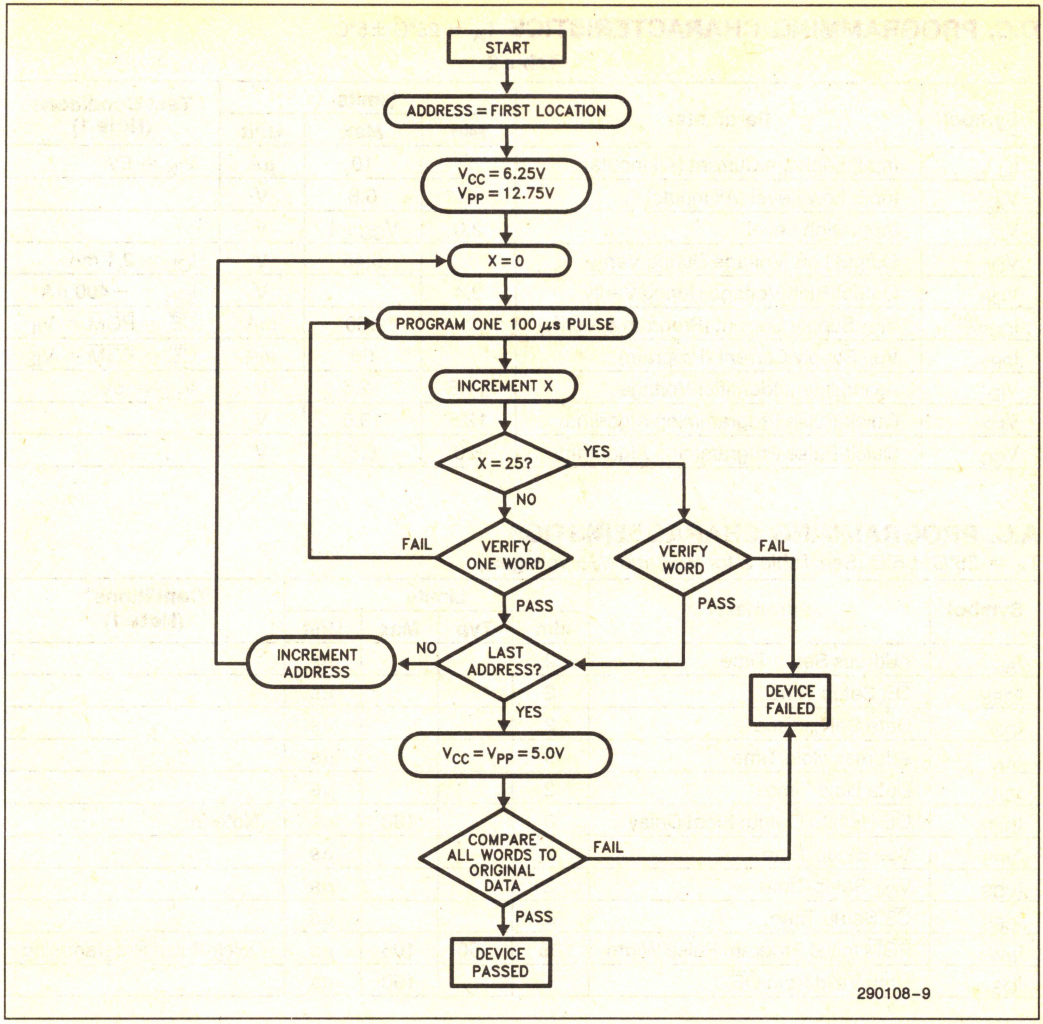


Figure 4. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27210 EPROMs can be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production programming environment. This algorithm allows these devices to be programmed in under eight seconds, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a word verification to determine when the addressed word has been successfully programmed. Up to 25 100 μs pulses per word are provided before a failure is recognized. A flow chart of the Quick-Pulse Programming Algorithm is shown in Figure 4.

For the Quick-Pulse Programming Algorithm, the entire sequence of programming pulses and word verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all data words should be compared to the original data with V_{CC} = V_{PP} = 5.0V.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Leakage Current (All Inputs)		10	μA	$V_{IN} = 6V$
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current (Program & Verify)		160	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	$V_{CC} = 5V$
V_{PP}	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$ (See Table 2 for V_{CC} and V_{PP} voltages.)

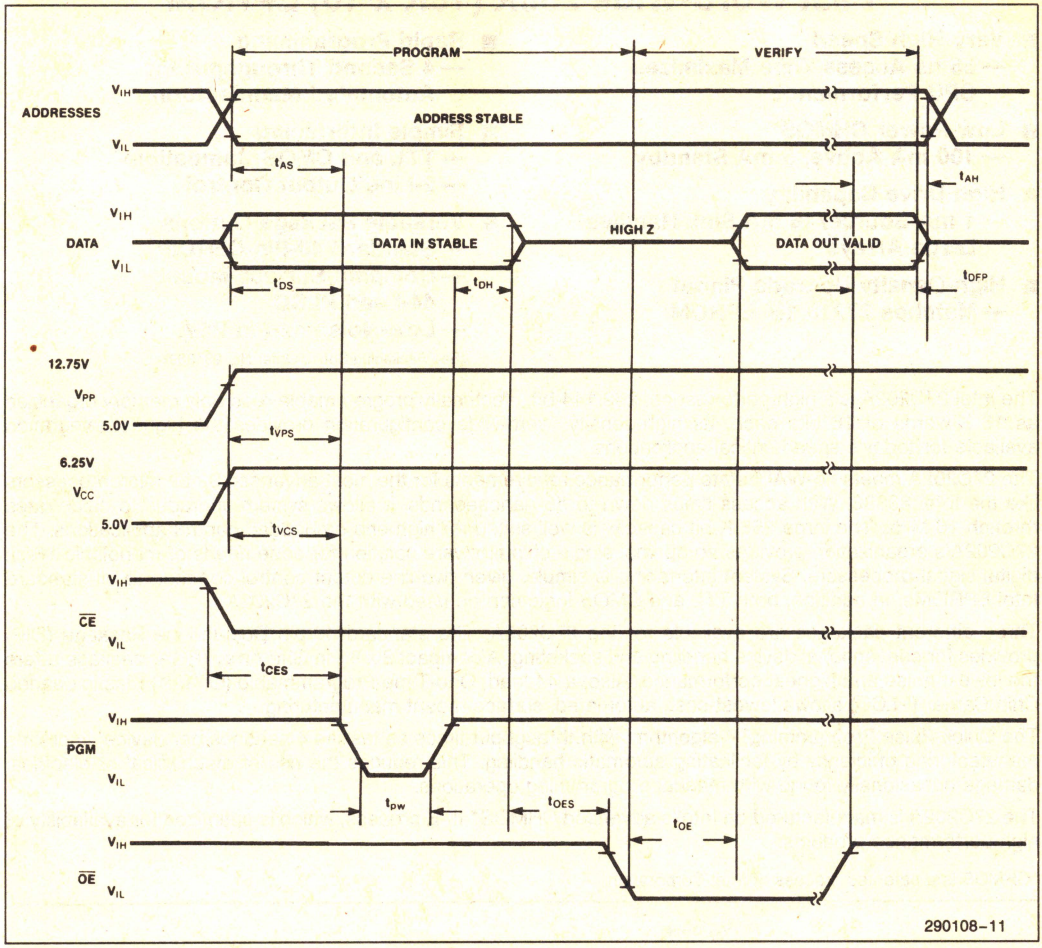
Symbol	Parameter	Limits				Conditions* (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	100	105	μs	Quick-Pulse Programming
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

*A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0–O_{15} unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27210, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

27C202A
Fast Word-Wide 256K (16K x 16) EPROM

- **Very High Speed**
  - **— 55 ns Access Time Maximizes CPU Performance**
- **Low-Power CHMOS***
  - **— 100 mA Active, 5 mA Standby**
- **High Drive Capability**
  - **— 4 mA Source/16 mA Sink Handles Large Arrays**
- **High-Density Upgrade Pinout**
  - **— Matches 27210 1M EPROM**
- **Rapid Programming**
  - **— 4 Second Throughput for Automated Manufacturing**
- **Simple Interfacing**
  - **— TTL and CMOS Compatible**
  - **— 2-Line Output Control**
- **Versatile Package Options**
  - **— Standard 40-Pin CERDIP**
  - **— Compact Surface-Mount 44-Lead PLCC**
  - **— Low-Noise 44-Pin PGA**

(See Packaging Spec., Order No. 231369)

The Intel 27C202A is a high-performance, 262,144-bit, electrically programmable read only memory organized as 16 K-words of 16 bits each. Its high-density, word-wide configuration provides the highest integration available for today's speed-critical applications.

The 27C202A meets no-WAIT-state performance requirements for the most advanced 32-bit microprocessors like the Intel 80386. With access times down to 55 nanoseconds, it allows system upgrades to clock rates through 16 MHz. The large 256 K-bit capacity is well suited for high-end embedded control applications. The 27C202A's organization provides an optimal single-chip firmware solution for code needs of monolithic 16-bit digital signal processors. System interfacing is simple, given two-line output control common to all standard Intel EPROMs. In addition, both TTL and CMOS logic can be used with the 27C202A.

Three different packages are available for the 27C202A. The standard 40-pin Dual-In-Line Package (DIP) provides for conventional device handling and socketing. A compact 8 x 8 Pin Grid Array (PGA) package offers the lowest noise and highest performance. Also, a 44-lead, One-Time-Programmable (OPT™) Plastic Leaded Chip Carrier (PLCC) allows lowest-cost, automated, surface-mount manufacturing.

The Quick-Pulse Programming™ algorithm, with throughput times as fast as 4 seconds per device, improves manufacturing efficiency by facilitating automatic handling. This reduces the risk of mechanical or electrical damage occasionally found with manual programming operations.

The 27C202A is manufactured on Intel's advanced CHMOS* III-E process, which is optimized for availability of high-performance products.

*CHMOS is a patented process of Intel Corporation.

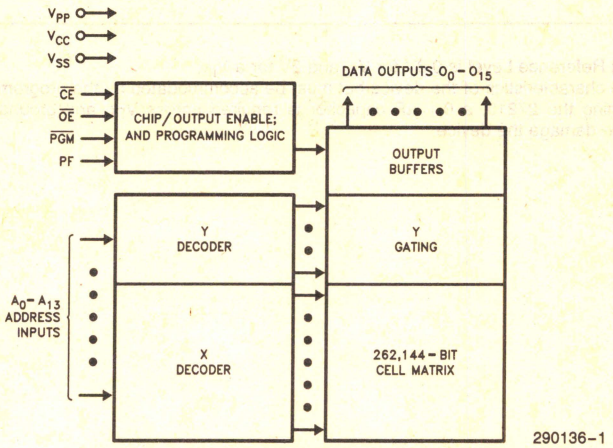


Figure 1. 27C202A Block Diagram

November 1987
Order Number: 290136-002

27C203A
FAST PIPELINED 256K (16K x 16) EPROM

- **Pipelined Interface**
  - **— Standard Latch/Clock for Address and Data Latching**
  - **— Optional Synchronous Chip Select**
  - **— TTL and CMOS Compatible**
- **Very High Speed**
  - **— 20 MHz Pipelined CPUs**
- **High Performance CHMOS***
  - **— Large Memory Density with Only 100 mA Maximum Current**
- **System Initialize Feature**
  - **— Initialization Register Forces Startup Vector for State Machine Applications**
- **Excellent Drive Capability**
  - **— 4 mA Source/16 mA Sink Current Handles Large Fanout**
- **Rapid Programming**
  - **— 4 Second Throughput for Automated Manufacturing**
- **Versatile Package Options**
  - **— Standard DIP**
  - **— Compact Surface-Mount PLCC**
  - **— Low-Noise PGA**

The Intel 27C203A is a high-performance, 262,144-bit electrically programmable read only memory organized as 16 K-words of 16 bits each. Its large density and word-wide configuration combined, with pipelined bus interface, provides a highly-integrated firmware solution for today's speed-critical applications.

The 27C203A supports pipelined bus architectures of the most advanced 32-bit microprocessors, like the Intel 80386. Pipelining relaxes memory interface logic requirements by utilizing an overlapping "early address," effectively stretching the read operation an additional clock cycle. Thus, much higher bus bandwidths are achievable. An 80386 design employing the 27C203A can accommodate future upgrades to system clock rates over 20 MHz, while utilizing slower, less expensive interface logic in current 16 MHz and 20 MHz versions. The large 256 K-bit capacity is well-suited for high-end embedded control applications. The 27C203A's simple interfacing and by-16 organization help minimize overall chip count.

State Machine designers can also use the 27C203A as a synchronous logic element, specifically where the designer needs a pipelined "data flow through" transfer function. For example, it can be applied to weighting or summing functions in high frequency filters using Digital Signal Processing techniques. To simplify design and debugging, the 27C203A provides a hardware-controlled initial condition vector through the INIT function pin.

The 27C203A is available in three package versions. The standard 40-pin Dual-In-Line-Package (DIP) provides for conventional device handling and socketing. A compact 8 x 8 Pin Grid Array (PGA) package offer the lowest noise and highest performance. Also, a 44-lead, One-Time-Programmable (OTP) Plastic Leaded Chip Carrier (PLCC) allows lowest-cost, automated, surface-mount manufacturing.

The Quick-Pulse™ Programming algorithm, with throughput times as fast as 4 seconds per device, improves manufacturing efficiency by facilitating automatic handling. This reduces the risk of mechanical or electrical damage occasionally found with manual programming operations.

The 27C203A is manufactured on Intel's advanced CHMOS* III-E process, which is optimized for availability of high-performance products.

*CHMOS is a patented process of Intel Corporation.

November 1987
Order Number: 290152-001

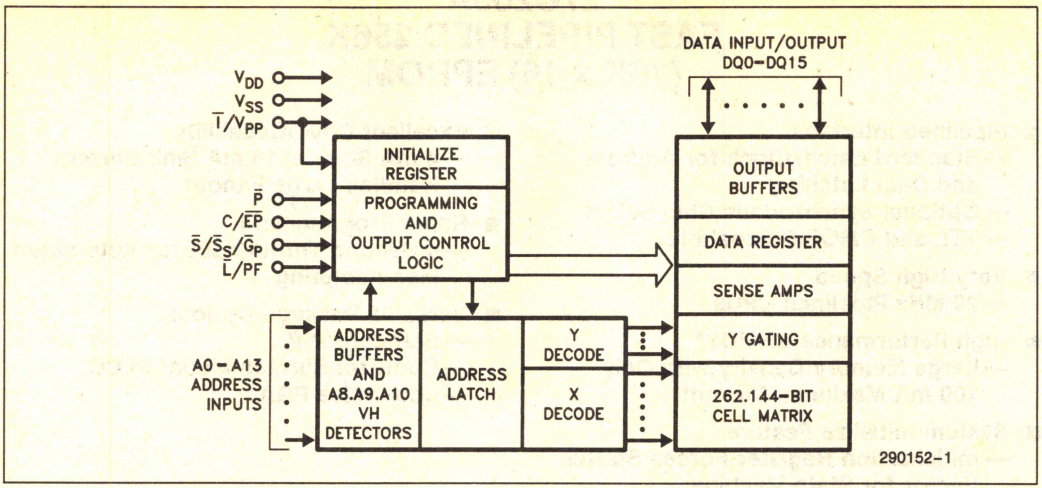


Figure 1. 27C203A Block Diagram

APPLICATION NOTE

AP-277

July 1986

The Quick-Pulse Programming™ Algorithm

TERRY KENDALL
PROGRAMMABLE MEMORY OPERATION
INTEL CORPORATION

Order Number: 292013-001

INTRODUCTION

Intel developed the Quick-Pulse Programming™ algorithm to dramatically reduce the programming throughput time in production environments. The algorithm supports plastic and PLCC (Plastic Leaded Chip Carrier) EPROMs because these devices are ideally suited for production applications. By using the Quick-Pulse Programming algorithm, a substantial decrease in programming time can be realized over older programming algorithms. For example, a 256k EPROM can be programmed in under four seconds, a 40 fold time improvement over the int$_e$ligent Programming™ algorithm.

BENEFITS FOR THE PRODUCTION ENVIRONMENT

The Quick-Pulse Programming algorithm has been introduced as the primary programming technique for OTP™ (One Time Programmable) EPROMs. OTP Plastic DIP EPROMs are ideal for production because they can be used in auto-insertion and auto-programming machines. Ceramic DIP (CERDIP) versions of newly introduced devices including the 27C256 and Megabit EPROMs (27010, 27011, and 27210) can also use Quick-Pulse Programming. Because of their erasability and reprogrammability, CERDIP EPROMs are used for prototyping and system development. When manufacturing begins, OTP EPROMs can be programmed as needed on the production floor using the Quick-Pulse Programming algorithm. If an error in firmware is discovered or a density increase is required after manufacturing has commenced, the production line need not come to a halt. Changes can be implemented instantly with OTP EPROMs. Scrapping an entire stock of masked ROMs or waiting weeks for revised ROMs is no longer necessary.

For surface-mount and space constrained applications, PLCC EPROMs are ideal. The footprint of a PLCC requires only 1/3 the surface area of a conventional DIP EPROM. PLCCs provide additional usable board space because both sides of the printed circuit board can be used for device surface mounting. To keep pace with automated handling equipment, which is used extensively with PLCCs, production line programming equipment must have fast throughput times. Again, the Quick-Pulse Programming algorithm comes to the rescue. Coupled with auto-handlers, Quick-Pulse Programming equipment can place code in PLCC EPROMs on the production floor.

The primary benefit of plastic EPROMs and the Quick-Pulse Programming algorithm is throughput time (TPT). The Quick-Pulse Programming algorithm provides a significant increase in the number of units that can be programmed in a given time. Below is an example that compares a typical PROM programmer (using the int$_e$ligent Programming algorithm) with a state-of-the-art Quick-Pulse Programmer.

Although the int$_e$ligent Programmer in the example above is typical of high quality programmers on the market today, it can achieve a TPT of only 3% that of an optimized Quick-Pulse Programmer. To put this in production terms, a supply of EPROMs that previously required a month to program using conventional programming equipment can now be programmed in only half a day using Quick-Pulse Programming equipment.

The Quick-Pulse Programming algorithm is supported by many single socket programmers. Coupled with automatic handlers, these programmers can be used for automated programming. High performance gang programmers that approach theoretical Quick-Pulse Programming times are also available.

		Quick-Pulse Programmer	Typical int$_e$ligent Programmer
Auto Handler	time/part	0.5 sec/part	0.5 sec/part
Programming	time/part (256k)	4.0 sec/part	158 sec/part
Total	time/part	4.5 sec/part	158.5 sec/part
Total	units/hour	800 U/hour	22 U/hour
Total	units/month	139 kU/month	3.9 kU/month

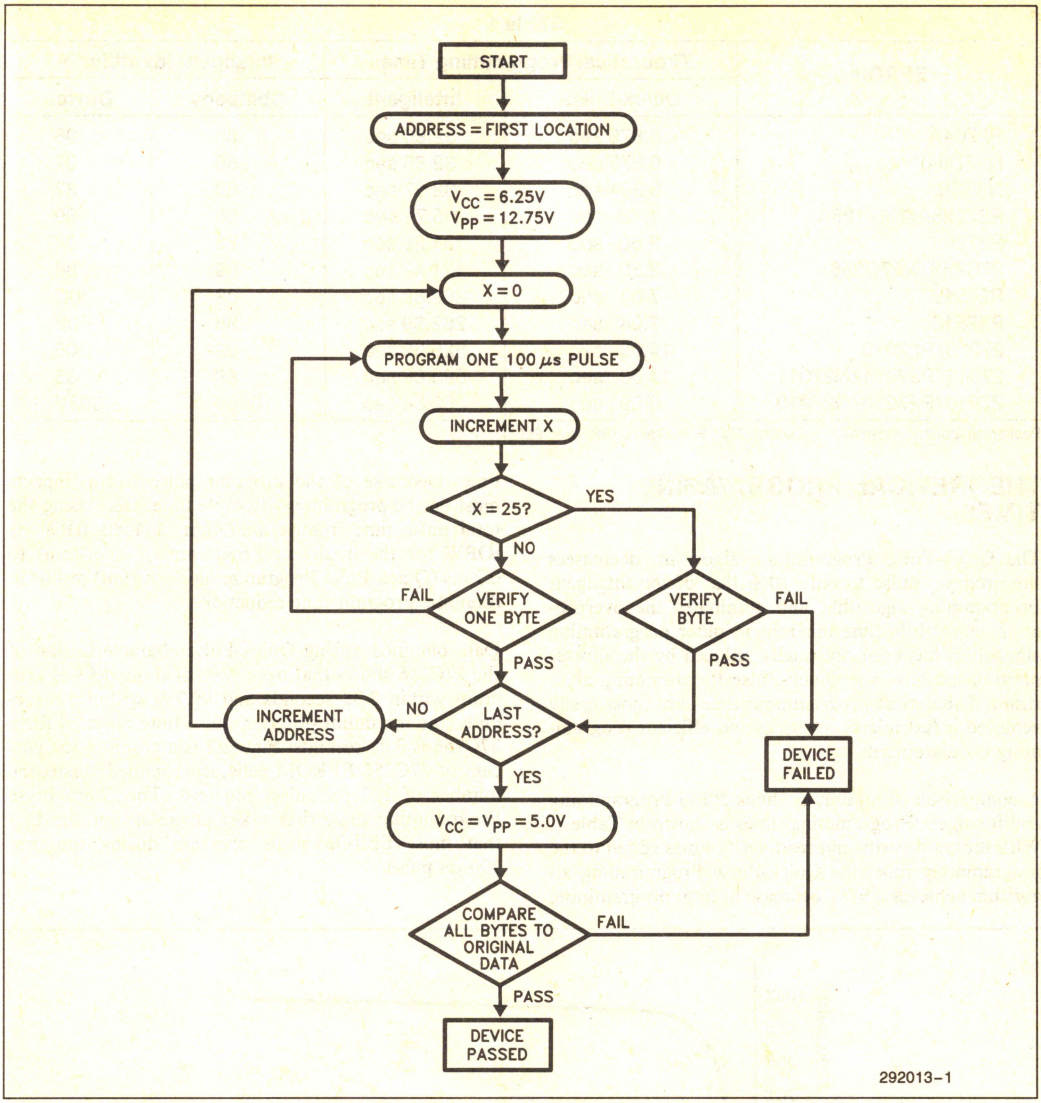


Figure 1. Quick-Pulse Programming™ Algorithm

QUICK-PULSE PROGRAMMING CHARACTERISTICS

The Quick-Pulse Programming algorithm uses a higher VPP voltage than the int$_e$ligent Programming algorithm to provide greater programming energy. This leads to faster programming. Overprogramming pulses are eliminated by using a higher reference level to check cell charge margin. At the beginning of the programming sequence, V_{CC} is raised from 5.0V to 6.25V and V_{PP} from 5V to 12.75V. A 100 microsecond programming pulse is applied and immediately followed by a byte verification. Up to twenty-five program/verify cycles are provided per byte before a programming failure is recognized. When all bytes are programmed, V_{CC} and V_{PP} are lowered to their 5.0V read mode voltages. All bytes are then compared with the original data to confirm proper programming. A flowchart of the Quick-Pulse Programming algorithm is shown in Figure 1.

Table 1

EPROM	Theoretical Programming Times		inteligent Identifier™	
	Quick-Pulse	Inteligent	Company	Device
P2764A	0.875 sec	32.86 sec	88	08
N27C64	0.875 sec	32.86 sec	88	07
N87C64	0.894 sec	32.87 sec	88	37
P27128A/N27128A	1.75 sec	65.71 sec	88	89
P27256	3.50 sec	131.29 sec	88	04
27C256/N27C256	3.50 sec	131.42 sec	89	86
P27512	7.04 sec	262.89 sec	88	0D
P27513	7.04 sec	262.89 sec	88	0F
27010/P27010	14.00 sec	525.69 sec	89	05
27011/P27011/N27011	14.00 sec	525.69 sec	89	85
27210/P27210/N27210	6.99 sec	262.84 sec	0089	00FF

Packaging Options: No prefix = Ceramic DIP, P = Plastic DIP, N = PLCC.

THEORETICAL PROGRAMMING TIMES

The Quick-Pulse Programming algorithm decreasees the program pulse to only 10% that of the inteligent Programming algorithm and eliminates the overprogram pulse. Idle time inherent in older programming algorithms has been drastically reduced by the shorter program pulse of the Quick-Pulse Programming algorithm. Theoretical programming times are most easily achieved if fast microprocessors and efficient programming code are used.

A comparison of minimum Quick-Pulse Programming and inteligent Programming times is shown in Table 1. With program-verify and read-verify times added to the programming time, the Quick-Pulse Programming algorithm achieves a 97% decrease in total programming time. Decrease of the program pulse width impacts most on the program/verify cycle time. Decreasing the total pulse time from a minimum of 4 ms (tPW + tOPW for the inteligent Programming algorithm) to 0.1 ms (Quick-Pulse Programming algorithm) results in dramatic program time reduction.

Data obtained during Quick-Pulse characterization of the 27C256 shows that over 87% of these devices program within 3.38 seconds and 99.7% within 5.8 seconds; the minimum program pulse time required for a 27C256 is 3.28 seconds. Figure 2 is a graph of the percent of 27C256 EPROM cells programmed versus the number of 100 μs pulses required. The Quick-Pulse Programming algorithm takes advantage of the fact that most EPROM cells program during the first 100 μs pulse.

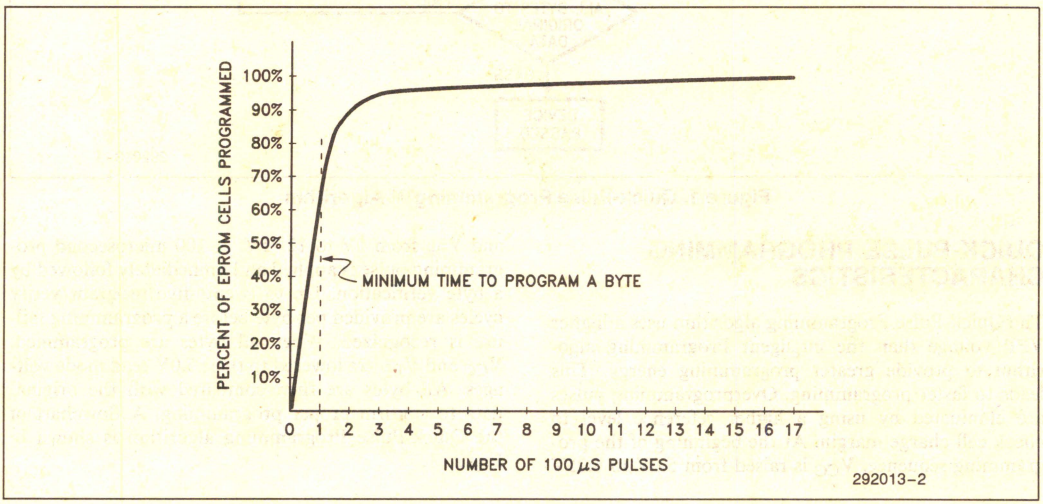


Figure 2. Pulses Required to Program 27C256 EPROM Cells

STORING DATA IN THE EPROM

The EPROM storage cell consists of a single MOS transistor with a floating gate (made of a layer of polysilicon surrounded by oxide layers) placed between the select gate and the substrate's diffusion layer. Figure 3 shows a simplified cross section of an EPROM cell. Data, representing a logic "0", is stored in the cell by placing electrons on the floating gate. The polysilicon-oxide interface creates a 3.1 eV potential barrier that traps these electrons on the floating gate. The absence of electrons on the floating gate represents an unprogrammed state; a logic "1".

Electrons are removed from the floating gate by exposure to ultra-violet (U.V.) light of wavelength 2537Å. Photons contained in the high frequency U.V. light are absorbed by these electrons. This places the electrons in a high energy state which allows them to overcome the 3.1 eV energy barriers of the interpoly oxide and gate oxide. With this energy the electrons are able to reach the Poly-2 layer (select gate) or substrate where they are removed from the cell.

Just as removing electrons (erasing) requires overcoming the energy barriers imposed by the gate oxide, programming requires energy to move electrons in the opposite direction. Placing a high voltage, V_{PP}, on the select gate and on the drain of the transistor allows programming (see figure 4). This potential causes electrons to be accelerated as they move from the source to the drain. Some of these electrons reach a high enough energy state to be drawn onto the floating gate.

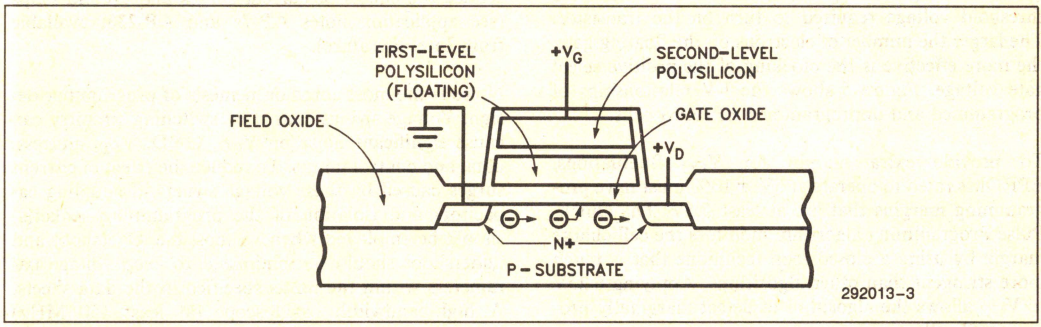


Figure 3. EPROM Cell

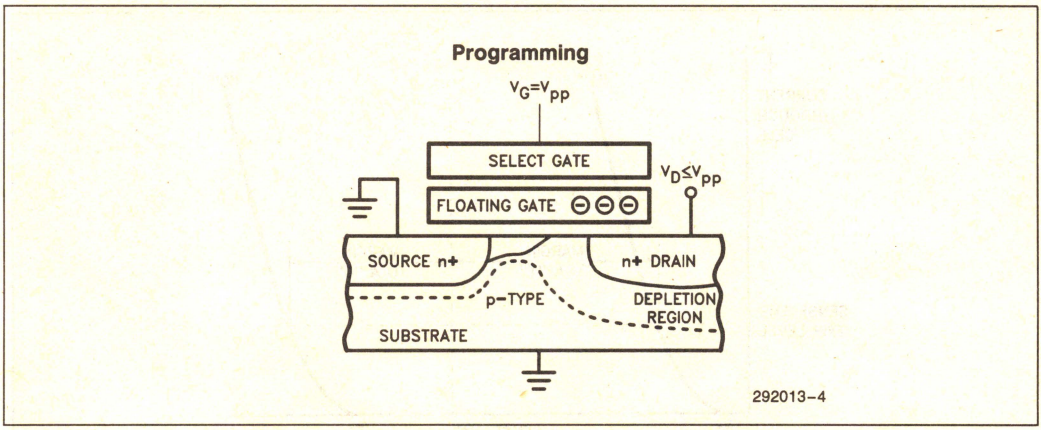


Figure 4. Programs Via Hot Electron Injection From Drain Depletion Region

More efficient programming of an EPROM cell is achieved by increasing the programming voltage, V_{PP}. As the programming voltage increases, the energy supplied to electrons as they accelerate through the channel increases. This energy allows "hot electrons" to overcome the potential barrier of the gate oxide. Since increasing the V_{PP} voltage makes for more efficient programming, the time required to place charge on the floating gate decreases. The Quick-Pulse Programming algorithm takes advantage of this.

Data stored in an EPROM cell is represented by the threshold voltage required to turn on the MOS transistor. In the Read Mode, information is requested from a cell by placing a voltage approximately equal to V_{CC} on the select gate. If the transistor turns on, a logic "1" is interpreted; if the transistor remains off, a logic "0" is detected. Programming an EPROM cell alters the threshold voltage required to turn on the transistor. The larger the number of electrons on the floating gate, the more effective is the blocking of the positive select gate voltage. Figure 5 shows the I-V relationships of programmed and unprogrammed EPROM cells.

To provide extra margin for V_{CC} fluctuations, EPROMs rated to operate at 5V ± 10% must have programming margins that are at least 5.5V. The Quick-Pulse Programming algorithm monitors the cell charge margin by using a closed loop technique that is much more stringent than other algorithms. Applying 6.25V to V_{CC} allows the algorithm to detect marginally programmed cells.

PROGRAMMER DESIGN PRACTICES

Reliable programming of EPROMs requires more than just an efficient algorithm. Good design practices should be followed when designing a PROM programmer to ensure that timing parameters, voltage parameters, and sequencing of control signals are properly implemented.

The power supply that drives the EPROM to its programming levels should be well regulated. Circuit board traces should be short, low-inductance lines that are decoupled at V_{CC} and V_{PP} device inputs with high-frequency capacitors; typically 0.1 μF ceramic capacitors. In addition, a 4.7 μF electrolytic capacitor should be used between V_{CC} and GND for every eight devices. Planes for routing V_{CC} and GND should be used to reduce the effects of current surges and ground loops (see application notes AP-74 and AP-238, available from Intel literature).

Noise is the most common nemesis of programmer design. Voltage swings caused by switching circuitry can cause significant noise on V_{CC}, GND, V_{PP}, address, data, and control inputs. To reduce the effect of current surges caused by these voltage swings, decoupling capacitors and isolation of the programming socket(s) should be employed whenever possible. Overshoot and undershoot should be minimized to keep voltage parameters within the limits specified in the data sheets. A high-bandwidth oscilloscope (at least 150 MHz) should be used to monitor the signals at the programming socket (with EPROM inserted).

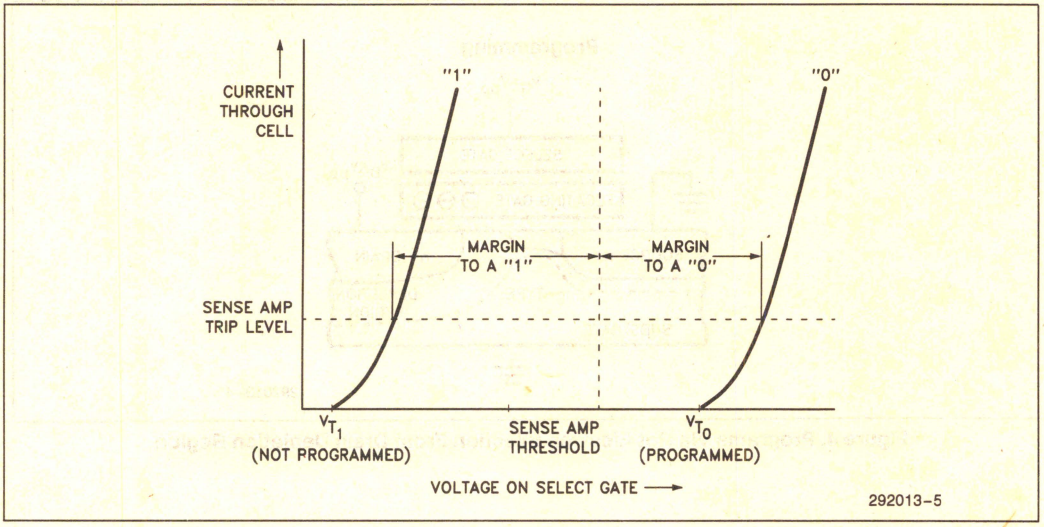


Figure 5. Read Operation

Since V_{PP} is the highest voltage applied to an EPROM, it is closest to the physical limits of the device. A V_{PP} voltage above 14.0V for any length of time will cause permanent damage to the EPROM. Proper decoupling capacitors should be placed at all V_{PP} inputs to help prevent damage caused by transients. Again, a high-bandwidth oscilloscope should be used to look for overshoot when adjusting V_{PP}.

Clean switching of V_{CC} and V_{PP} voltages will help ensure proper programming. Circuits for switching these voltages are easily built. Article reprint AR-294, which can be ordered from Intel's literature department, has example circuits that can be used to cleanly switch V_{CC} and V_{PP} from 5V to their programming voltages. These switching circuits also allow V_{CC} and V_{PP} to be switched off so EPROMs are not hot-socketed when they are inserted and removed.

SUMMARY

Production of electronic equipment requires programmable memory devices that can be used in auto-test and auto-insertion machines. Electronic systems also require program memory that can be changed easily when code crashes or program errors occur. Plastic and PLCC EPROMs provide solutions to both of these needs. They can be used in automated test and manufacturing equipment, and code changes can be implemented immediately. To reduce the programming times of these devices to accommodate production-line speeds, Intel has developed the Quick-Pulse Programming algorithm. Intel's line of plastic EPROMs can now be tested, quickly programmed, and mounted on circuit boards by totally automated production equipment.

intel

APPLICATION NOTE

AP-284

November 1986

Using Page-Addressed EPROMS

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Order Number: 292020-001

INTRODUCTION

For several years, eight-bit systems have been a mainstay of computerized systems. There are some very good reasons for this. The instruction sets of most 8-bit microprocessors and microcontrollers are very rich. Basic operations—move, jump, arithmetic, and logical—are common to all. These CPUs can perform the vast majority of functions available in later generation processors, but at a different performance level. 8-bit machines are entrenched in thousands of applications and are more than adequate for many new ones. So, why are 16-bit processors replacing their smaller cousins in new systems?

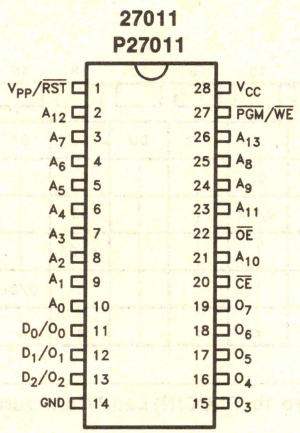
Part of the reason, of course, is the more powerful data manipulation made possible by the wider word width. Many 8-bit systems, however, are redesigned with 16-bit processors simply because extended memory addressing capability is needed. Most existing 8-bit systems function adequately, but 64 kilobytes of memory addressing is too small to accommodate RAM and constantly maturing program memory. The instruction sets of 8-bit processors usually suffice for new applications as well, except for the address constraint. Many 16-bit systems have predefined segments set aside for program memory. Additional program memory can not be expanded without intruding on RAM memory space.

Bank switching is a good way of providing additional program memory to address limited systems. A few logic gates, latches, decoders, ample circuit board space, and a lot of memory chips allow designers to provide virtual program memory capability to any system. This solution, although not ideal, can be implemented in new designs, but what happens when an existing design requires additional program memory? Board real estate is non-existent and a hardware redesign to implement bank switching is a very costly proposition.

An ideal solution to this problem would be one that implements a form of bank switching with no extra hardware, not even additional memory devices. An even better solution would allow for future growth in the system's program memory.

This "no extra hardware" expansion of program memory is now possible with Intel's page-addressed (paged) EPROM family. These devices allow 8-bit, 16-bit, 32-bit, . . . systems utilizing 27128 EPROMs to quadruple or octuple their program memory space with only a plug-in replacement. In addition, the page addressing scheme allows for future density upgrades to 4 Megabytes! within the same 28-pin (32-pin PLCC) footprint. Figure 1 shows the pin configurations for paged EPROMs and their relationship to other 28-pin DIP and 32-pin PLCC EPROMs.

4 M-bit	2 M-bit	27513	27128A
$V_{PP}/\overline{RST}$	$V_{PP}/\overline{RST}$	$\overline{RST}$	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
D_0/O_0	D_0/O_0	D_0/O_0	O_0
D_1/O_1	D_1/O_1	D_1/O_1	O_1
D_2/O_2	D_2/O_2	O_2	O_2
GND	GND	GND	GND



292020-2

27128A	27513	2 M-bit	4 M-bit
V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{PGM}$	$\overline{WE}$	$\overline{PGM/WE}$	$\overline{WE}$
A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	D_4/O_4
O_3	O_3	D_3/O_3	D_3/O_3

Figure 1a. Cerdip(D)/Plastic(P) DIP Pin Configurations

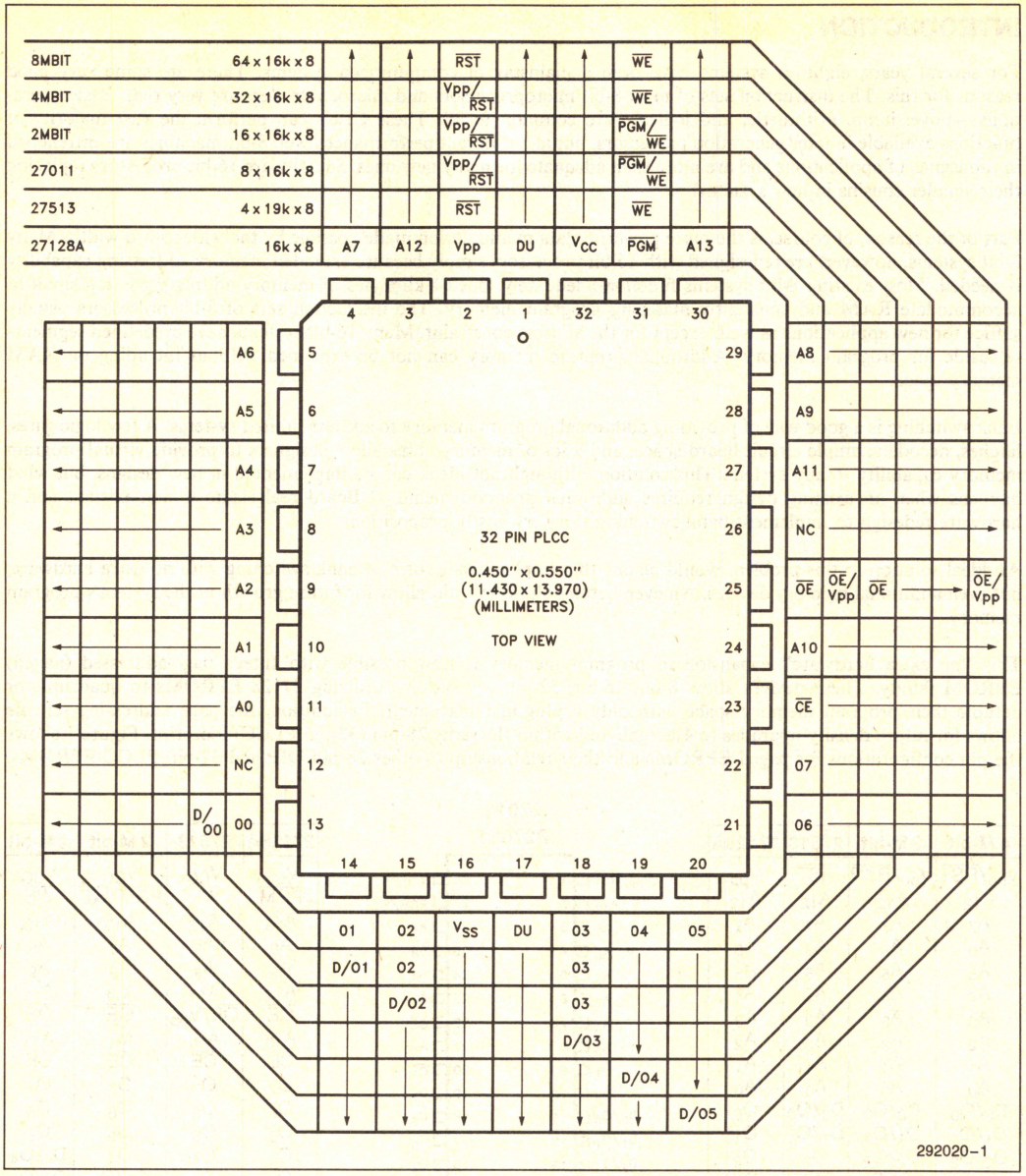


Figure 1b. PLCC(N) Lead Configuration

The 27513 is a 64 kilobyte EPROM organized as four 16 kilobyte pages that fits within a single 16K address space. Address-constrained applications that require more than 64K of program memory can benefit by using Intel's 1 megabit (128K byte) page-addressed EPROM, the 27011. The 27011 provides eight 16K pages within a single 16K memory space and is fully hardware compatible with the 27128 and 27513 EPROMs. Figure 2 shows the block diagram of paged EPROMs. Refer to data sheets for further details.

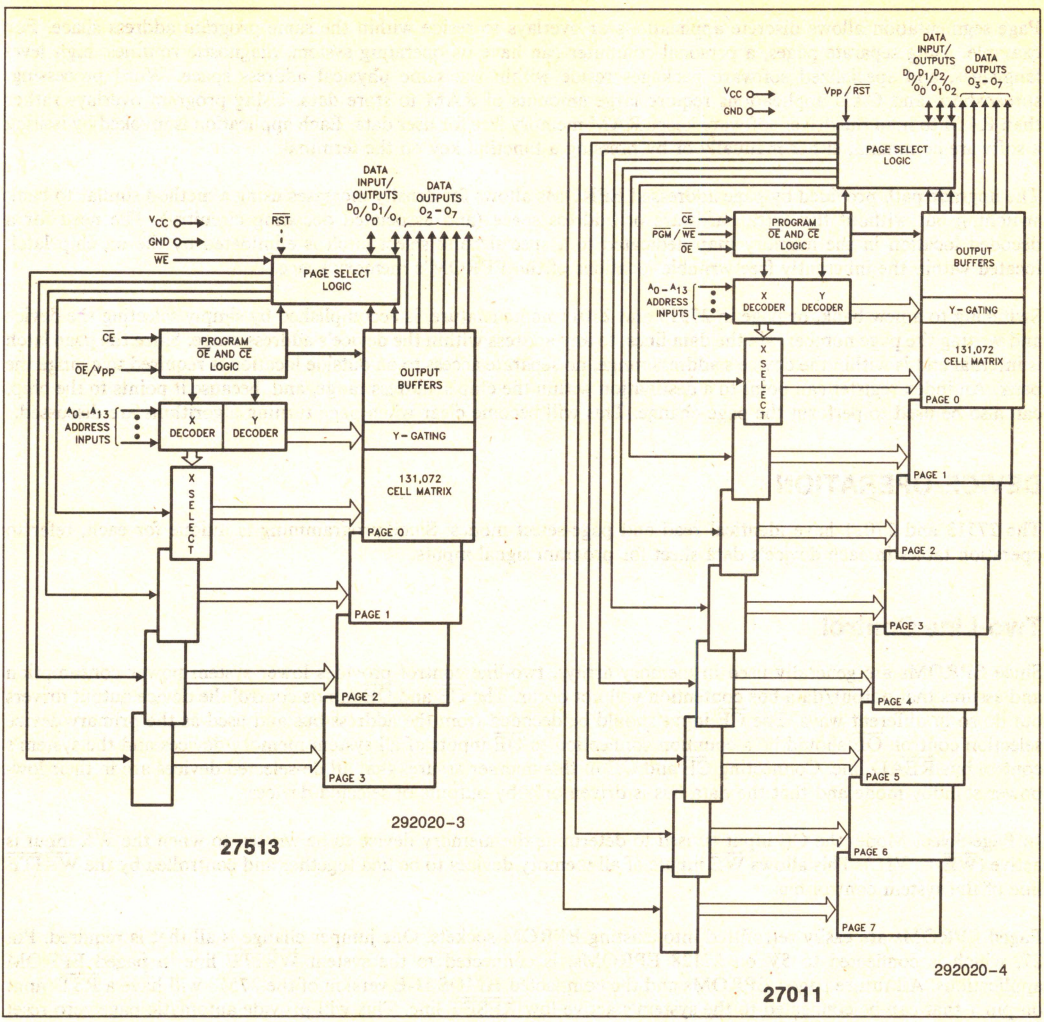


Figure 2. Block Diagrams

Page selection allows large programs of up to 64 kilobytes (27513) or 128 kilobytes (27011) to reside within a 16K address space. For 8-bit systems, extensive programs that would normally consume the entire memory space can be compressed within a 16K space leaving the remaining 48K for RAM memory. Program memory boundaries that may be predefined in 16-bit systems need no longer restrict the size of firmware.

Page segmentation allows discrete applications or overlays to reside within the same program address space. For example, using separate pages, a personal computer can have its operating system, diagnostic routines, high level languages, and specialized software packages reside within the same physical address space. Word processing, spreadsheet, and CAD applications require large amounts of RAM to store data. Using program overlays rather than RAM to hold the driver software keeps RAM memory free for user data. Each application is invoked by issuing a software command, either manually or by pressing a function key on the terminal.

The upgrade path provided by page addressed EPROMs allows for density increases using a method similar to bank switching but without the extra hardware or address space (and associated decoding circuitry). The need for a decoded location in the memory map dedicated to a special bank select latch is eliminated by the on chip latch located within the inherently free writable locations of the EPROM's memory space.

Switching to a new bank, or page in 27513 and 27011 nomenclature, is accomplished by simply selecting the device and writing the page number, via the data lines, to any address within the device's address range. Since the page latch is internal and is within the device's address range, no separate access to an outside location is required to change the bank. An index register can point to a destination within the chip's address range, and, because it points to the chip, can also be used to perform the page change. This will become clear when page turning algorithms are discussed.

DEVICE OPERATION

The 27513 and 27011 have identical read and page-select modes. Since programming is unique for each, refer to operation tables in each device's data sheet for program signal inputs.

Two-Line Control

Since EPROMs are generally used in memory arrays, two-line control provides lower system power consumption and assures that output/data bus contention will not occur. The $\overline{CE}$ and $\overline{OE}$ inputs control the device output drivers but do so in different ways. The $\overline{CE}$ input should be decoded from the address bus and used as the primary device selection control. $\overline{OE}$ should be a common connection to $\overline{OE}$ inputs of all system memory devices and the system's control bus $\overline{READ}$ line. Connecting $\overline{CE}$ and $\overline{OE}$ in this manner assures that all de-selected devices are in their low-power standby mode and that the data bus is driven only by outputs of selected devices.

In Page-Select Mode, the $\overline{CE}$ input is used to determine the memory device to be written to when the $\overline{WE}$ input is active ($\overline{WE}$ = VIL). This allows $\overline{WE}$ inputs of all memory devices to be tied together and controlled by the $\overline{WRITE}$ line of the system control bus.

Paged EPROMs are easily retrofitted into existing EPROM sockets. One jumper change is all that is required. Pin 27, which is connected to 5V on 27128 EPROMs, is connected to the system $\overline{WRITE}$ line in paged EPROM applications. All future paged EPROMs and the compacted HMOS II-E version of the 27513 will have a $\overline{RST}$ input on pin 1 that can be connected to the system's active low $\overline{RESET}$ line. This will provide automatic page zero reset when the system is reset. See Figure 3 for these connections.

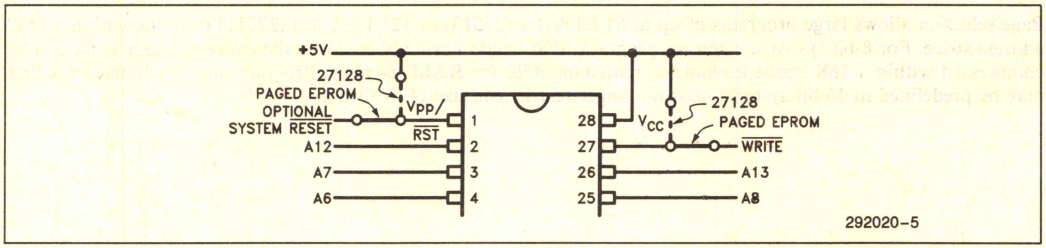


Figure 3. Single Jumper Change for Paged EPROM in Read and Write Modes

STANDBY and CHIP ENABLE Modes

Standby mode reduces the maximum EPROM current whenever data is not required from the EPROM. Standby mode is entered any time $\overline{CE}$ is at a TTL-high. All other mode select inputs ($\overline{OE}$ and $\overline{WE}$), are don't care, and outputs are in a high impedance state. The active mode ($\overline{CE}$ = VIL) allows the EPROM to enter the read, page-select, or program modes.

READ Mode

Information is obtained from the EPROM when it is placed in the read mode. This mode is entered when the device is selected ($\overline{CE}$ = VIL), the page-select (or write) mode is disabled ($\overline{WE}$ = VIH), and the outputs are enabled ($\overline{OE}$ = VIL). Outputs of all memory devices in the system can be connected directly to the data bus. Two-line control ensures that bus conflict is avoided by enabling only the outputs of the selected device.

PAGE-SELECT (WRITE) Mode

The page-select (or write) mode is entered by applying a TTL-low signal to the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs. This mode allows for random access to any page. Individual page selection is accomplished by selecting the chip ($\overline{CE}$ = VIL) and writing ($\overline{WE}$ = VIL) the page number, via the data inputs, to the device ($\overline{OE}$ = VIH). Table 2 shows the data required to perform a page change. When a page change occurs in the middle of a program sequence, the processor's program counter status must be considered. After a page-select write, the program counter will point to the physical location immediately following the write instruction. Since this location is on a new page, it contains code that may not be valid for program continuation. Therefore, proper sequencing of the page change events is necessary. Procedures to accomplish this are described in later sections of this application note.

Table 1. Page Selection Data

Input/Output Page Selection			D_2/O_2	D_1/O_1	D_0/O_0
27011	27513	Select Page 0	V_{IL}	V_{IL}	V_{IL}
		Select Page 1	V_{IL}	V_{IL}	V_{IH}
		Select Page 2	V_{IL}	V_{IH}	V_{IL}
		Select Page 3	V_{IL}	V_{IH}	V_{IH}
		Select Page 4	V_{IH}	V_{IL}	V_{IL}
		Select Page 5	V_{IH}	V_{IL}	V_{IH}
		Select Page 6	V_{IH}	V_{IH}	V_{IL}
		Select Page 7	V_{IH}	V_{IH}	V_{IH}

Automatic Page-Latch Clear

To ensure a consistent starting point for systems using a paged EPROM in the boot-up memory space, an automatic page-latch clear circuit has been included. As the V_{cc} supply voltage ramps above 4V to its operating voltage, the page-latch is reset to zero. This latching voltage provides an additional 500 mV safety margin to guard against spurious page-latch clearing due to noise in systems operating with ±10% V_{cc} supply.

During power-up, the state of control, address, and data outputs from the microprocessor should be considered when the automatic page-latch clear feature is used. If, during power-up, the processor's write line is in a TTL-low or an indeterminate state and address lines are such that the paged EPROM is selected, a spurious write of an undesired page number can occur. In most cases, spurious page writes during boot-up can be avoided by connecting a pull-up resistor (1K to 10 KΩ) between the $\overline{WE}$ pin and V_{cc}.

Relative Addressing

At power-up the device is automatically reset to page zero allowing program execution to begin from a known location in the EPROM memory. For example, 8085 systems automatically begin execution at location 0000H on page zero and continue sequential operation until the 16K page boundary is encountered. At that time, a program sequence can change the EPROM to page 1 and reset the program counter to 0000H allowing program execution to continue on the new page. This means that all address locations within the paged EPROM are relative to the base address of the device (in this case location 0000H). Jumps and calls within a page are easily accomplished using relative addressing, as opposed to absolute addressing. This is consistent with modular programming techniques and allows for flexible code structure in the paged format.

DEVICE PROGRAMMING

The programming mode is entered when the V_{pp} input is at its programming voltage. A byte of data is stored when the programming input is pulsed to a TTL-low. Data to be programmed is applied 8 bits in parallel to the data output pins. Levels required for the address and data inputs are TTL. Refer to data sheets for parameters, algorithms, and programming inputs used to program paged EPROMs.

Program Inhibit

Programming of multiple paged EPROMs in parallel with different data is easily accomplished using the program inhibit mode. A TTL-high level on the $\overline{CE}$ input will prevent programming of a device. This allows normal chip enable circuitry to select the particular EPROM to be programmed. Except for $\overline{CE}$, and $\overline{OE}$ in certain gang programming applications, all control inputs and bus lines of parallel EPROMs may be common.

Program Verify

A verify (read) should be performed on the programmed bytes immediately following the program pulse to determine that they have been correctly programmed. Data is read with V_{cc} and V_{pp} at their programming voltages and $\overline{OE}$ and $\overline{CE}$ at VIL. See the data sheets for programming voltages and proper sequencing of device control inputs.

TYPICAL PAGED EPROM/8085 SYSTEM

Hardware

A first approach to understanding the hardware and software considerations for interfacing a paged EPROM to a microsystem can be seen by analyzing the operation of a single paged EPROM in an 8085 8-bit microprocessor system. Paged EPROMs are easily incorporated into 16-bit systems by using techniques similar to those described below for 8-bit systems. Also, see Appendix D for an example that uses paged EPROMs in an 8086 system. Figure 4 shows the configuration of a basic 8-bit system.

System boot-up during power-up initializes the EPROM to page zero. This automatic feature of the page-latch circuit is meant to ensure consistent page selection when power is first applied. Similar to other microprocessors, the 8085 begins program execution at location 0000H after power-on or reset. Bootstrap initialization or vectoring routines should be located at 0000H of page 0.

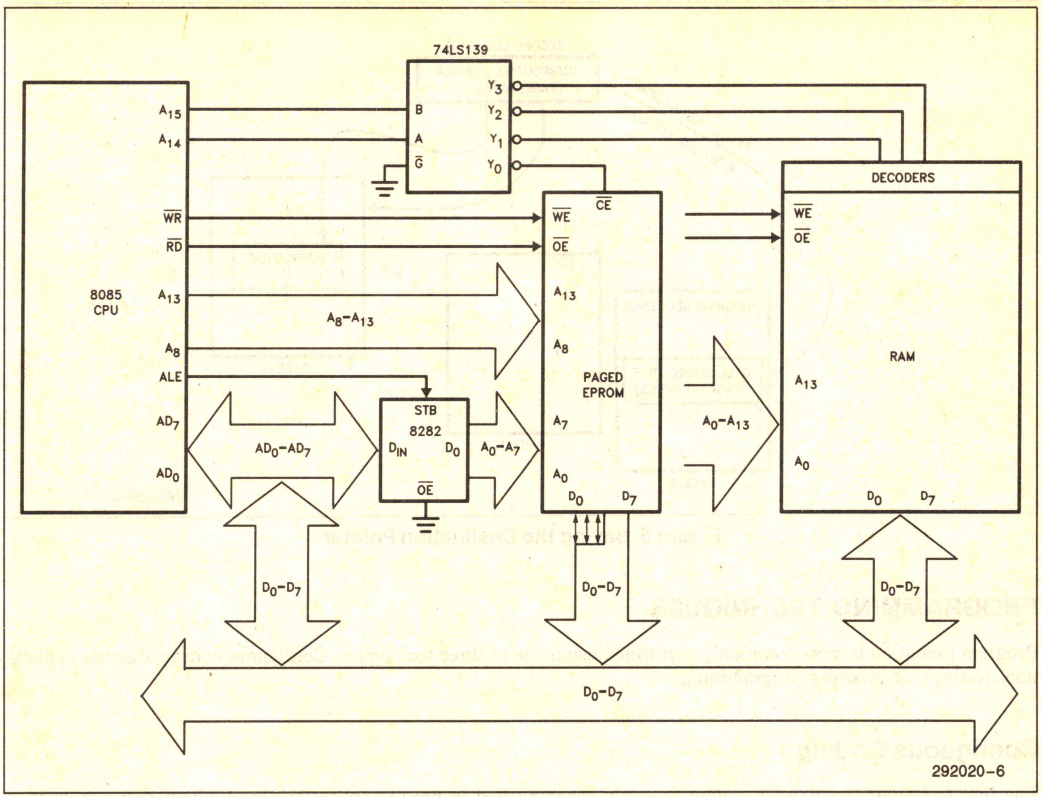


Figure 4. Basic 8-bit Microsystem

Unlike power-up, a hardware reset or software "RST" command will not automatically select page zero on early 27513 versions. A simple software routine can be placed at location 0000H of other pages to accomplish page 0 selection. A two line (6 byte) sequence to select page 0 is:

```
0000  MVI  H,0000H    ;HL register points to reset location.
0003  JMP  TURNTO_0   ;Jump to routine that changes to page
                      ;0 and begins execution at location
                      ;0000 (HL register).
```

Page selection routines are discussed in the next section.

Software Page Selection

Performing a page change involves proper sequencing of two events: 1) selecting the new page and 2) moving to the appropriate relative location on it. Although this sounds simple, which step should be performed first? After the first step is executed, how is the other performed if information about it resides on the page just left by the program?

The solution is a two-fold approach that 1) places the relative destination in a secure location where it can be retrieved no matter what page or what location is pointed to by the program counter, and 2) continues the program flow on the new page as if no page change had occurred (see Figure 5). Following is a discussion of methods for implementing these steps in a simple 8-bit (8085) microprocessor driven system. Keep in mind that these same techniques can be used when paged EPROMs are incorporated in word-wide systems.

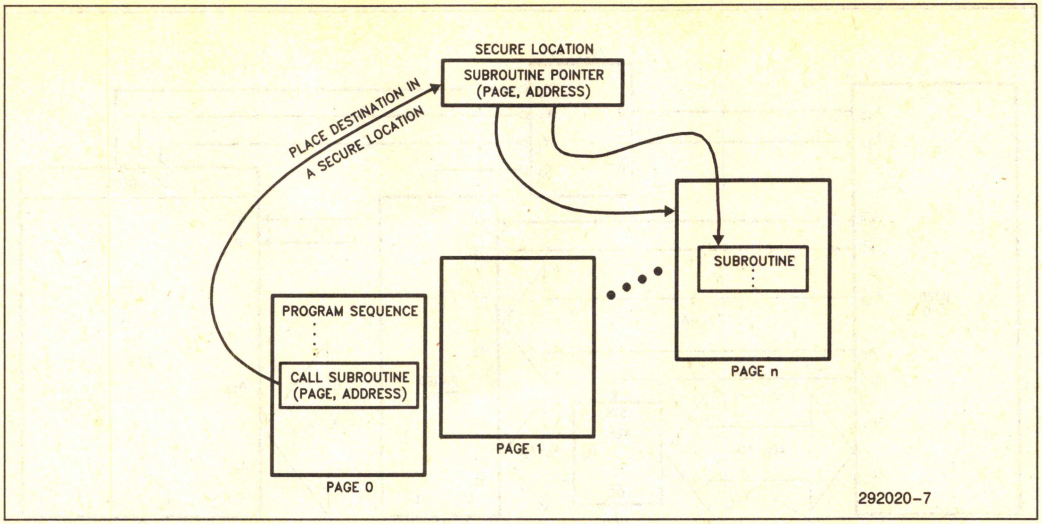


Figure 5. Saving the Destination Pointer

PROGRAMMING TECHNIQUES

Program execution is most commonly performed using one of three techniques: Contiguous coding, discrete application overlays, or modular programming.

Contiguous Coding

The first technique, contiguous coding, is easily accomplished in paged applications by duplicating a simple two-statement software routine at the beginning of each page. This routine writes the number of the next sequential page to the EPROM which changes the page and continues execution at the next relative sequential location on the new page. A one line jump statement at the end of a page boundary re-directs program execution to this page turning routine. For an 8085 system, the page turning routine would be as follows:

```
LOCATION   SOURCE      STATEMENT
0000       CHANGEPG    MVI A,next page number.
0002                   STA Any location within the EPROMs address range.
0005       program continuation
```

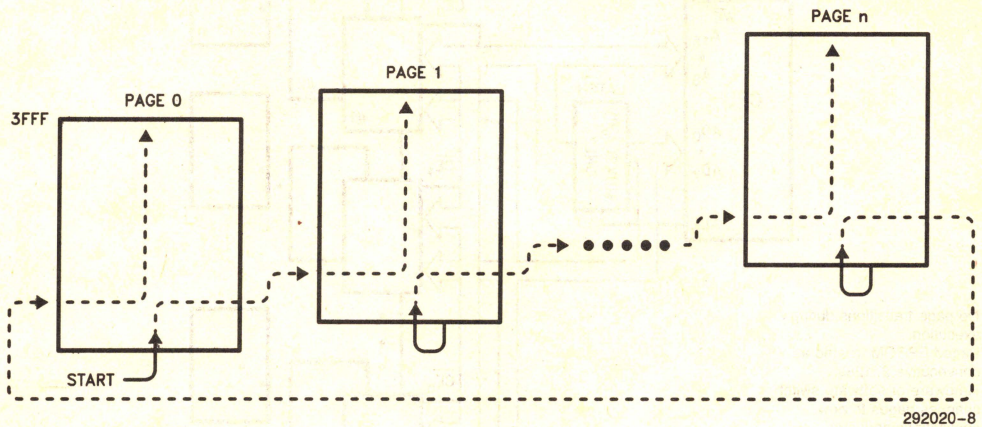
The following statement at the end of the page requests this routine:

```
3FFD       NEXTPG      JMP CHANGEPG
```

Although power-up automatically resets the EPROM to page zero, the page change instructions at the beginning of page zero cause the application software to begin execution at location 0000H on page one. Figure 6 illustrates this technique.

STRAIGHT LINE CODE

Issue: Page transitions during execution.
Solution: Paging instructions at the beginning and end of each page.
(Program counter must be reset to stay within 16K boundary)



Sample instructions for 8085:

			3FFD	C3
Beginning of page 0	JMP	0000	3FFE	00
			3FFF	00
			0000	3E
	MVI	A,01H	0001	01
End of page 0			0002	32
	STA	"PAGED EPROM"	0003 0004	} "PAGED EPROM"

—Program Execution Begins at Location 0005

Figure 6. Contiguous Coding

Discrete Applications

The second technique uses the paged EPROM in discrete application overlays. Each page contains all the system information required for individual software applications to stand alone in their control of system operation. A small section at the same location on each page is set aside to handle page-change routines. Another application is requested by a software or function key command that directs the microprocessor to the routine below.

```
APPONE   LXI  H,starting address of page 0 application.
         MVI  M,00H        ;"HL" (M) points to page 0. Next
                           ;instruction continues on page zero.
         PCHL              ;Jump to Application-one.
APPTWO   LXI  H,starting address of page 1 application.
         MVI  M,01H
         PCHL
         etc.
```

A block diagram for discrete system options is shown in Figure 7.

DISCRETE SYSTEM OPTIONS

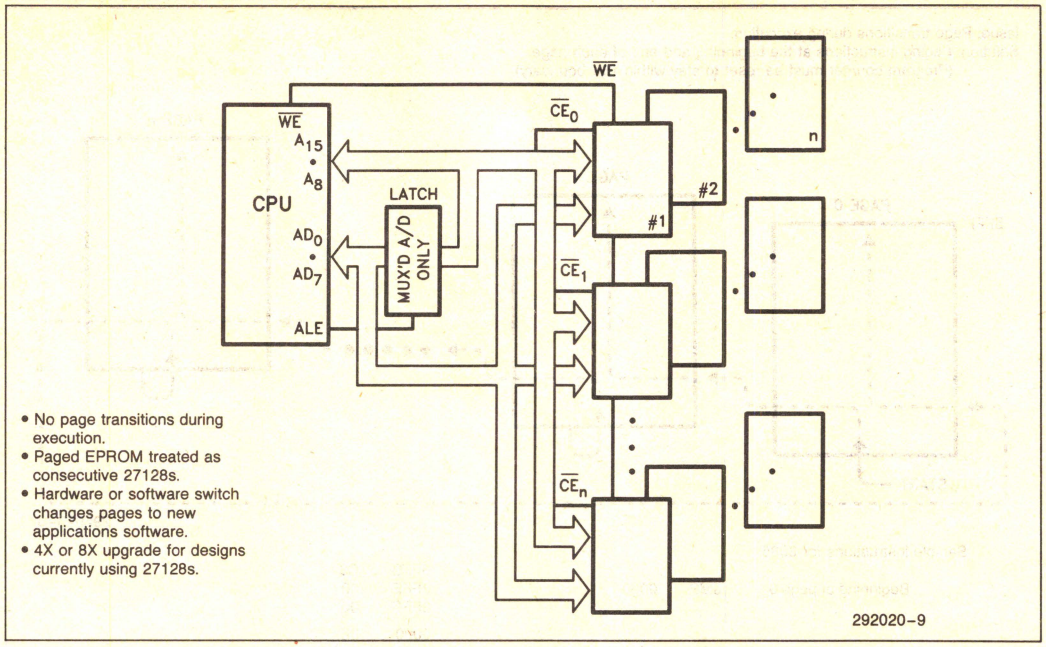


Figure 7. Paged EPROM's In Discrete Applications

Modular Programming

The third technique, modular programming, is a common and desirable means for implementing application software. This technique requires special considerations for paged EPROMs. Three algorithms for inter-page calls and jumps are discussed in the next section.

SYSTEM IMPLEMENTATION

Three page turning algorithms—Manual Paging, Automatic Paging, and Look-Up Tables—are summarized below in the context of three different hardware configurations—Paged EPROM only, Paged EPROM + Small EPROM, and Paged EPROM + RAM. An 8085 system is used for illustrative purposes, but these implementations can also be used with word-wide systems, except for algorithm 2 (Automatic Paging).

Algorithm 1 (Manual Paging) Summary: This algorithm relies on the ability of the programmer to determine the page and relative location that subroutines inhabit. These two pieces of information must be manually supplied when a subroutine on a different page is called.

Advantage:

- The most direct and most easily understood approach.
- Provides for fast page changes.
- Upgrades easily to megabit page-addressed EPROM applications.

Disadvantage:

- Programmer must know the page and relative location for every call and jump.
- Assembler won't supply this information and has trouble with labels that reference unknown addresses on another page.

Algorithm 2 (Automatic Paging) Summary: Automatic paging is applicable to the 27513 only in 8-bit (16-bit addressing) applications. This method allows the programmer to write code in a more conventional, sequential manner but at the expense of restricting the base address of the 27513 in the system's memory map. Programs are assembled as a contiguous sequence. The two most significant bits of a destination address are used to determine the page (one of four), and the remaining bits are used to determine the relative location on that page.

Advantage:

- While writing programs, the user does not need to know the page or relative location on that page of routines accessed by jumps or calls.
- Segmentation into 16 kilobyte pages is simple.

Disadvantage:

- A page change takes more time than Algorithm 1.
- The 27513 must reside at locations: 00000H, 04000H, 08000H, or 0C000H; no other locations are allowed.
- Upgrading to megabit densities in 8-bit systems is not possible.

Algorithm 3 (Look-up Tables) Summary: Code may be written in sequential or modular form. Global subroutines may be located on, and accessed from, any page by using indirect addressing. Actual page and relative address information of subroutines is located in a look-up table. When a call or jump is initiated, a pointer to the table information is used to extract the destination address.

Advantage:

- Fast access to global subroutines.
- Easy program assembly.
- Easy upgrades to megabit page addressed EPROM applications.

Disadvantage:

- Large look-up tables can occupy significant portions of memory.
- A page change takes a little more time than Algorithm 1.

Algorithm 1: MANUAL PAGING.

This page change algorithm allows for fast jumps and calls to another page. The page of residence for destinations must be determined by the user and supplied with each call and jump instruction. To implement this procedure, one register must be dedicated to the system for current page information and an index register pair must be made available at the time a call, jump, or return to/from a subroutine is made. In the following 8085 example, the "D" register contains the current page number, which is initialized to 00H (page zero) during boot-up, and the "HL" register points to the destination address. This group of routines must be located at the same relative address on every page.

```
SOURCE     STATEMENT
PAGE_0     PUSH      D                ;Save the current page number.
TURNTO_0   MVI       D,00             ;Change current page identifier.
           MOV       M,D              ;Writing the page number "D" to where
                                      ;"HL" points (EPROM) changes the page.
                     PCHL             ;Change Program Counter to begin at
                                      ;desired location on new page.
PAGE_1     PUSH      D
TURNTO_1   MVI       D,01
           MOV       M,D
           PCHL
           .
           .
           .
PAGE_n     PUSH      D                ;n=3 for the 27513,n=7 for the 27011.
TURNTO_n   MVI       D,n
```

```
        MOV     M,D
        PCHL
RETURN  POP     D               ;Retrieve old page number.
        POP     H               ;"HL" points to old return address.
        MOV     M,D             ;"HL" points to EPROM; Change the page.
        PCHL                    ;The program counter is loaded with the
                                ;return address.
```

Calling a routine on another page is accomplished by the programming sequence:

```
GETSUB  LXI     H,routine       ;Load "HL" with destination address.
        CALL    PAGE_n          ;Call the subroutine to turn to page
                                ;n=0, 1, 2, ... The CALL instruction
                                ;may be a conditional call since LXI H
                                ;does not affect the flags register.
```

Nested calls to any depth (limited only by the RAM space available to the system stack) are supported with guaranteed returns to the calling routine. One statement at the end of a subroutine will facilitate a return to the calling routine (to its proper page number). The usual return instruction (RET or conditional return) is replaced by

```
        JMP     RETURN          ;A conditional return would use its
                                ;equivalent jump cousin.
```

Jumps to a location on another page do not require that the current page or return address be saved. Only a page change and a jump to the destination are required. This is accomplished by the two program statements:

```
        LXI     H,destin        ;"HL" gets the destination address.
        JMP     TURNTO_n        ;Jump to the standard routine to turn
                                ;the page to n = 0, 1, 2, ... JMP may
                                ;be replaced by a conditional JMP.
```

Figure 8 shows the program flow during page changes.

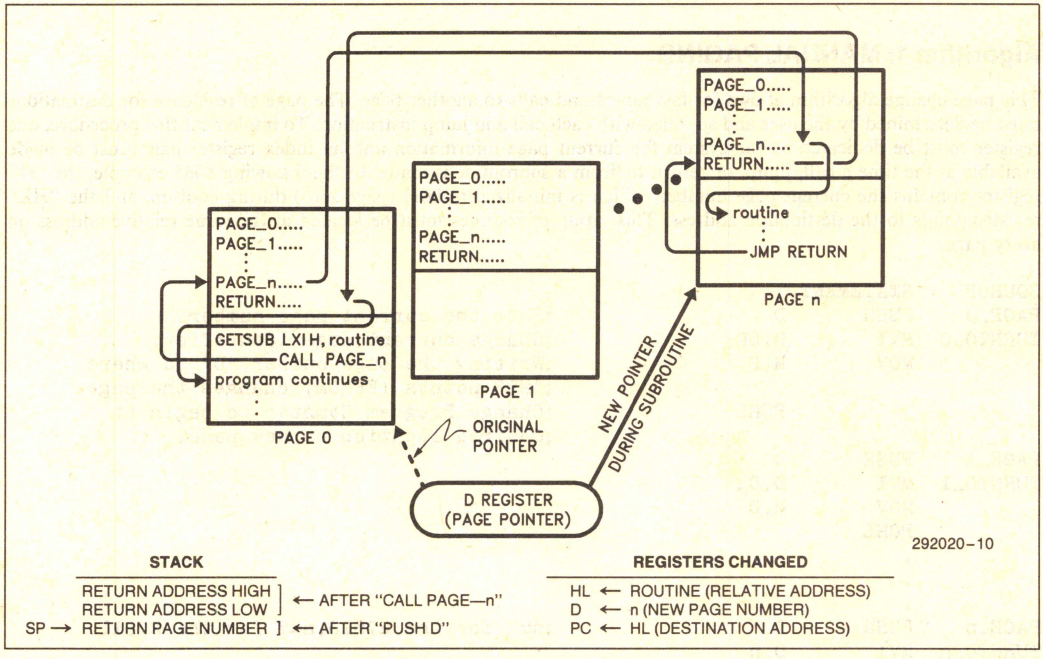


Figure 8. Changing Pages with Algorithm 1

Assembling the Program

Program assembly is a two-stage process. Program code for each segment (page) is written as a distinct 16K program; this anticipates assembly problems caused by duplicate addressing inherent in the stacked-page format. The first assembly of each page will generate an error for each label reference that does not reside on the assembled page. A master equate table can be formed by merging the equate tables of each page generated during the first round of assembly. This master table is then used to re-assemble all the pages.

Algorithm 2: AUTOMATIC PAGING (27513 only)

The second algorithm allows a programmer to write code in an uninterrupted manner and assemble the finished program as a single block (up to 64K) without having to discern the page on which a subroutine resides. Figure 10 shows the assembled code and its segmentation into separate pages. This is accomplished by using the two most-significant bits of a destination address as determined during normal assembly of the program. The two most-significant bits hold the page number information (one of four pages) and the remaining bits hold the relative location on the page of the desired routine. As described in Algorithm 1, calls and jumps to routines are not made directly. An intermediate step is required to move to another page. The following page change routine resides at identical relative locations on each page.

```
SOURCE    STATEMENT
PAGECALL  PUSH      D                ;Save old page number.
PAGETURN  PUSH      PSW              ;Save anything in "A".
          MOV       A,H              ;"A" gets high address byte.
          RLC       A                ;Rotate "A" to get two
          RLC       A                ;most-significant bits.
          ANI       00000011B        ;Reset bits 2-7.
          MOV       D,A              ;Bits 0 and 1 are the page number.
          MVI       A,00111111B      ;"A" gets mask bits.
          ANA       H                ;Strip off MS bits of "H".
          MOV       H,A              ;New high-address byte back to "H".
          MOV       M,D              ;Change the page of 27513.
          POP       PSW              ;"A" retrieves old information.
          PCHL                       ;Jump to new location.

RETURN    POP       D                ;Get old page number.
          POP       H                ;"H" gets return address.
          MOV       M,D              ;Change the page.
          PCHL                       ;Return to program.
```

The main concepts of this routine are:

1) Save the current page number.

2) Isolate the most-significant two bits in the "H" register which contain the page information.

3) Write these bits to the 27513 to change the page and save them in the current page pointer.

4) Reset the two most-significant bits of the HL register pair to zero to maintain relative addressing within the 16K range of the 27513; if the 27513's base address is other than 0000H, bits 6 and/or 7 must be set to "1" as required.

5) Jump to the relative location on the page (HL register).

The Page Changing routine is called by:

```
GETSUB    LXI       H,routine        ;"HL" gets routine's address as
                                     ;determined by the assembler.
          CALL      PAGECALL         ;Call the paging routine.
```

To return to the Calling routine:

```
          JMP       RETURN
```

Jumps to destinations on any page are accomplished by:

```
LXI     H,destin        ;"HL" gets address of routine as
                        ;determined by the assembler.
JMP     PAGETURN
```

Figure 9 shows the "bit stripping" sequence for calling a routine using Algorithm 2.

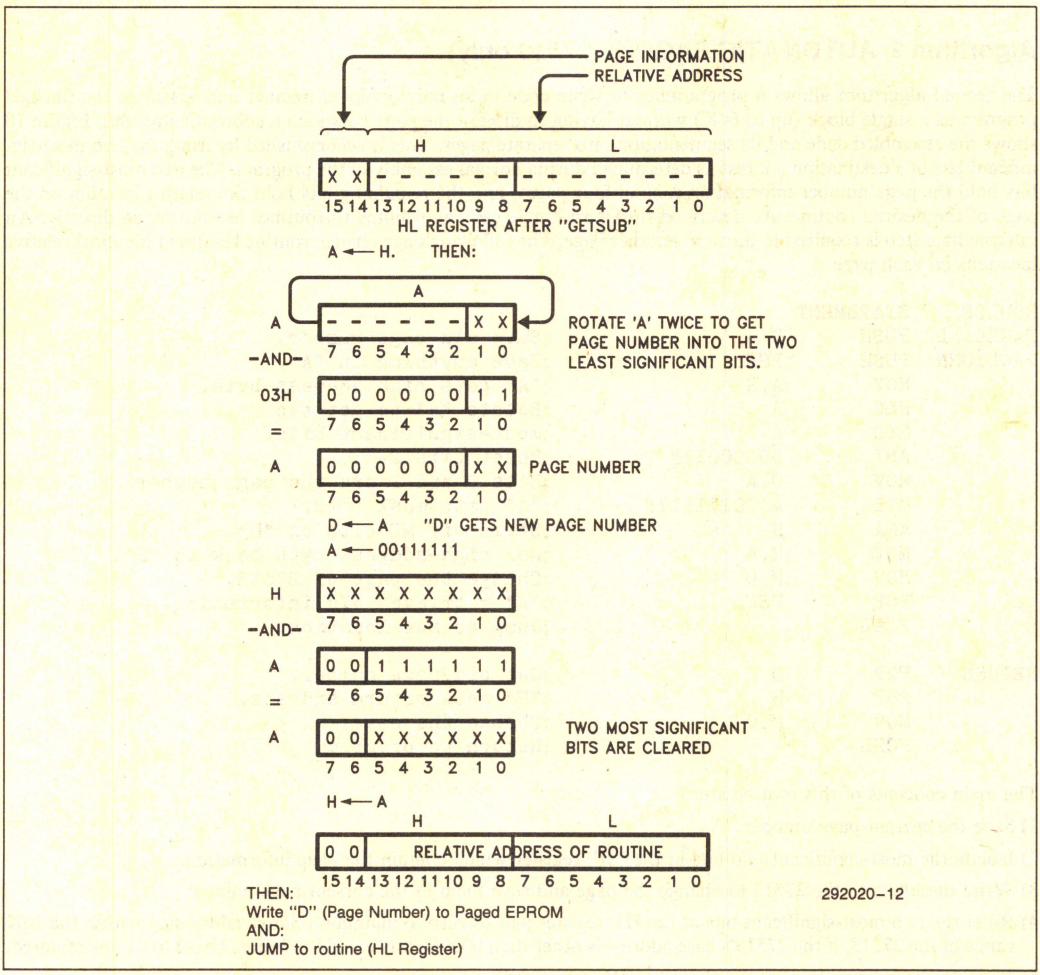
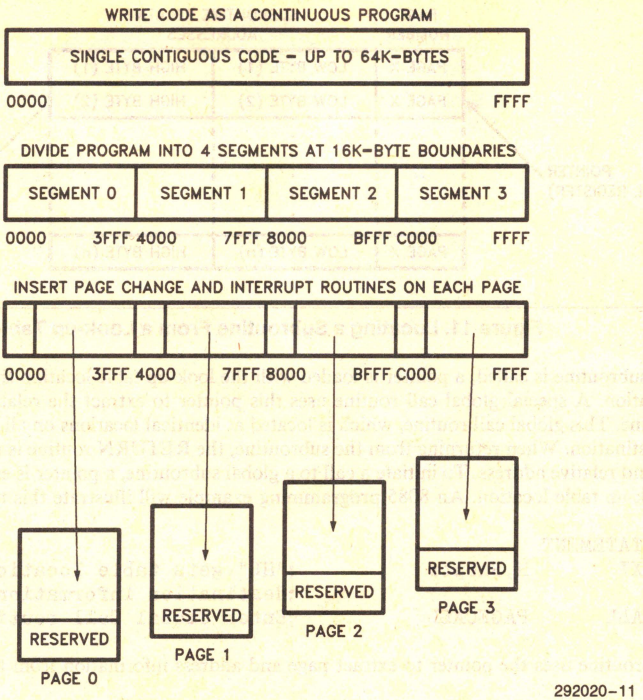

PAGE INFORMATION
RELATIVE ADDRESS
H
L
X X - - - - - - - - - - - - - - -
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
HL REGISTER AFTER "GETSUB"
A ← H. THEN:
A
A
X X
7 6 5 4 3 2 1 0
ROTATE 'A' TWICE TO GET PAGE NUMBER INTO THE TWO LEAST SIGNIFICANT BITS.
-AND-
03H
0 0 0 0 0 0 1 1
=
A
0 0 0 0 0 0 X X
PAGE NUMBER
D ← A "D" GETS NEW PAGE NUMBER
A ← 00111111
H
X X X X X X X X
-AND-
A
0 0 1 1 1 1 1 1
=
A
0 0 X X X X X X
TWO MOST SIGNIFICANT BITS ARE CLEARED
H ← A
H
L
0 0 RELATIVE ADDRESS OF ROUTINE
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
THEN:
Write "D" (Page Number) to Paged EPROM
AND:
JUMP to routine (HL Register)
292020-12

Figure 9. Changing Pages With Algorithm 2

Assembling the Program

Algorithm 2 allows code to be written using standard programming techniques. 64K of sequential code and subroutines can be written without the need to discern page and relative address information when calls and jumps occur. A section should be reserved at identical locations on each page for reset, interrupt, and page change routines (see Figure 10). Calls and jumps do not address destinations directly. Destinations (derived from subroutine label names as determined by the assembler) are loaded into the "HL" register, and the universal PAGECALL/PAGETURN routine (as described above) is called. The "bit stripping" routine takes care of page selection and relative addressing. RAM locations may be accessed directly. Even though their addresses appear to overlap program memory, no "bit stripping" takes place so RAM actually occupies a unique location.



Assemble Code and Place Each Segment Into a Page of the 27513

Figure 10. Assembling Code For Algorithm 2

Algorithm 3: LOOK-UP TABLES

Another technique that allows for random calls and jumps to routines on any page is to use a look-up table. Pointers to locations in a table containing destination addresses and page numbers are used to access subroutines. Two types of subroutines need to be considered in this technique—global and local. Global subroutines are located on any page of the EPROM and can be accessed from any other page. Local subroutines are located on the same page as the calling routines and can not be accessed from any other page. Local subroutines can be called directly and need not be accessed via a look-up table.

Page and relative address locations of global subroutines are assembled into a look-up table. Pointers are used to extract the location information from the table when calling these routines. Figure 11 shows the basic concept of the look-up table approach.

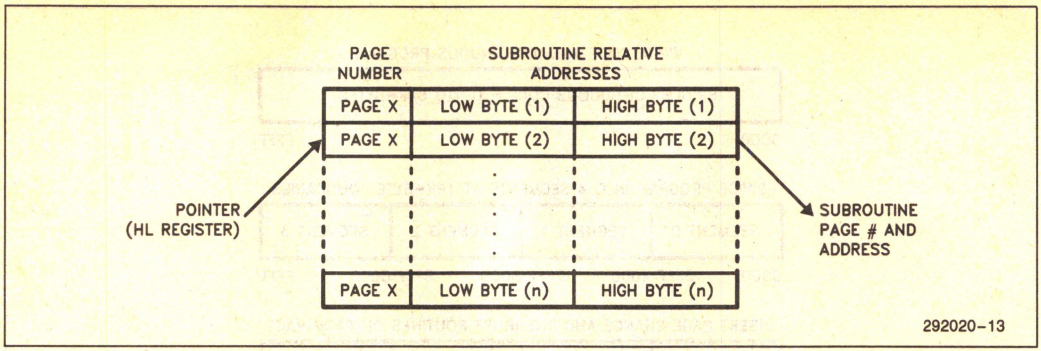


Figure 11. Locating a Subroutine From a Look-up Table

When a global subroutine is called, a pointer is loaded with the look-up table location that contains the subroutine's address information. A special global call routine uses this pointer to extract the relative address and page of the desired subroutine. This global call routine, which is located at identical locations on all pages, changes the page and jumps to the destination. When returning from the subroutine, the RETURN routine is used to change to the calling routine's page and relative address. To initiate a call to a global subroutine, a pointer is established that addresses the appropriate look-up table location. An 8085 programming example will illustrate this technique.

```
SOURCE    STATEMENT
GETSUB    LXI       H,Subptr          ;"HL" gets table location of
                                      ;destination information.
          CALL      PAGECALL          ;Enter Global Call routine.
```

The global call routine uses the pointer to extract page and address information from the look-up table.

```
PAGECALL  PUSH      D                 ;Save old page number.
PAGETURN  MOV       D,M               ;"D" gets destination page from table.
          INX       H                 ;"HL" points to destination's Low
                                      ;address byte in table.
          MOV       E,M               ;"E" gets destination Low byte.
          INX       H                 ;"HL" points to destination High
                                      ;address byte in table.
          MOV       H,M               ;"H" gets destination High byte.
          MOV       L,E               ;"L" gets destination Low byte.
          MOV       M,D               ;Change page.
          PCHL                        ;Jump to routine.

RETURN    POP       D                 ;Retrieve old page number.
          POP       H                 ;Get return address.
          MOV       M,D               ;Change page.
          PCHL                        :Return to program.
```

The RETURN routine is part of the global call routine and provides instructions for return to the calling program. The following statement is used to enter the RETURN routine at the end of a subroutine:

```
          JMP       RETURN
```

The look-up table can also be used when jumps are made to global routines. The following statements will accomplish this.

```
          LXI       H,Jmpptr          ;"HL" gets Table location of
                                      ;destination information.
          JMP       PAGETURN          ;Enter global jump routine.
```

The global call routine must reside at identical locations on each page. This keeps programming flow continuous when a page change occurs in the middle of an instruction sequence. Faster table look-up can be accomplished if identical copies of the look-up table are located on each page. If the table is large, memory space can be saved by locating the table on one page only. Extra instructions are required, however, to change the page to the look-up table's page.

Assembling the Program

Programs are written in a standard modular form. Calls and jumps to routines that reside on another page are done using indirect addressing. Rather than call the routine directly, a pointer is loaded (using a label) with the look-up table location and a call is made to the universal PAGECALL routine. After the program is assembled, destination page and relative address information is entered in the look-up table.

HARDWARE AND ALGORITHMS

The following diagram describes the contexts in which the three algorithms will be discussed. The matrix shows headings for software considerations and system configurations and where they are discussed. Also indicated is the preferred algorithm for a particular hardware/software implementation; the most efficient algorithm for the specific application is listed first if more than one algorithm applies.

SYSTEM CONFIGURATION		SOFTWARE CONSIDERATION Random Paging	Interrupts & Reset	Paging @ Page End	Discrete Overlays
PAGED EPROM ONLY	Heading	A1	A2	A3	A4
	Algorithm	2, 3, 1	2, 3, 1	1, 2, 3	1
	Page	17	18	19	19
PAGED + SMALL EPROM	Heading	B1	B2	B3	B4
	Algorithm	2, 3, 1	2, 3, 1	1, 2, 3	1
	Page	19	19	19	20
PAGED EPROM + RAM	Heading	C1	C2	C3	C4
	Algorithm	2, 3, 1	2, 3, 1	1, 2, 3	1
	Paged	20	20	20	20

System Hardware Configurations

Three configurations will be considered for page addressed implementation using an 8085 system to illustrate each. Word-wide systems use similar techniques (see the appendix for 8086 + Paged EPROM). The algorithms established above will be used to implement page turning for each system. These system configurations are:

A) Paged EPROM Only—located at location 0000H.

B) Paged EPROM + small EPROM—small EPROM placed at location 0000H, paged EPROM at a 16K boundary.

C) Paged EPROM + RAM—EPROM at location 0000H, RAM available anywhere in the memory space.

Within each of these three system configurations, four software considerations will be covered:

1) Paging and continuous program execution.

2) Interrupts and reset.

3) Crossing page boundaries.

4) Discrete programs on each page (preset overlays).

A) Paged EPROM Only

1) Paging and Continuous Programming

The paged EPROM must reside at the beginning of memory (or end of memory for systems that boot up at the top).

Page turning algorithms must reside at the same relative location on each page.

For continuous execution, place these statements at the end of each page:

Algorithm 1

```
        LXI     H,next page starting location
        JMP     TURNTO_n          ;n = page number.
```

Algorithms 2 or 3

```
        LXI     H, next page starting location
        JMP     PAGETURN
```

2) For interrupt and reset routines:

Page zero can contain the normal reset, boot-up and interrupt routines (or vectors) that would normally be placed at the beginning of memory in a 27128 EPROM. Other pages should contain the following statements.

Algorithm 1

```
0000    RESTART  LXI     H,0000H
0003             JMP     TURNTO_0
```

Algorithms 2 and 3

```
0000    RESTART  LXI     H,0000H
0003             JMP     PAGETURN
```

For interrupts (algorithms 2 and 3 shown, algorithm 1 is similar; PAGE_n replaces PAGECALL), the following should reside on each page.

```
0024    TRAP     LXI     H, address of Trap routine
0027             CALL    PAGECALL


002C    RST5.5   LXI     H,RST5.5 interrupt routine
002F             CALL    PAGECALL


0034    RST6.5   LXI     H,RST6.5 interrupt routine
0037             CALL    PAGECALL

003C    RST7.5   LXI     H, RST7.5 interrupt routine
003F             CALL    PAGECALL
```

Interrupt routines vectored to by an interrupt controller should have space reserved at the same locations on each page in a manner similar to the hardware restart routines shown above.

When returning from an interrupt, the normal return statement (RET or RETI) at the end of an interrupt service routine should be replaced by a jump to the RETURN routine.

```
Interrupt routine
:
:
:
INTRTRN   JMP              RETURN
```

The 8085 handles interrupts in a simple manner. An interrupt pushes the contents of the program counter onto the stack as it performs an automatic CALL to the interrupt routine. Therefore, returning from an interrupt is exactly the same as returning from a called routine ("Interrupt Enable", IE, may have to be reestablished).

Some processors push not only the program counter but also certain status registers and the accumulator onto the stack (some push all index registers, accumulator, and status registers) when an interrupt occurs. When using these processors, returns from interrupts must use a procedure appropriate to their implementation.

3) Page Boundaries

Care must be taken when page boundaries are encountered. As program execution continues to the next page, restart and interrupt vectoring routines that reside at the beginning of each page should be jumped over. When a program is assembled, a two line procedure should be placed at the end of the page to allow programming to continue to the next page.

```
ENDPAGE   LXI        H,next page starting address.
          JMP        PAGETURN
```

4) Discrete Applications

When discrete application software is to reside on each page, a kernel routine must also be placed at the beginning of each page. This kernel takes care of reset, interrupts, I/O routines, and general boot-up instructions pertinent to the application program it supports. A routine should be placed on each page to handle softkey switching between discrete applications. Page switching algorithm 1 is most appropriate for softkey generated page switching.

B) Paged EPROM + Small EPROM

1) Paging and Continuous Programming

This is an efficient configuration for using a paged EPROM in a system since reset routines, interrupt vectoring routines, bootstrap codes, and page switching routine(s) can all reside in the small EPROM. These routines can be called from any page of the paged EPROM. The small EPROM can act as the kernel (main driver) of the system and the paged EPROM contains the application program (holding either a continuous block of program or discrete applications; one on each page).

Since the base address of the paged EPROM is offset from location 0000H by some distance, Algorithm 2 (for the 27513 only) can be used only if the paged EPROM is placed on a 16K byte boundary. If the 27513 is located at 04000H, for example, boot-up code must set the 27513 to page 1. Page 2 becomes the second page, page 3 the third page, and page 0 the fourth page. Straight-line coding can then be used to program the 27513 if programming begins at location 04000H. If the assembler can not handle five digit program counter locations, program segments that exceed 0FFFFH must be ORGed at 0000H. When assembly is complete, code is placed into the 27513 by initializing it to page 1 and transferring assembled code as follows:

Assembled Addresses	Page	To 27513 Relative Address
04000-07FFF	1	0000-3FFF
08000-0BFFF	2	4000-7FFF
0C000-0FFFF	3	8000-BFFF
00000-03FFF	0	C000-FFFF

Since information contained in the two most significant bits is the important factor for Algorithm 2, the 27513 can be placed at any 16 kilobyte boundary using programming and assembly methods similar to that shown above. During program execution, proper displacement of the 27513 in the address space can be accomplished by setting either or both of the two high order bits of the "HL" register.

For all algorithms, calls and jumps are performed just as they were in the Paged EPROM Only method. The only difference is that the page turning routine resides in the small EPROM rather than on each page of the paged EPROM.

2) Resets and Interrupts

Resets and interrupts require the same considerations as a system using standard memory. Interrupt vectoring routines lie in the small EPROM. If the service routines addressed by these vectors reside within the paged EPROM, code within the small EPROM must take care of changing the paged EPROM to the proper page.

3) Page Boundaries

Crossing page boundaries in a continuous programming mode is accomplished by a two instruction routine:

```
          LXI        H,Starting address on next page
          JMP        PAGETURN
```

Since redundant code need not be placed on each page, programming and assembly is less of a burden on the programmer.

4) Discrete Applications

Discrete applications on each page can be selected by allowing the small EPROM to act as the operating system. Code within the small EPROM decides which page is to be selected by monitoring softkeys or responding to software directives.

C) Paged EPROM + RAM

1) Paging and Continuous Programming

Since almost all systems contain some amount of RAM, a portion of this RAM can be set aside to hold routines that would otherwise require duplication on every page. Since the paged EPROM is the only ROM in this implementation, boot-up code must be located on page zero (as it was for the Paged EPROM Only configuration). Interrupt and reset vectoring routines, which are fixed locations in most processor schemes, would have to reside as they did in a Paged EPROM Only system. The main variant for this Paged EPROM + RAM system is that the page switching routine(s) can reside in a small amount of RAM rather than on every page of the EPROM.

The boot-up code on page zero must transfer the page switching routine to RAM where it can be accessed from any routine, anywhere in memory; even from any page of the EPROM. Some advantage in EPROM space (due to the elimination of redundant coding) and programming ease is gained.

2) Interrupt and Reset

There is no advantage over the Paged EPROM Only configuration as far as reset and hard-wired interrupt routines are concerned. However, an advantage is realized in systems that use interrupt controllers to provide vector addresses. Interrupt service routines can be placed into RAM by (and from) the boot-up code or downloaded from disk. The interrupt controller can point to RAM code for service routines when an interrupt is encountered.

Service routines may be too lengthy to be duplicated from page zero to RAM. In this case, code pointed to by an interrupt controller can contain information that directs program execution to the proper page and the relative location on that page.

3) Crossing Page Boundaries

Page boundaries are crossed in this Paged EPROM + RAM system just as they were in the Paged EPROM Only configuration; i.e. by using the ENDPAGE routine. As noted in the Paged EPROM Only system, reset and interrupt routines residing at the beginning of each page must be jumped over as a page boundary is crossed.

4) Discrete Programs

When discrete applications reside on each page, provisions must be made to allow reset and interrupt routines to occupy their normal positions on each page. To eliminate redundant coding, routines on page zero, such as keyboard service routines, interrupt service routines common to the applications software on all pages, and I/O routines, can be written to RAM space by the boot-up code on page zero. This code can reside on page zero before being transferred to RAM, or it can be loaded into RAM from a system disk.

MULTIPLE PAGED EPROMs

Multiple Paged EPROMs can be used in any system. For example, if two of these devices are used in adjacent memory mapped locations, continuous program execution between them is performed exactly as it would between two 27128 EPROMs. When page changes occur, both EPROMs should have their page numbers updated. This is most likely to occur when discrete applications are contained on each page. For large discrete applications, a simple page change performed on all paged EPROMs will replace one application with an entirely new one.

SUMMARY

Address-constrained systems can now realize a dramatic increase in program memory through the use of paged EPROMs. Code overflow can be accommodated in existing systems by a simple plug-in replacement of a higher density EPROM. For new applications, program memory constraints need never be the cause of system obsolescence. Programs can occupy 64 kilobytes today and be upgraded to as much as 4 megabytes in the future using a single 28-pin site (32-pin PLCC site). Discrete applications can occupy the same address space without having to add decoders, latches, or logic circuitry for bank selection. The on-chip page latch located within the free writable address locations of the EPROM saves board and address space. Paged EPROMs provide the highest integration, smallest footprint solution for applications requiring programmable nonvolatile memory.

APPENDIX A
PAGED EPROM + 8031

The 8031 microcontroller provides two 64K memory blocks; one for program memory and one for data storage. Microcontrollers are generally used in program intensive environments which require large amounts of nonvolatile memory. Systems requiring up to 64K of memory can use EPROMs with linear addressing schemes, such as the 27512. For systems that require more than the 64K linear address space, the paged EPROM can add a new dimension to the 8031's program memory. Up to four of these devices can be used to provide 256 kilobytes (27513) or 512 kilobytes (27011) of executable memory without intruding on the data memory's space.

The 8031's hardware and instruction set facilitate easy read access of the program memory area but do not provide a simple means for writing to that area in order to change pages. The $\overline{WR}$ output from port 3 of the 8031 could be routed directly to the $\overline{WE}$ input of a paged EPROM to allow page changes whenever a write instruction addresses a location within a paged EPROM's memory partition. However, if four of these devices are used, filling all of the program memory space, the entire data area will be overlayed by the program memory area for all write instructions. Advantage can be taken of the output ports provided by the 8031 by designating a single bit of port 1, for example, to serve as a selector to allow the $\overline{WR}$ output of the 8031 to be directed to either data memory or program memory. Figure A1 shows how the inclusion of simple logic gates can provide up to 512K of program memory and a full array of data memory.

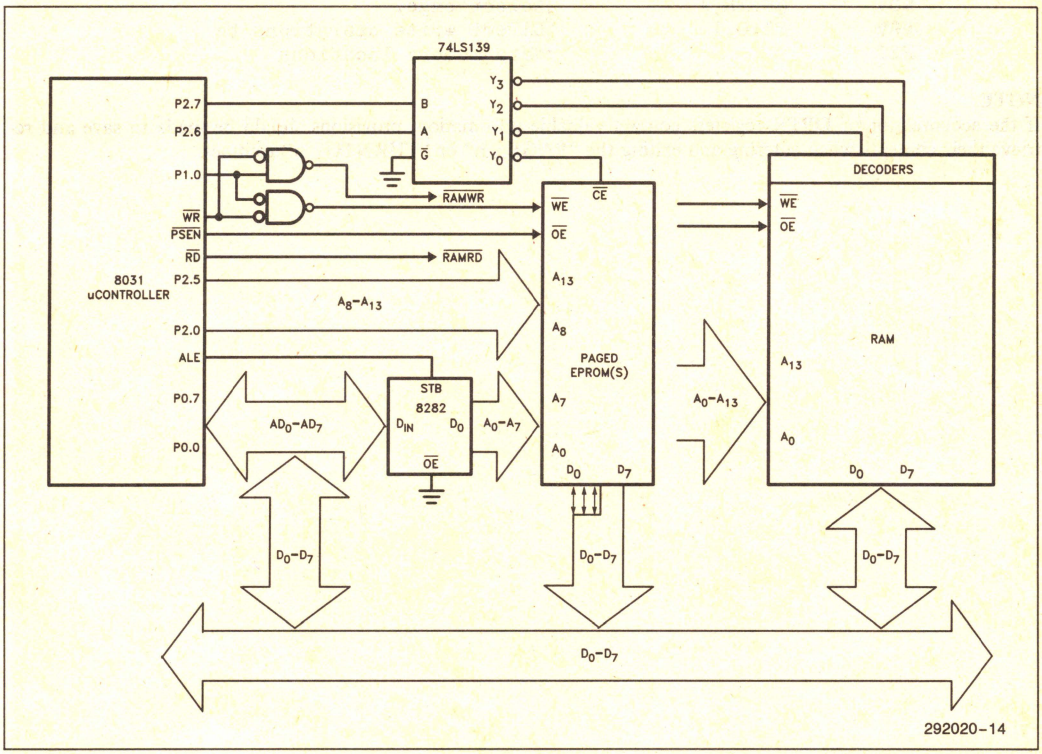


Figure A1. 8031 System Configuration

Changing The Pages

Calling or jumping to a subroutine on another page is accomplished by:

```
SOURCE    STATEMENT
GETSUB    MOV       DPTR,#destination ;"DPTR" gets destination address.
          LCALL     Page_n            ;Call the subroutine to turn
                                      ;to page n = 0, 1, 2, ...
```

Following are routines that actually accomplish the page change. "PAGE_n" routines (where n = the page number) are located at identical relative addresses on each page of the EPROM.

```
PAGE_n    PUSH      Present_page      ;Save present page number.
TURNTO_n  MOV       A,#New_page_number;"A" gets destination page number.
          MOV       Present_page,A    ;Update present page.
          MOV       P1.0,0            ;Direct write operations to
                                      ;program memory locations.
          MOV       @DPTR,A           ;Select new page.
          MOV       P1.0,1            ;Direct write operations to
          CLR       A                 ;data memory locations.
          JMP       @A+DPTR           ;Jump to destination.
RETURN    POP       A                 ;Retrieve return page number.
          MOV       Present_page, A   ;Update present page pointer.
          MOV       P1.0,0            ;Direct write operations to
                                      ;program memory locations.
          MOV       @DPTR,A           ;Select page.
          MOV       P1.0,1            ;Direct write operations to
          RET                         ;data memory locations
```

NOTE:
If the accumulator or DPTR registers contain valuable information, provisions should be made to save and retrieve their contents when entering and exiting the "PAGE_n" or "TURNTO_n" routines.

APPENDIX B
PAGED EPROM + Z80

Z80 microprocessor systems easily accommodate the paged EPROM. Address and data bus connections are straight forward, and software page changing routines are very similar to those used by the 8085. Figure B1 shows the hardware block diagram for a Z80/Paged EPROM system. Although the $\overline{MREQ}$ output of the Z80 need not be used in conjunction with the $\overline{RD}$ and $\overline{WR}$ signals, maximum system flexibility is achieved by using $\overline{MREQ}$ and $\overline{IORQ}$ to select between Program/Data memory and I/O locations.

Z80 instructions at identical locations on each page call routines on other pages.

Algorithm 1: Manual Paging

```
SOURCE    STATEMENT
PAGE_n    PUSH     DE              ;Save old page (n = page number).
TURNTO_n  LD       D,#Newpage      ;"D" gets new page number.
          LD       (HL),D          ;Change the page.
          JP       (HL)            ;Go to destination.
RETURN    POP      DE              ;Retrieve old page.
          POP      HL              ;Get return address.
          LD       (HL),D          ;Change the page.
          JP       (HL)            ;Return to calling routine.
```

Calling a routine on another page and returning afterward are accomplished by:

```
GETSUB    LD       HL,#destination
          CALL     PAGE_n
```

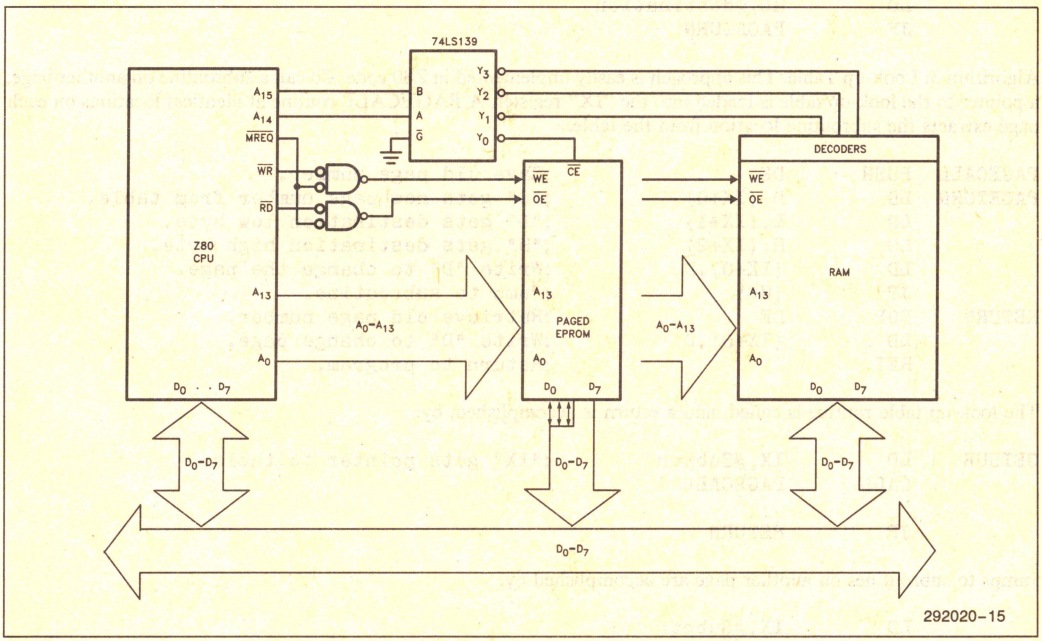


Figure B1. Z80 System Configuration

```
        JP      RETURN
```

The following two statements allow jumps to destinations on other pages.

```
        LD      HL,#destination
        JP      TURNTO_n
```

Algorithm 2: Automatic Paging. Contiguous-code programs can use automatic paging in 27513/Z80 systems. Routines at identical locations on each page access routines on other pages.

```
PAGECALL  PUSH    DE              ;Save old page # (D register).
PAGETURN  LD      D,H             ;"D" gets high address byte.
          RLC     D               ;Rotate to get page # from
          RLC     D               ;two most significant bits.
          RES     6,H             ;Clear bits 6 and 7 of the
          RES     7,H             ;"H" register for relative address.
          LD      (HL),D          ;Change the page.
          JP      (HL)            ;Jump to new location.
RETURN    POP     DE              ;Retrieve old page number.
          POP     HL              ;Get return address.
          LD      (HL),D          ;Change to old page.
          JP      (HL)            ;Return to program.
```

The page changing routine is called and a return is accomplished by:

```
GETSUB    LD      HL,#destination
          CALL    PAGECALL

          JP      RETURN
```

Jumps to destinations are accomplished by:

```
          LD      HL,#destination
          JP      PAGETURN
```

Algorithm 3: Look-up Table. This approach is easily implemented in Z80 code. To call a subroutine on another page, a pointer to the look-up table is loaded into the "IX" register. A PAGECALL routine at identical locations on each page extracts the subroutine location from the table.

```
PAGECALL  PUSH    DE              ;Save old page number.
PAGETURN  LD      D,(IX+0)        ;"D" gets new page number from table.
          LD      L,(IX+1)        ;"L" gets destination low byte.
          LD      H,(IX+2)        ;"H" gets destination high byte.
          LD      (IX+0),D        ;Write "D" to change the page.
          JP      (HL)            ;Jump to subroutine.
RETURN    POP     DE              ;Retrieve old page number.
          LD      (IX+0),D        ;Write "D" to change page.
          RET                     ;Return to program.
```

The look-up table routine is called, and a return is accomplished, by:

```
GETSUB    LD      IX,#Subptr      ;"IX" gets pointer to table.
          CALL    PAGECALL

          JP      RETURN
```

Jumps to subroutines on another page are accomplished by:

```
          LD      IX,#Subptr
          JP      PAGETURN
```

APPENDIX C
PAGED EPROM + 6800/6809

The 6800 series of microprocessors differs from Intel's and Zilog's in the way it boots up at power on. The 6800/6809 looks to the end of its address space for a restart vector. At power-up, the program counter is loaded with the two-byte address contained at physical addresses 0FFFEH and 0FFFFH. If the paged EPROM is to be the only ROM in the system, as shown in Figure C1, its base address should be memory mapped at system address 0C000H. This allows the 6800/6809 to find its boot-up vector at the top two bytes of page zero (system addresses 0FFFEH and 0FFFFH; device addresses 3FFEH and 3FFFH). To allow for system RESET, the top two bytes of all other pages should also contain vectors that direct program execution to a routine that changes the EPROM to page zero and begins program execution at the boot-up routine.

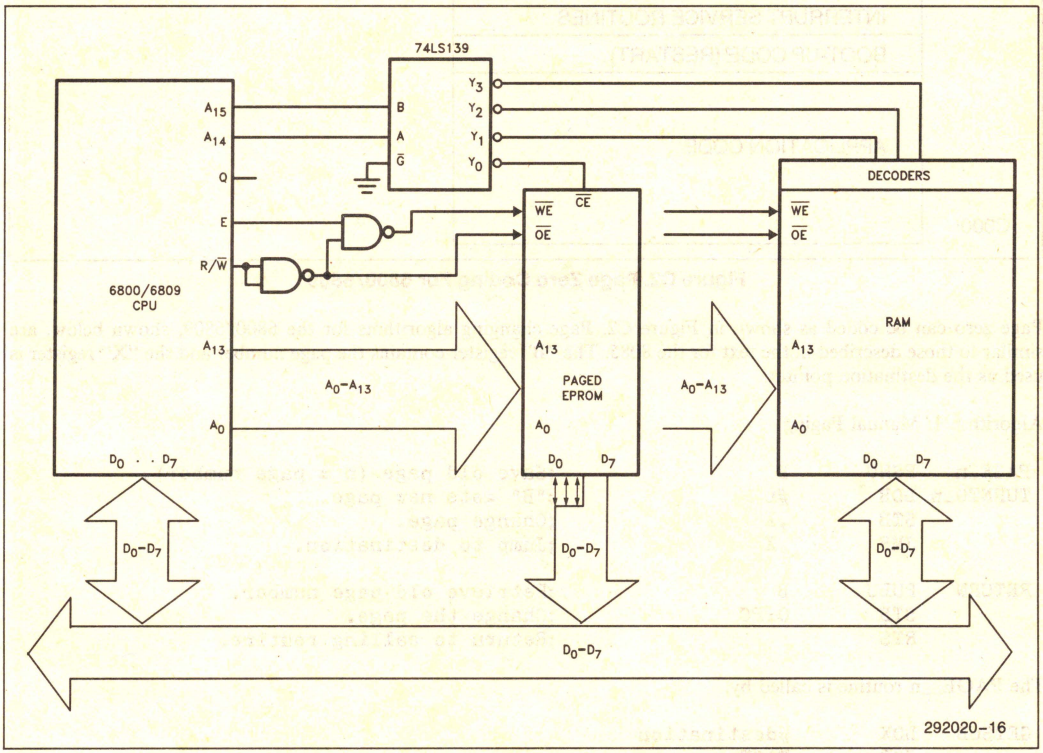


Figure C1. 6800/6809 Configuration

The 6800/6809 also uses addresses 0FFF0H–0FFFDH to hold vectors that direct program execution to service routines when hardware or software interrupts occur. These addresses must be reserved at the top memory locations for all pages. Locations pointed to by these vectors must either contain service routines or direct the microprocessor to routines on appropriate pages.

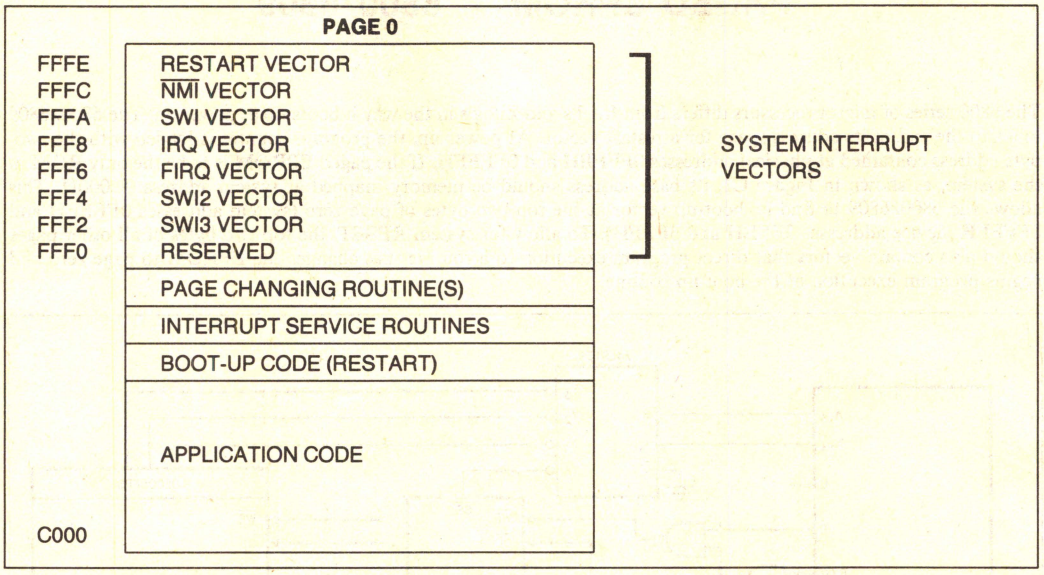


Figure C2. Page Zero Coding For 6800/6809

Page zero can be coded as shown in Figure C2. Page changing algorithms for the 6800/6809, shown below, are similar to those described in the text for the 8085. The "B" register contains the page number and the "X" register is used as the destination pointer.

Algorithm 1: Manual Paging

```
PAGE_n    PSHU    B          ;Save old page (n = page number).
TURNTO_n  LDB     #n         ;"B" gets new page.
          STB     ,X         ;Change page.
          JMP     ,X         ;Jump to destination.

RETURN    PULU    B          ;Retrieve old page number.
          STB     0,PC       ;Change the page.
          RTS                ;Return to calling routine.
```

The PAGE__n routine is called by:

```
GETSUB    LDX     #destination
          JSR     PAGE_n
```

To return to the calling routine:

```
          JMP     RETURN
```

Jumps to destinations are accomplished by:

```
          LDX     #destination
          JMP     TURNTO_n
```

Algorithm 2: Automatic Paging (27513 Only). To determine the page and relative address, the following routine can be used in 27513 applications to strip off the two most significant bits.

```
PAGECALL PSHU     B              ;Save old page number.
PAGETURN PSHU     X              ;Save destination address.
         ROLB                    ;Get the two most significant bits
         ROLB                    ;for new page number
         ROLB                    ;(discard old carry bit).
         LDA      #00111111B     ;"A" gets mask bits.
         ANDA     -1,U           ;AND "A" with destination high byte.
         PSHU     A              ;Save destination high byte.
         PULU     X              ;"X" gets relative destination.
         STB      0,PC           ;Change to new page.
         JMP      ,X             ;Jump to destination.

RETURN   PULU     B              ;Get old page number.
         STB      0,PC           ;Change page.
         RTS                     ;Return to program.
```

The page change routine is called by:

```
GETSUB   LDX      #destination
         JSR      PAGECALL
```

To return to the calling routine:

```
         JMP      RETURN
```

Jumps to destinations on another page are accomplished by:

```
         LDX      #destination
         JMP      PAGETURN
```

Algorithm 3: Look-up Table. The indirect indexing capability of the 6809 is particularly useful in the look-up table approach. If identical copies of the table are located on each page, the following routine can be used.

```
PAGECALL PSHU     B              ;Save old page number.
PAGETURN LDB      ,X+            ;"B" gets new page, increment pointer.
         STB      0,PC           ;Change page.
         JSR      [,X]           ;Call routine pointed to by "X".

RETURN   PULU     B              ;"B" gets old page number.
         STB      0,PC           ;Change page.
         RTS                     ;Return to program.
```

The PAGECALL routine is called by:

```
GETSUB   LDX      #destination
         JSR      PAGECALL
```

Return to the calling routine is simply:

```
         RTS
```

A Jump to a destination is accomplished by:

```
         LDX      #destination
         JMP      PAGETURN
```

APPENDIX D
PAGED EPROM + 8086: A 16-BIT APPLICATION

Sixteen-bit systems can also have limitations placed on the size of program memory space. Discrete firmware based applications such as word processing, data base management, and spreadsheet programs don't need to occupy unique locations in the linear address space. Each of these applications can be placed on a separate page of the paged EPROM(s). A simple software or function key command can switch a new application into the "shared" program memory space. Figure D1 is a block diagram of an 8086 + paged EPROM system.

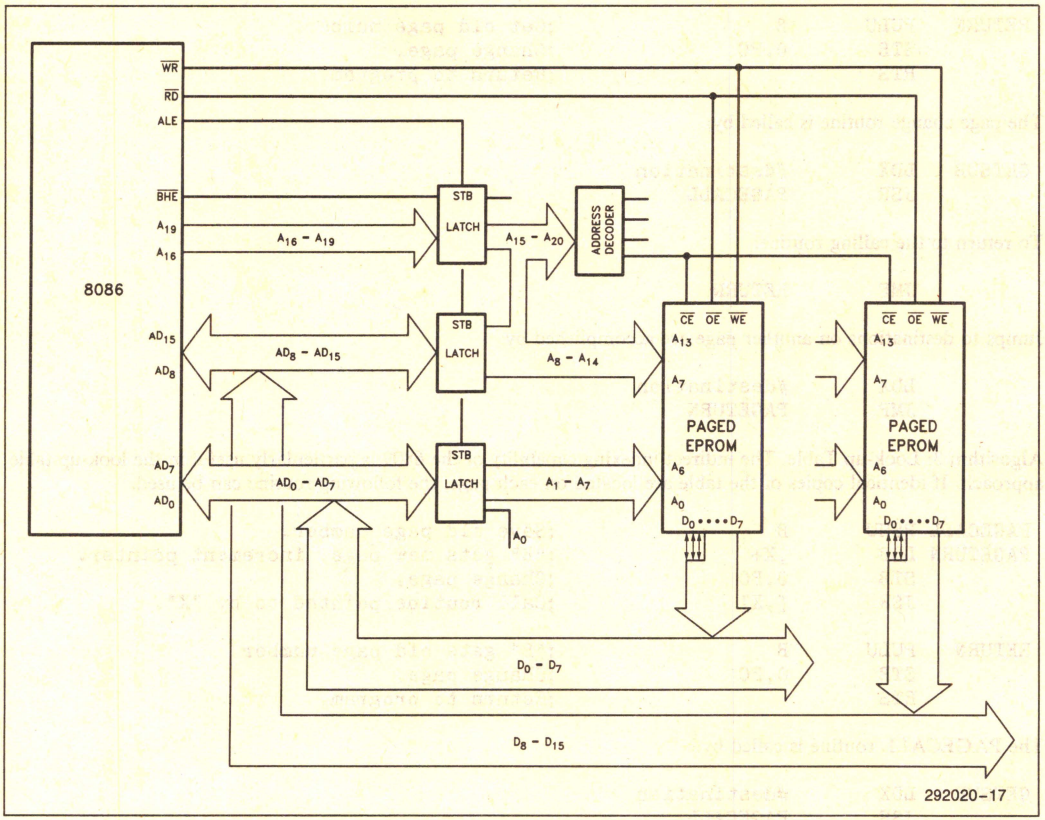


Figure D1. 8086 Configuration

The word-wide (16-bit) data bus requires two paged EPROMs: one for lower data (D0–D7) and one for upper data (D8–D15). During a program memory fetch, the 8086 reads an entire word at a time. Only one byte of each instruction fetch is used, and the other byte is discarded. For this reason it is possible to omit the A0 and $\overline{BHE}$ (low-byte and high-byte) decode signals. Both EPROMs are enabled and their data is read by the microprocessor.

During page changes, a single write instruction to an even address within the EPROMs address range will change the page simultaneously on both paged EPROMs. To do this, a word-write instruction is performed with the upper and lower bytes of the word containing identical page numbers. A programming segment using algorithm 1 will illustrate how a page change is accomplished.

In the following, the "D" register holds the present page number, and "DI" is the destination address.

```
SOURCE    STATEMENT
PAGE_n    PUSH      DX              ;Save old page (n=page number).
          MOV       DL,n            ;"D" gets new page number.
          XCHG      AX,DX           ;Save "A", move "D" to accumulator.
          MOV       AH,AL           ;Page number in high and low bytes.
          MOV       PAGEPROM,AX     ;Change the page on both EPROMs.
          XCHG      AX,DX           ;Restore "A" and save new page #.
          JMP       DI              ;Go to destination.

RETURN    POP       DX              ;Retrieve old page.
          MOV       PAGEPROM,DX     ;Change to old page.
          POP       DI              ;Retrieve return address.
          JMP       DI              ;Return to calling routine.
```

The page change routine is called by:

```
GETSUB    MOV       DI,destination
          CALL      PAGE_n
```

To return to the calling routine:

```
          JMP       RETURN
```

intel

ENGINEERING REPORT

ER-15

April 1985

The 512K EPROM Family
27512: 512K (64K x 8) EPROM
27513: Page Addressed 512K (4 x 16K x 8) EPROM
The A Stepping

Order Number: 290009-001

INTRODUCTION

The 512k EPROM family from Intel consists of the 27512, the standard-addressed version with a 64K × 8 organization, and the 27513, a page-addressed version organized as four 16K × 8 pages. Intel's HMOS*II-E process technology, proven on the 64K through 256K densities, is employed on the 512K EPROMs. The 512K EPROMs have a die size of 185 x 317 mils.

GENERAL DESCRIPTION

Both the 27512 and 27513 are compatible with the industry-standard 28-lead EPROM pinout. The 27512 is the logical density upgrade from the 27256 with pin 1 (V_{PP} on the 27256) freed up for the highest order address, A15, via multiplexing the V_{PP} programming supply with $\overline{OE}$, pin 22.

The 27513 was designed to provide the highest level of memory integration for systems with address range constraints. Popular 8-bit microprocessors and 8- and 16-bit microcontrollers have only 16 address lines. One standard 27512 would consume their entire 64 K-byte address range, leaving no room for other types of memory. The 27513 overcomes these limitations by providing on-chip latches for the two highest order address bits. The former A14 pin (pin 27) becomes a $\overline{WE}$, which when brought low latches the information appearing on the D1 and D0 data lines into internal A14 and A15 registers. Externally, only A0 through A13 are required to address random locations within the selected 16 K-byte page, reducing the physical addressing requirement to 16K (see the 27513 data sheet for a more detailed operational description). The result is that the 27513 is pin for pin compatible in read mode with 128K EPROMs like the 27128A. The $\overline{WE}$ control line, required to change 27513 pages, is on the same pin used for $\overline{WE}$ on byte-wide RAMs. Utilizing the Intel Universal Site concept for byte-wide memories allows simple jumpering of the $\overline{WE}$ function into pin 27 for an easy upgrade to the 27513 from a 128K EPROM. Figure 1 shows the 27513 pinout along with those of the entire Intel EPROM family. Note the compatibility between the 27512 and the 27256 and between the 27513 and the 27128A.

The 27512 and 27513 share the same basic die, benefitting mutually from shared processing. Consequently, they are physically and electrically identical with the exception that the two-bit address latch circuitry is only activated in the process of manufacturing the 27513. The significant differences are in programming and testing where the 27513 is addressed and checked out with page-select operations at the 16 K-byte page boundaries. Figures 2 and 3 illustrate circuit layout relationships (the chip plan) and address decoding scheme (bit map), respectively, for both 512K's.

SIMILARITIES WITH OTHER HMOS II-E EPROMs

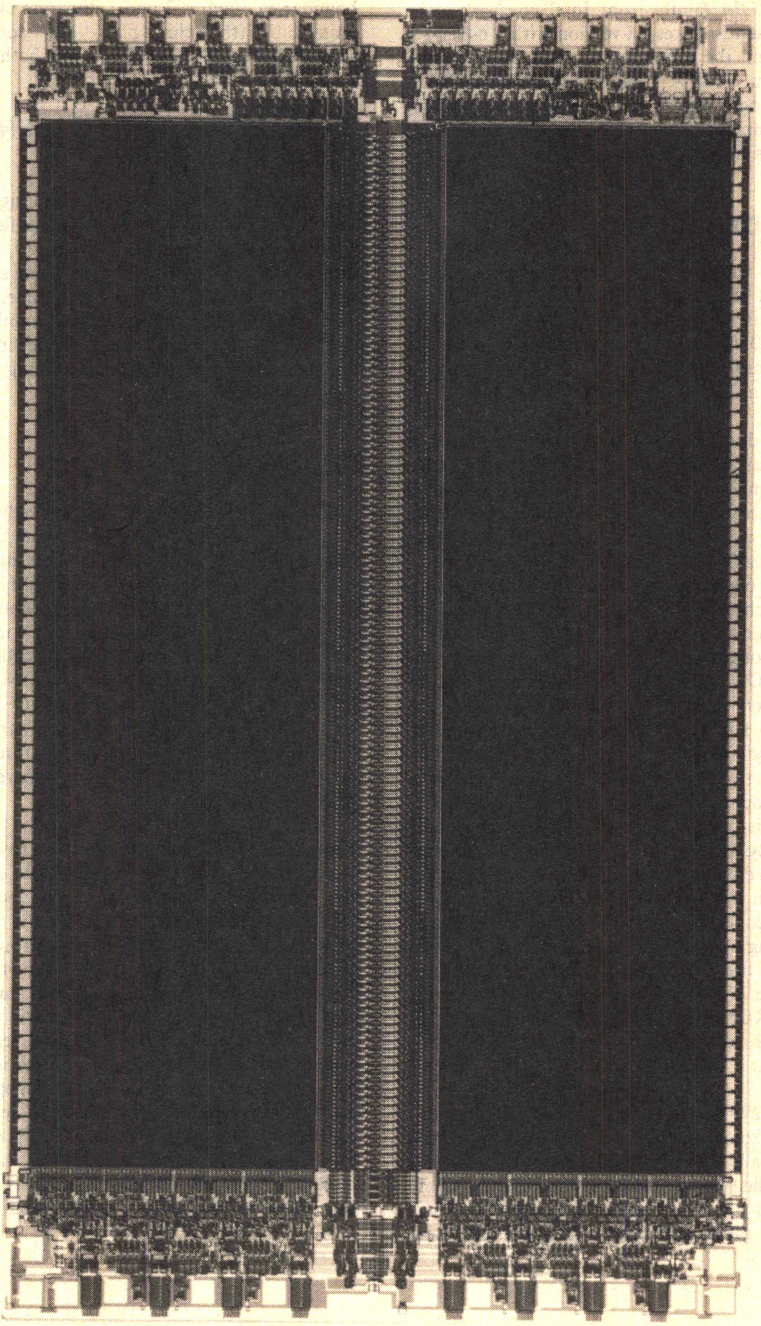
The 512K EPROMs share several design features with the other members of the HMOS II-E family. Common features include input buffer circuitry, sense amplifier design, and a reference column sensing scheme (refer to ER-11, "HMOS II-E: The Next Generation EPROM Technology"). The internal programming circuitry is also similar with the exception of additional 512K logic required to multiplex the programming supply voltage, V_{PP}, with $\overline{OE}$ (pin 22).

REDUNDANCY

The 512K EPROM family employs redundant memory array elements for yield enhancement, using an approach similar to that which was first introduced on the 27128. The 27128 proved the viability of the use of unerasable EPROM (UPROM) cells as the programmable elements for redundancy implementation. UPROM cells are normal EPROM cells which have a metal covering and polysilicon layout such that the resulting structure is inpenetrable to UV light. Not only do UPROM cells have excellent programming yields for maximum success rates in repairing defective arrays, they also exhibit the same high reliability as the EPROM array cells.

The 512K EPROMs have both spare rows and columns (4 redundant rows and 16 redundant columns) available for repair. This scheme is also incorporated into the 27256 C-stepping. While Intel's first redundant EPROM, the 27128, had only spare rows, the addition of redundant columns was later shown to produce a higher repairable yield than earlier statistical models predicted. The experience acquired in manufacturing the 27128 enables a 512K EPROM testing approach which optimizes yields through proper identification of defect type and appropriate repair algorithm. This experience also enables identification of defects which are not "hard", repairable problems. 512K EPROM arrays containing these other defect types which may later spread further into the array, such as those that are contamination-related, are rejected and not repaired.

*HMOS is a patented process of Intel Corporation.



290009-1

Photo 1. 27512/27513 Die Photograph

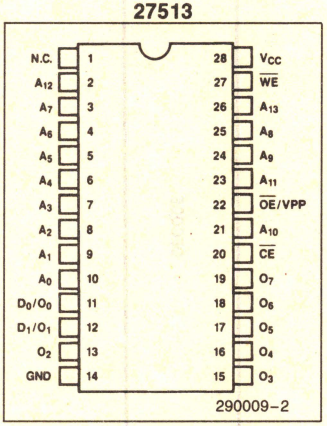
SUMMARY

The HMOS II-E process is one of the densest, most advanced semiconductor technologies in high volume production today, yet it was in use for two years before being employed at the 512K density. This process experience, combined with proven redundancy yield-enhancement techniques, ensures manufacturability of the Intel 512K EPROM family. The mature HMOS II-E process has the added advantage of high reliability. The excellent programming quality and long-term data retention characteristics exhibited by the 2764A, 27128A, and 27256 are also found in the 27512 and 27513 since the EPROM array cells are identical.

Intel's 512K's provide 64 K-bytes of code storage, a capacity which makes it practical to store significant portions of system and application software in EPROM. Firmware is not only inherently more reliable, it provides highest performance and simplest overall system operation from the user's perspective. Facilitating this expanded role for high density EPROMs, Intel's 512K EPROM family is designed for availability and dependability expected of "Software Carriers".

2732A	2764A	27128A	27256	27512
	V_{PP}	V_{PP}	V_{PP}	A_{15}
	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

27513



290009-2

27512	27256	27128A	2764A	2732A
V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A_{14}	A_{14}	$\overline{PGM}$	$\overline{PGM}$	
A_{13}	A_{13}	A_{13}	N.C.	V_{CC}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE:
Intel "Universal Site" compatible EPROM pin configurations are shown in the blocks adjacent to the 27513 pins.

Pin Names

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/V_{PP}
$\overline{WE}$	Page Select Write Enable
O_2–O_7	Outputs
D_0/O_0,D_1/O_1	Input/Outputs
N.C.	No Connect

Figure 1. 27513 and Standard EPROM Pin Configurations

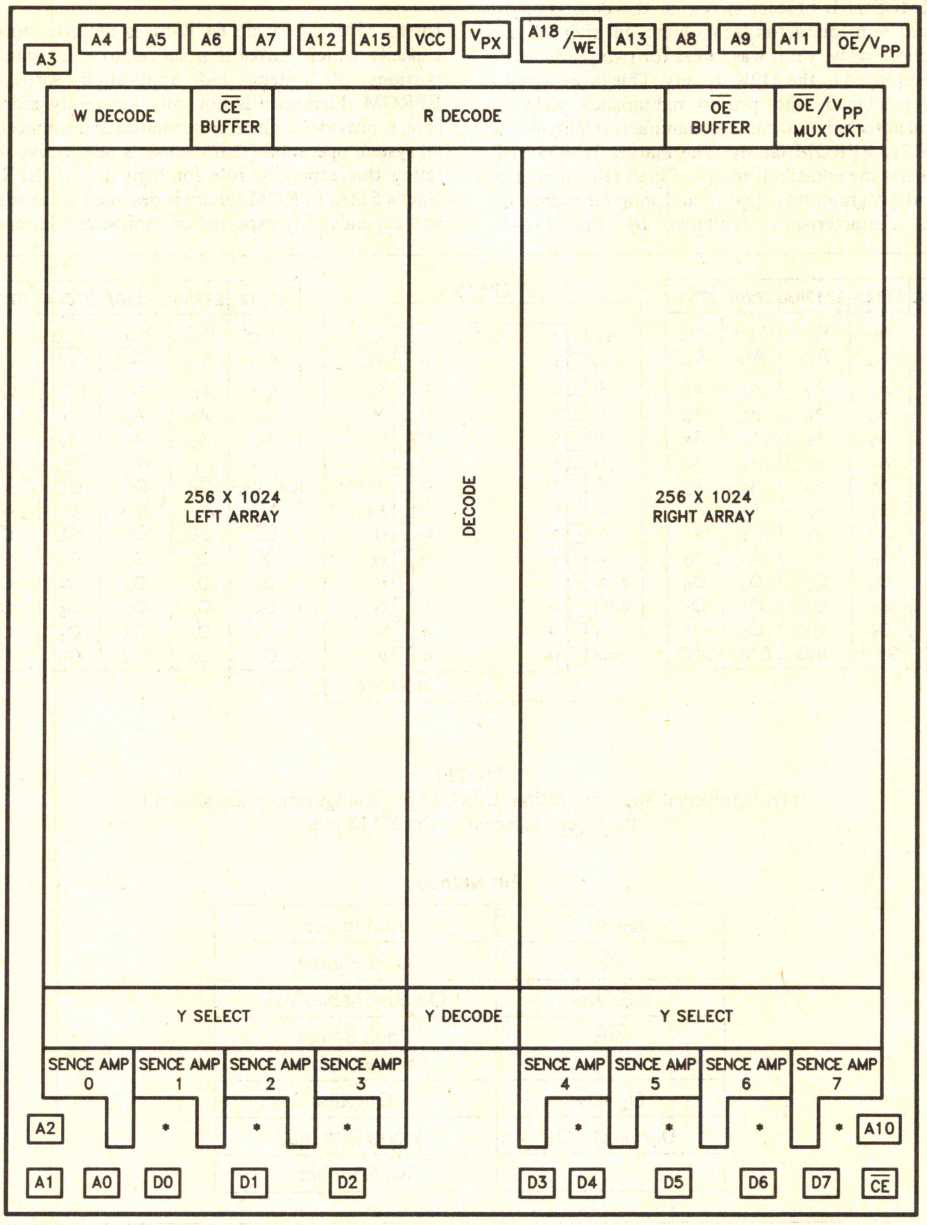


Figure 2. 27512/27513 Chip Plan

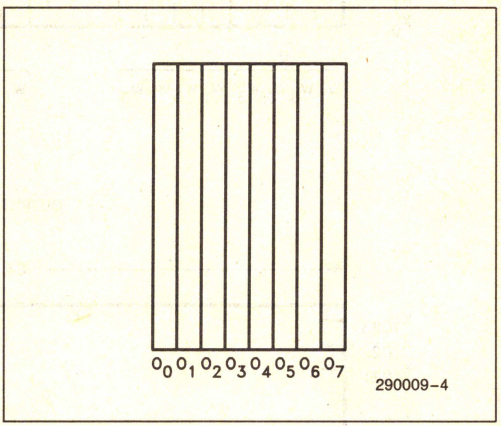
ADDRESS DECODING

	Y DECODE					W DECODE	
	A4	A10	A1	A2		A0	A3
Y_0	0	0	0	0	W_0	0	0
Y_1	0	0	0	1	W_1	0	1
Y_2	0	0	1	0	W_2	1	0
	•			•	W_3	1	1
	•			•			
	•			•			
Y_{15}	1	1	1	1			

	X DECODE							R DECODE		
	A15*	A14*	A13	A12	A8	A7	A6	A11	A9	A5
X_0	0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	0	1	0
•				•			•			•
•				•			•			•
•				•			•			•
X_{1023}	1	1	1	1	1	1	1	1	1	1

*For 27513, A15 & A14 equal $\overline{D_1}$ & $\overline{D_0}$ (inverted) page data

ARRAY ORGANIZATION



BIT MAP

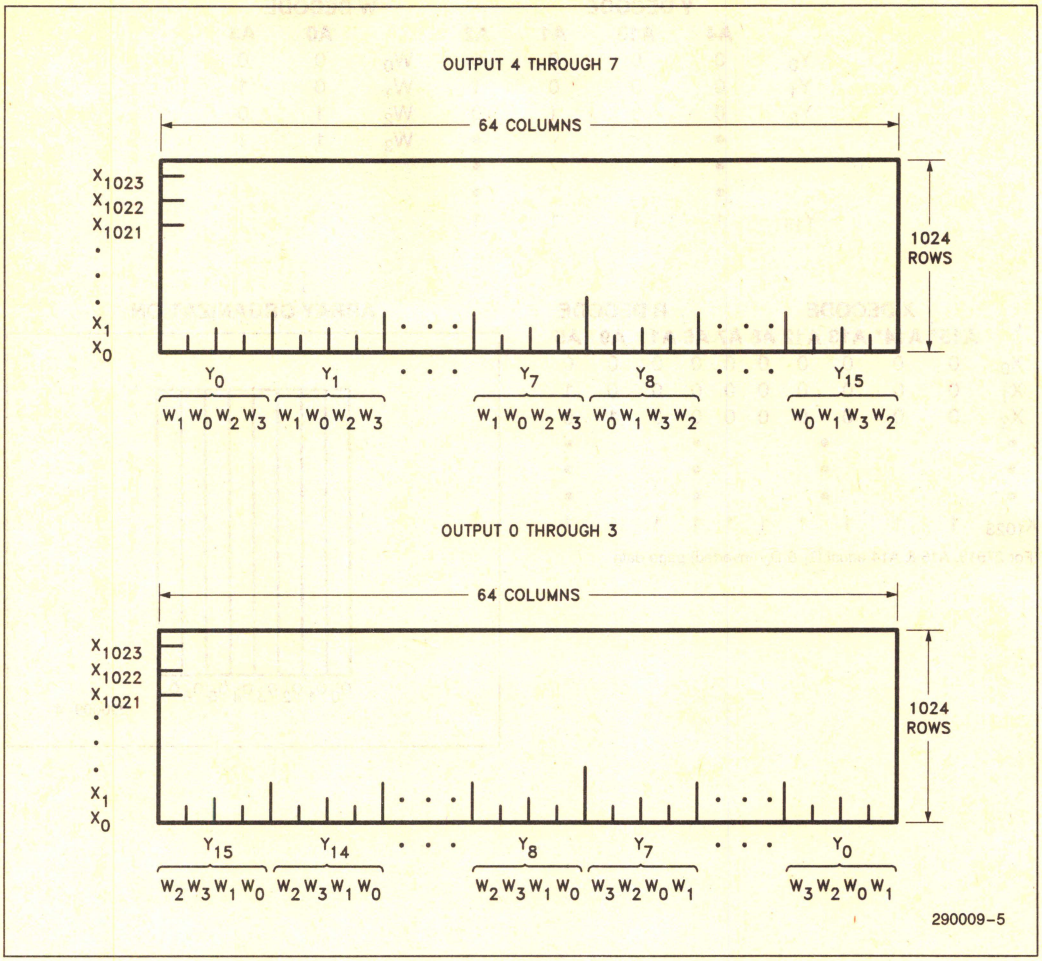


Figure 3. 27512/27513 Bit Map

intel

ENGINEERING REPORT

ER-16

January 1987

Compacted HMOS II-E: The High Density, High Performance EPROM Technology

Order Number: 294000-001

INTRODUCTION

This report describes the process, design, and specification changes in the Compacted HMOS* II-E EPROMs. Intel has developed this process to improve the performance and manufacturability of high density EPROMs as part of its continuing commitment to offer the most advanced EPROMs, manufactured to high quality and reliability standards.

Compacted HMOS II-E is a 15% linear shrink of the existing HMOS II-E process. It incorporates Tungsten-Silicide to lower wordline resistance, enhancing device performance. The products which will be based on this new process are: The Megabit Family, 27010, 27011, and the 27210, two new 512K EPROMs, and the 27128B.

New process features of Compacted HMOS II-E include: a.) reduced cell area, b.) addition of Tungsten-Silicide wordlines, c.) reduction of minimum geometry design rules from 1.5μ to 1.2μ. The major benefits that these improvements bring are:

- Immediate availability, and a rapid transition to cost-effectiveness at the megabit density.
- 128K and 512K densities benefit from substantial performance improvements.

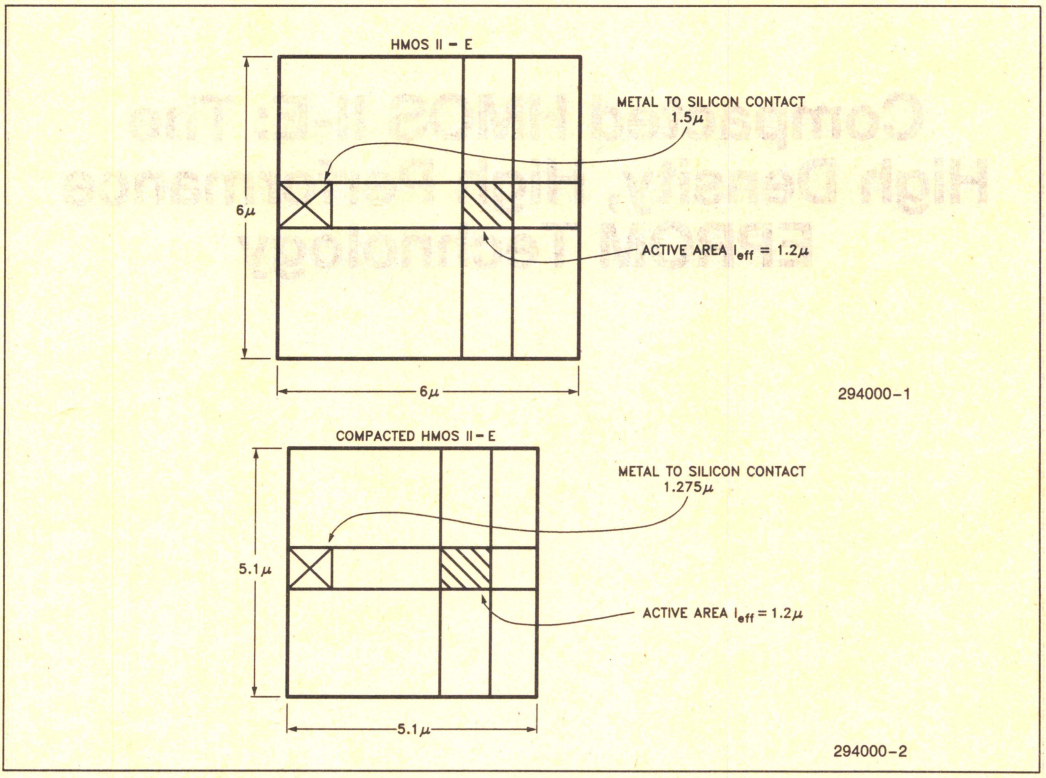
COMPARISON WITH HMOS II-E

Process parameters that are the same as HMOS II-E include: all HMOS II-E EPROM transistor parameters; channel length, depth, and profile, oxide thicknesses, and EPROM programming voltage. The advantages that result from this are:

The same excellent reliability as HMOS II-E.

The same programming algorithms and equipment can be used on Compacted HMOS II-E that were used on HMOS II-E.

Guaranteed availability due to the cumulative learning experience gained on HMOS II-E when applied to Compacted HMOS II-E.



EPROM Cell Size Comparision (Drawn to Scale)

* HMOS is a patented process of Intel Corporation.

COMPACTION

The compaction of the HMOS II-E process involves a 15% linear shrink of all existing HMOS II-E design features. This is made possible through improvements in photo-resist processing and refinements in wafer stepper lithography techniques. The compaction of the design does not effect the active area of the EPROM transistor, only the spacing between transistors.

TUNGSTEN SILICIDE

Manufacturing Considerations

After the second gate poly-silicon deposition is performed, a layer of Tungsten-Silicide is deposited. This results in reduced wordline resistance optimizing the access time of the device. Tungsten-Silicide is deposited using a CVD (Chemical Vapor Deposition) technique which is an extremely well controlled process. This results in film integrity and excellent step coverage. The characteristics of Tungsten-Silicide film are similar to the poly-silicon film creating a reliable, low-resistance wordline. In fact, the same manufacturing equipment which has yielded over 100 million HMOS II-E devices is employed for this new compacted HMOS II-E process module.

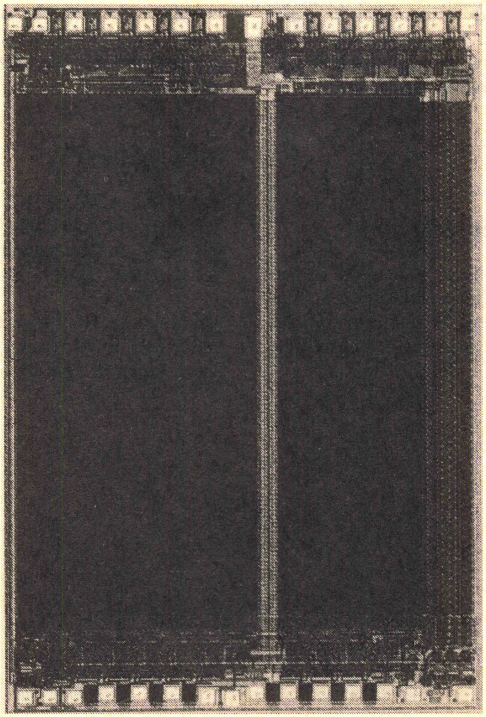
RELIABILITY

Since the HMOS II-E transistor has remained unchanged, the reliability failure rate (FIT's) for devices produced on Compacted HMOS II-E are essentially the same as with HMOS II-E.

Qualification results for Compacted HMOS II-E will be published in the regular updates of the Intel reliability data summary (RR-35).

DIE SIZE COMPARISON

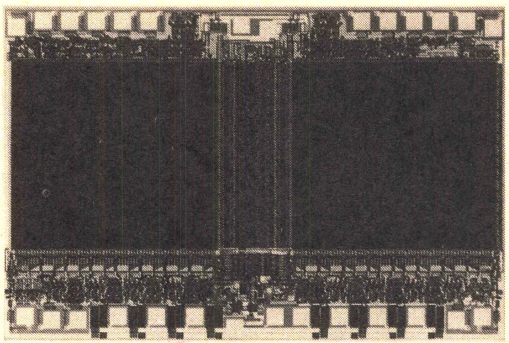
27128
205 MIL-SQ



294000-3

HMOS E

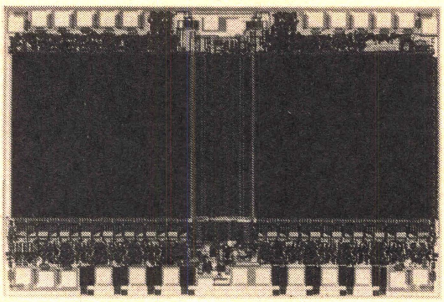
27128A
141 MIL-SQ



294000-4

HMOS IIE

27128B
121 MIL-SQ



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Compacted HMOS IIE

intel

ENGINEERING REPORT

ER-17

November 1986

The One-Megabit EPROM Family 27010: (128K x 8) Bytewide EPROM 27011: (8 x 16K x 8) Page-Addressed EPROM 27210: (64K x 16) Wordwide EPROM

Order Number: 294001-001

INTRODUCTION

The One-Megabit EPROM Family from Intel consists of three products.

1) The 27010 is a standard-addressed version with a 128K x 8 organization. It is housed in a 32 pin DIP package and is upward and downward compatible with other byte-wide EPROM densities. Its die size is 274 x 283 mils.

2) The 27011 is a page-addressed version and is organized as eight 16K x 8 pages. It is fully compatible with the 27513 and is housed in a 28 pin DIP package. Its die size is 274 x 283 mils.

3) The 27210 is a standard-addressed version with a 64K x 16 organization. It is housed in a 40 pin DIP package and is Intel's first word-wide EPROM. Its die size is 282 x 312.

A compacted version of Intel's HMOS II-E process technology, proven on the 64K through 512K densities, is employed on the One-Megabit EPROMs.

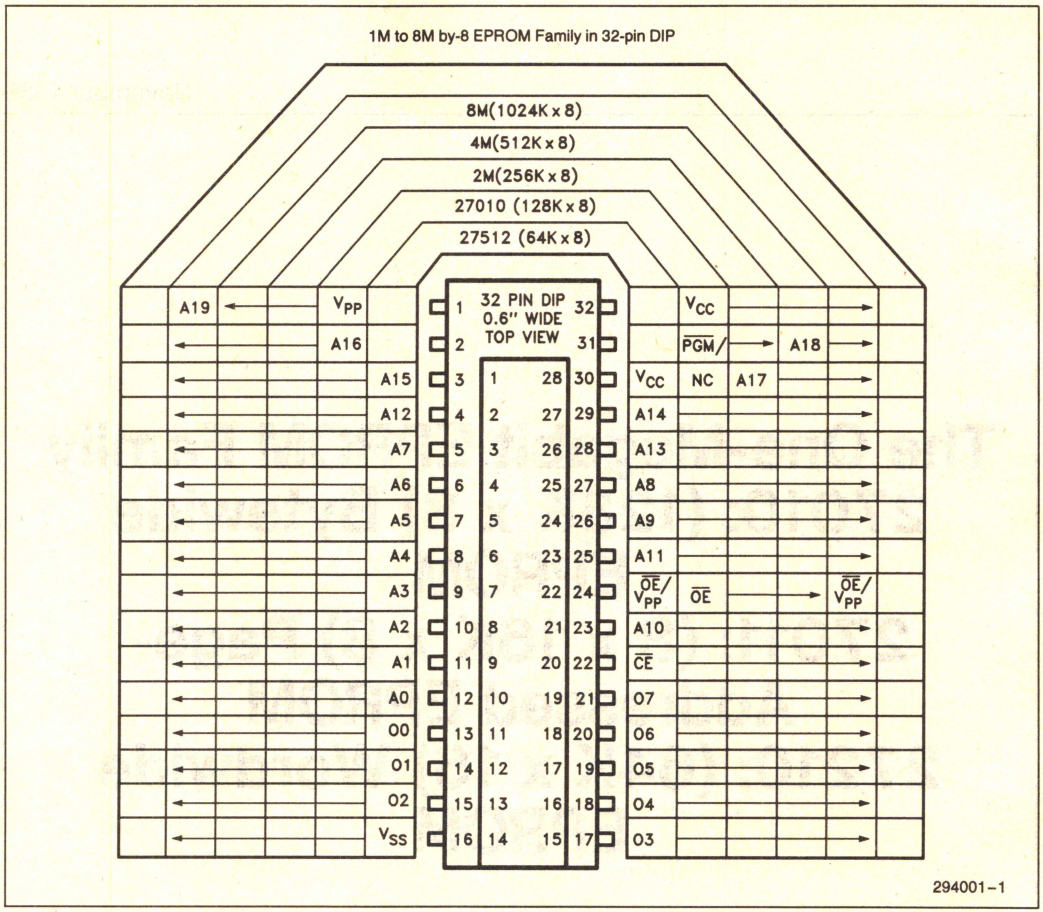


Figure 1. 27010 Pinout

GENERAL DESCRIPTIONS

27010

The standard-addressed 27010 takes the same step from the 28-pin family as the first 28-pin configuration (the 2764) took from the standard 24-pin site in 1980. It is a logical extension of the mainstream EPROM market today. Its upward and backward compatibility with other densities gives customers the flexibility to accommodate code overruns or to upgrade their systems to take advantage of the most cost-effective density. The 27010 is pin-compatible with 27256 and 27512 EPROMs. For larger, standard-addressed memory arrays of 16-bit or 32-bit words, the smaller 32-pin DIP sockets use less board space than the 40-pin DIP alternatives. This concept allows pin-compatible growth through the 8-megabit density. The 200 ns access time version of the 27010 provides no-WAIT-state operation with high performance CPU's such as the 10 MHz 80188.

Figure 1 illustrates the 27010's 32-pin DIP footprint and its compatibility with both lower and future, higher-density devices.

27011

The 27011 was designed to provide the highest level of memory integration for systems with address range constraints. Popular 8-bit microprocessors and 8- and 16-bit microcontrollers have only 16 address lines, less than that of a standard byte-wide 1-Megabit EPROM. The 27011 overcomes these limitations by providing on-chip latches for the three highest order address bits.

The 27011 is an extension of the page-addressing concept introduced at the 512K density with the 27513. It is the only no-hardware-change upgrade path of all memory architectures; the 27011 drops directly into a 27513 socket with only minor software modifications.

Pin 27 provides a page-write enable ($\overline{WE}$), which when brought low latches the information appearing on the D2, D1, and D0 data lines into internal A16, A15, and A14 registers. Externally, only A0 through A13 are required to address random locations within the selected 16 K-byte page, reducing the physical addressing requirement to 16K (see the 27011 data sheet for a more detailed operational description). The result is that the 27011 is pin for pin compatible in read mode with 128K EPROMs like the 27128A. The $\overline{WE}$ control line, required to change pages, is on the same pin used for $\overline{WE}$ on byte-wide RAMs. Utilizing the Intel Universal Site concept for byte-wide memories allows simple jumpering of the $\overline{WE}$ function into pin 27 for an easy upgrade to the 27011 from a 128K EPROM. Figure 3 shows the 27011 pinout along with those of existing and future page-addressed devices. Although this figure stops at 8 M-bit, page-addressed memories allow upgrades to 32 M-bit without hardware modification!

The 27010 and 27011 share the same basic die, benefitting mutually from shared processing. Consequently, they are physically and electrically identical with the exception that the three-bit address latch circuitry is only activated in the process of manufacturing the 27011 prior to packaging. The significant differences are in programming and testing where the 27011 is addressed and checked out with page-select operations at the 16 K-byte page boundaries. Figures 4, 5 and 6 illustrate circuit layout relationships (the chip plan) and address decoding schemes (bit maps) for the 27010 and 27011.

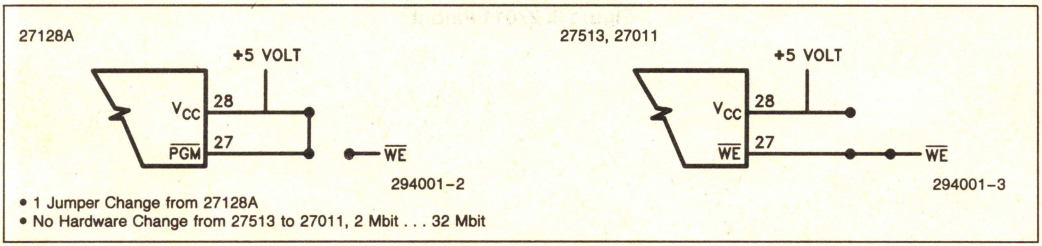
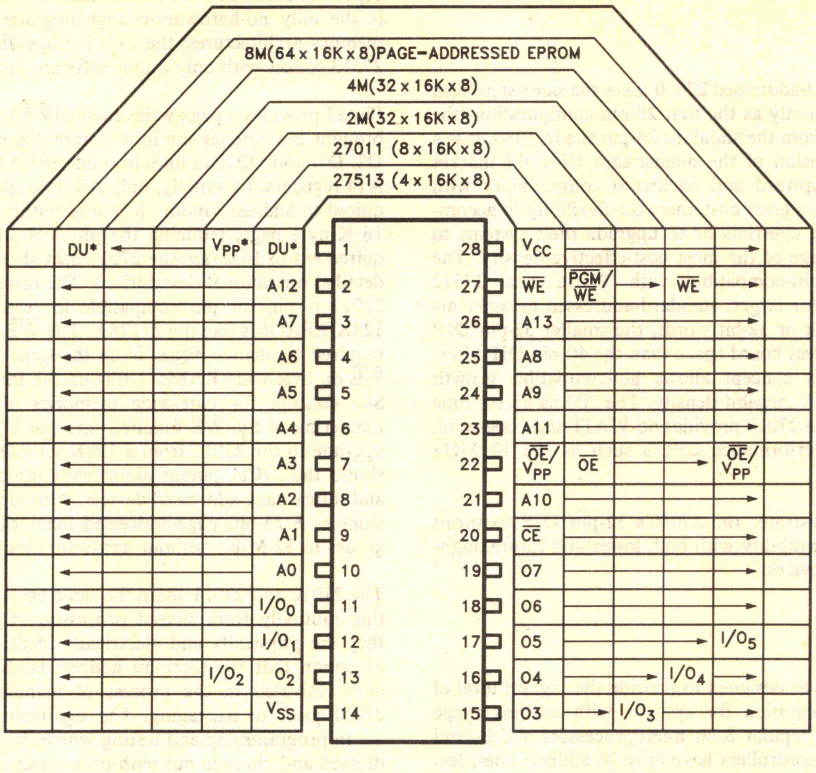
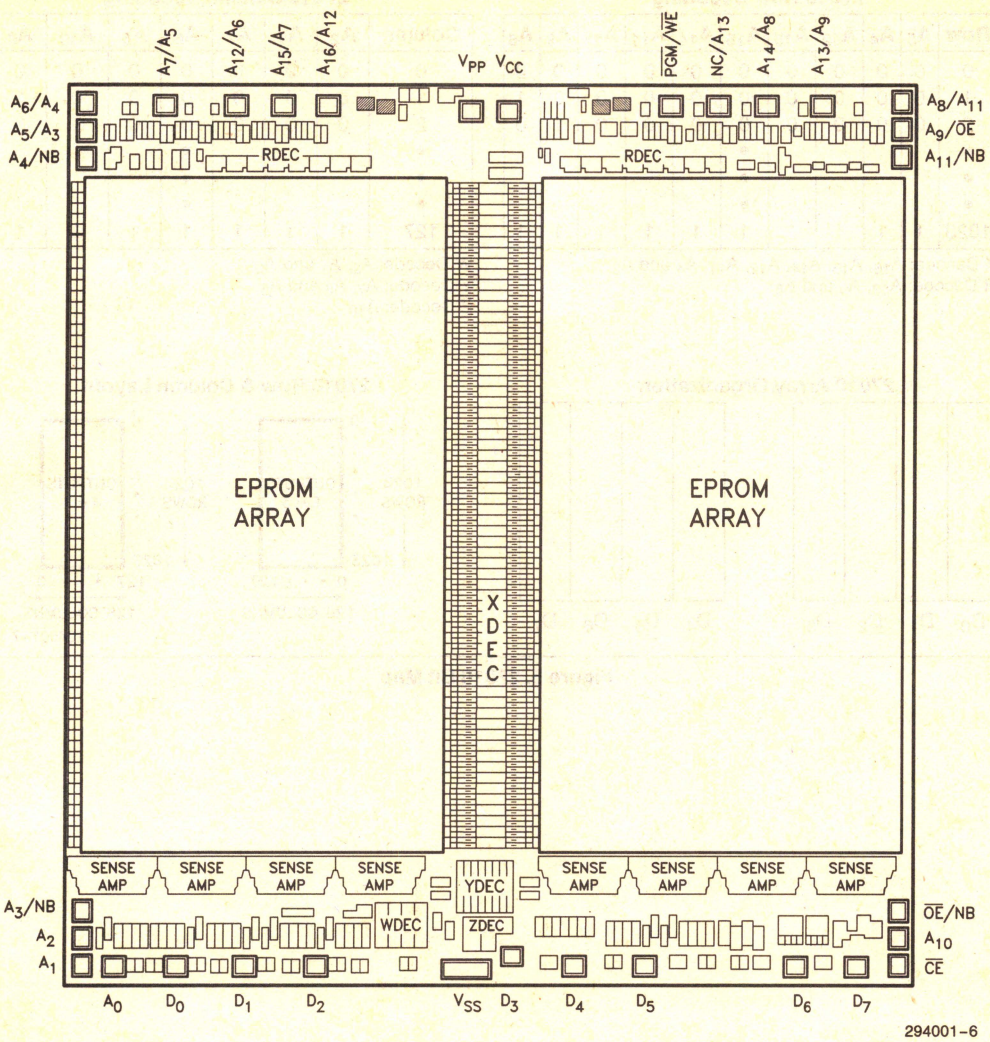


Figure 2. 27011 Upgrade Path



NOTE:
DU = Don't Use
* This pin should be tied to an active low system reset line ($\overline{RST}$). Now available on the 27513, this feature will be added later (1987) on the 27011 to reset device to PAGE 0 when this line is brought to a TTL low (V_{IL}).

Figure 3. 27011 Pinout



NOTE:
Pin functions are labeled 27010/27011, respectively, when used differently. NB on 27011 are "not bonded" pins.

Figure 4. 27010/27011 Chip Plan

27010 Row Decoding

Row	A_3	A_4	A_{12}	A_{15}	A_{16}	A_{14}	A_{11}	A_{13}	A_9	A_8
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

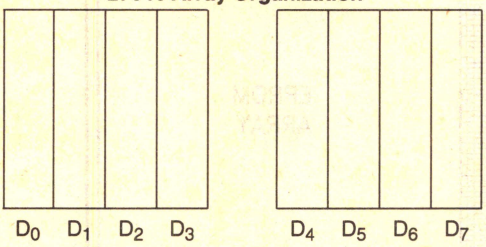
X Decode: A_{16}, A_{15}, A_{14}, A_{12}, A_{11}, A_4 and A_3
R Decode: A_{13}, A_9 and A_8

27010 Column Decoding

Column	A_2	A_1	A_7	A_6	A_5	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_7, A_6 and A_5
Z Decode: A_{10}

27010 Array Organization



27010 Row & Column Layout

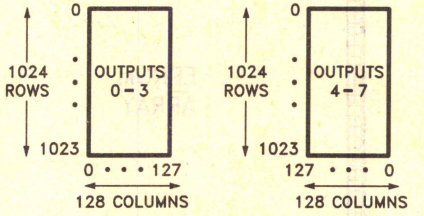


Figure 5. 27010 Bit Map

27011 Row Decoding

Row	$\overline{D_0}$	$\overline{D_1}$	A_6	A_7	A_{12}	A_8	$\overline{D_2}$	A_9	A_{13}	A_{11}
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

X Decode: D_2, D_1, D_0, A_{12}, A_8, A_7 and A_6
R Decode: A_{13}, A_{11} and A_9

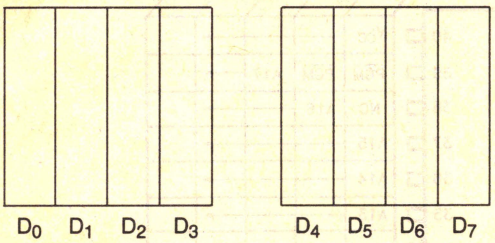
NOTE:
$\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ are complemented page-select write input data.
e.g., $\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ = 000 corresponds to page data 07H.

27011 Column Decoding

Column	A_2	A_1	A_5	A_4	A_3	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_5, A_4 and A_3
Z Decode: A_{10}

27011 Array Organization



27011 Row and Column Layout

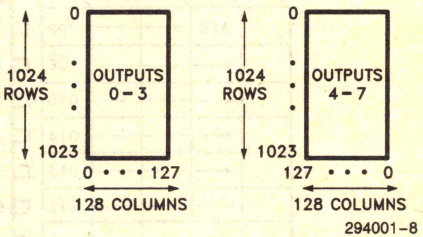


Figure 6. 27011 Bit Map

27210

The 27210 is Intel's first word-wide EPROM offering. Intel has broken with the past to offer a simplified pin-out, shown in Figure 7, which is well-suited for both 16-bit and 32-bit microprocessor-based systems. All addresses are on one side of the device and data on the other, making this architecture a simple solution that meets the needs of today's advanced microprocessors. This approach preserves performance while simplifying board layout design.

The 27210 also is the fastest 1-Megabit EPROM with speeds up to 150 ns available. This enables no-WAIT-state operation in such high performance CPU's as the 10 MHz 80286.

Figures 8 and 9 illustrate the circuit layout relationships (the chip plan) and the address decoding scheme (the bit map), respectively for the 27210.

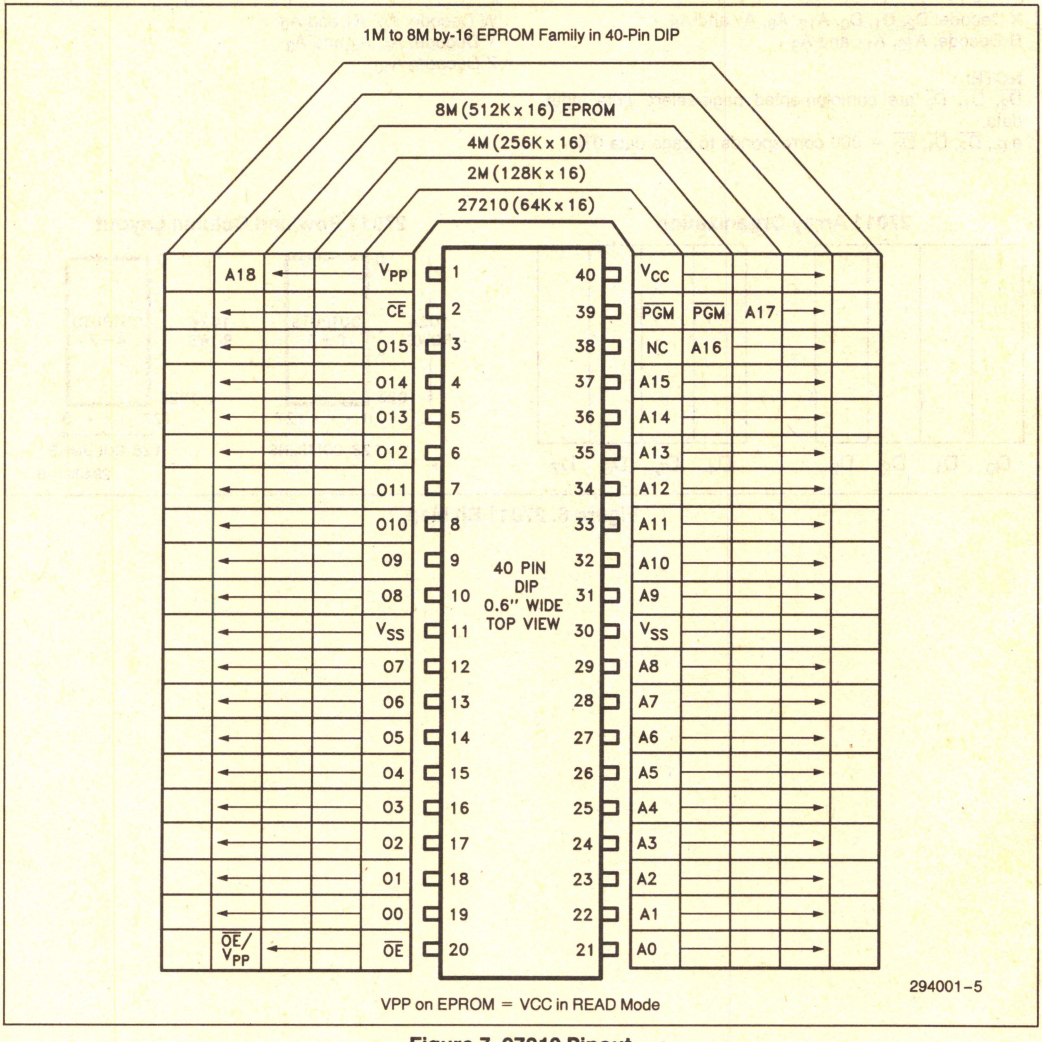


Figure 7. 27210 Pinout

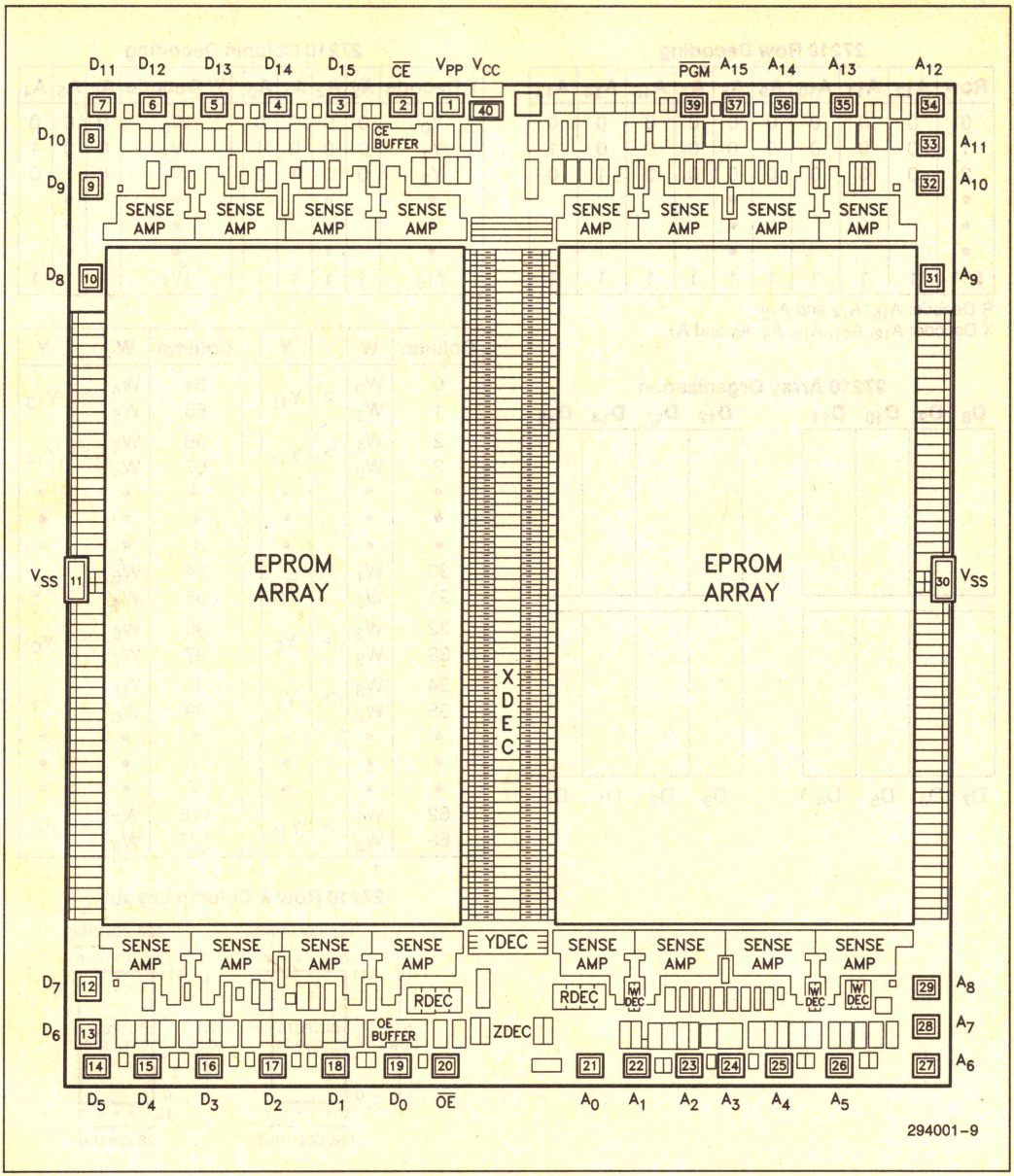


Figure 8. 27210 Chip Plan

27210 Row Decoding

Row	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_{15}	A_{14}	A_{13}
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	1	0
•					•				
•					•				
•					•				
511	1	1	1	1	1	1	1	1	1

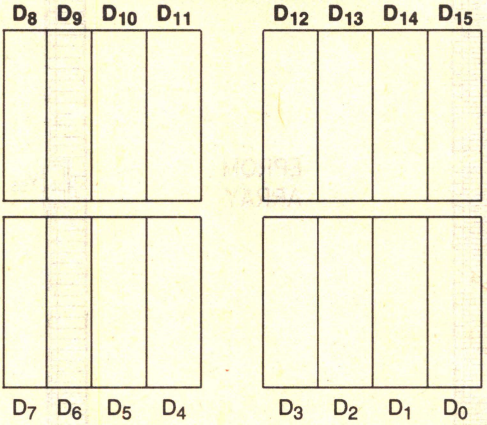
R Decode: A_{15}, A_{14} and A_{13}
X Decode: A_{12}, A_{11}, A_{10}, A_9, A_8 and A_7

27210 Column Decoding

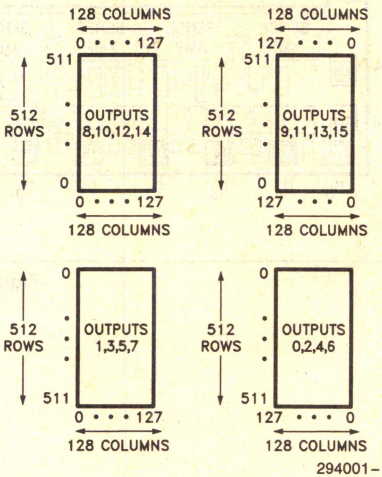
Y Decode	A_3	A_2	A_1	A_0	W Decode	A_6	A_5	A_4
Y_0	0	0	0	0	W_0	0	0	0
Y_1	0	0	0	1	W_1	0	0	1
Y_2	0	0	1	0	W_2	0	1	0
•		•			•		•	
•		•			•		•	
•		•			•		•	
Y_{15}	1	1	1	1	W_7	1	1	1

Column	W		Y	Column	W		Y
0	W_0	>	Y_{15}	64	W_4	>	Y_{15}
1	W_1			65	W_5		
2	W_1	>	Y_{14}	66	W_5	>	Y_{14}
3	W_0			67	W_4		
•	•		•	•	•		•
•	•		•	•	•		•
•	•		•	•	•		•
30	W_1	>	Y_0	94	W_5	>	Y_0
31	W_0			95	W_4		
32	W_2	>	Y_0	96	W_6	>	Y_0
33	W_3			97	W_7		
34	W_3	>	Y_1	98	W_7	>	Y_1
35	W_2			99	W_6		
•	•		•	•	•		•
•	•		•	•	•		•
•	•		•	•	•		•
62	W_3	>	Y_{15}	126	W_7	>	Y_{15}
63	W_2			127	W_6		

27210 Array Organization



27210 Row & Column Layout



294001-10

Figure 9. 27210 Bit Map

Similarities with Other Intel EPROMs

The One-Megabit Family of EPROMs share several design features with other members of the HMOS II-E family of EPROMs like the 27256 and the 27512. Common features include input buffer circuitry, sense amplifier design and a reference column sensing scheme.

The Compacted HMOS II-E process has reduced the cell dimensions of the 1-Megabit EPROMs to 26 square microns from the 36 square microns used on HMOS II-E. The active region of the EPROM cell for compacted HMOS II-E is the same as for HMOS II-E. However, the inactive cell area has been reduced, resulting in the final cell dimension of 26 square microns. Compacted HMOS II-E also uses advanced photolithography to reduce minimum feature sizes from 1.5 microns to 1.2 microns. The use of existing equipment assures that the manufacturability and reliability of the proven HMOS II-E process will extend to 1-Megabit EPROMs.

New Design Features

Both the 27010 and 27210 have a new feature which allows pre-wiring of higher-order addresses. V_{PP} and $\overline{PGM}$ pins are inactive, that is, in a "don't care" state, as long as V_{PP} is kept at or below the V_{CC} supply voltage. This allows direct wiring of A_{17}/A_{18} and A_{18}/A_{19} (for 27210 and 27010, respectively) to accommodate subsequent 4 M-bit and 8 M-bit devices, eliminating the need for board jumper wires. A_{16}/A_{17} addresses can obviously be routed into the N.C. pins for the 2 M-bit upgrade.

Page-addressed memories, like the 27011, have identical pinouts for upgrades all the way to 32 M-bits without hardware changes.

Redundancy

The One-Megabit EPROM Family employs redundant memory elements for yield enhancement, using an approach similar to that used on the 27256 and the 27512. The viability of the use of unerasable EPROM (UPROM) cells as the programmable elements for redundancy implementation has been proven on the 27256 and the 27512. UPROM cells are normal EPROM cells which have a metal covering and polysilicon layout such that the resulting structure is impenetrable by U.V. light. Not only do UPROM cells have excellent programming yields for maximum success rates in repairing defective arrays, they also exhibit the same high reliability as the EPROM array cells.

The 27010 and 27011 both have 4 redundant rows and 4 redundant columns per output. The 27210 has 4 redundant rows each for the upper and lower bytes and 2 redundant columns per output. The experience acquired in manufacturing the 27256 and the 27512 enables a 1-Megabit EPROM testing approach which optimizes yields through proper identification of defect type and appropriate repair algorithm. This experience also enables identification of defects which are not "hard", repairable problems. 1-Megabit EPROMs containing these other defect types which may later spread further into the array, such as those that are contamination-related, are rejected and not repaired.

Summary

The One-Megabit EPROM Family from Intel consisting of the 27010, 27011 and 27210 offers the broadest range of solutions at the highest EPROM density. First, the standard byte-wide (x8) configuration will preserve the JEDEC-approved 28-pin footprint as a subset of a new 32-pin package, allowing growth through eight megabits. Second, the byte-wide (x8) page-addressed version is an extension of the 28-pin site that allows "page" upgrades up to a 32 megabit density. Using this version, either existing systems or new systems with physical address constraints can be upgraded without hardware changes. Finally, the word-wide (x16) architecture, in a 40-pin package, provides an ideal solution for systems based on today's 16-bit and 32-bit microprocessors.

A compacted version of Intel's HMOS II-E process technology, proven on the 64K through 512K densities, is employed on the 1-Megabit EPROMs. By decreasing the EPROM cell size, manufacturable 1-Megabit EPROMs are feasible and cost-effective. The technological and manufacturing experience we've gained with our HMOS II-E technology on earlier EPROM densities is being applied directly to our One-Megabit Family today.

December 1986

EPROM RELIABILITY DATA SUMMARY

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Order Number: 210473-004

THE IMPORTANCE OF RELIABILITY

Reliability of the non-volatile memories in your end product is critical to your total system reliability. The use of Intel EPROMs can make a difference. Reliability is not just tested, but designed into each component Intel manufactures.

QUALITY ≠ RELIABILITY

A quality component is one that meets your specification when received and tested. A reliable component continues to meet your specification even years after you have shipped your product. While Intel is a quality leader, we also adhere to stringent reliability standards which we have established for ourselves.

Consider Quality vs. Reliability

The true cost of any component involves more than just the purchase price. The true component cost encompasses the initial purchase price, cost of rework during system production, and the cost of field repairs due to component failures. "Rework" costs during system production are incurred prior to shipment of your end product, and are a function of the quality of the component you purchase.

Repair costs incurred in the field after end product shipments, are a function of the reliability of the components. In addition to the increasing real cost of a system field service call, there is the intangible cost of a poor reliability reputation to the end use of your product. These costs depend upon the reliability of the components you purchase. Thus, reliability may impact costs during the system lifetime more than the initial quality of the components!

MONITOR PROGRAM

Reliability is designed into each component Intel manufactures. From the moment the design is put to paper, stringent reliability standards must be met at each step for a product to bear the Intel name.

Designing-in reliability, however, is only the beginning. Ongoing tests must be conducted to ensure that the original reliability specifications remain as valid in volume production as they were when the device was first qualified.

Intel's Reliability Monitor Program, devised to measure and control device reliability in production, is a proven tool that Intel has used for seven years and is now available to its customers. The Monitor Program subjects all of Intel's technologies to a 48 hour dynamic burn-in at 125°C (with a portion of these devices continued for a 1000 hour lifetest) and provides answers about device reliability that are not generally available from limited testing programs. But it's much more than burn-in and device testing. When test rejects are encountered, failure analysis is performed on each failed part. Isolating the fault and determining the failure mechanism is a critical part of the Monitor Program. It is the most comprehensive reliability program anywhere.

The paramount objective is to deliver reliable, quality devices. Actions that Intel takes to meet this objective may include a process or design change, or added reliability screen. Each decision is made with our customers in mind so that they receive the parts—and the performance—that they ordered by specifying Intel. Reliability qualification assures that all new production meets Intel's reliability standards. The Reliability Monitor Program ensures that these high standards are continually maintained, day in, day out, over the duration of a device's life. This reliability improves the lifetime reputation of your product, reducing the required number of field service calls.

EPROM RELIABILITY DATA SUMMARY

Intel routinely publishes this "EPROM Reliability Data Summary", a continuing update of reliability information covering Intel's entire EPROM product line. This document includes a discussion on EPROM reliability testing methodology and the most current failure rate calculations, failure analyses and lifetest results.

Intel's commitment to the reliability of our products is clearly reflected in the information we make available to customers. We believe that supplying detailed reliability information to our customers is part of the total solution Intel offers, and is an important part of Intel's leadership in microelectronics technology.

EPROM RELIABILITY TESTING

Intel EPROMs undergo comprehensive testing to insure electrical reliability. This testing is done at qualification and/or during ongoing monitor checks. Where testing differs for plastic packaged production EPROMs, it is so noted.

Intel continually reviews its testing procedures and makes improvements to its methodology whenever overall reliability can be enhanced. Our goal is to be the industry leader in delivering reliable parts and no compromises are accepted.

Information on Intel's reliability testing procedures follows.

High Temperature Dynamic Lifetest—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test the memory is sequentially addressed and the outputs are exercised, but not monitored or loaded. A checkerboard data pattern is used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with the failure analysis. In order to best determine long-term failure rate, all devices used for lifetesting are subjected to standard INTEL screening. The 48 hour burn-in results measure infant mortality and are not included in the failure rate calculation. (See Figure 1 for typical burn-in bias and timing diagrams.)

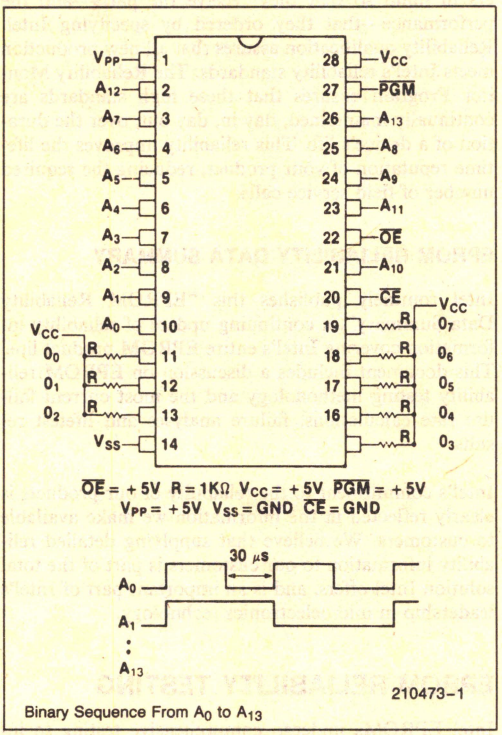


Figure 1. 2764A Burn-In Bias and Timing Diagrams

Failure rate calculations are given for each relevant activation energy. Failure rate calculations are made using the appropriate energy(1,2,3,4) and the Arrhenius Plot as shown in Figure 2*. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. The failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution to arrive at a confidence level associated failure rate. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV. Devices submitted to other stresses received a 168 hour lifetest prior to stressing.

*The activation energies for various failure mechanisms are listed in Table 1.

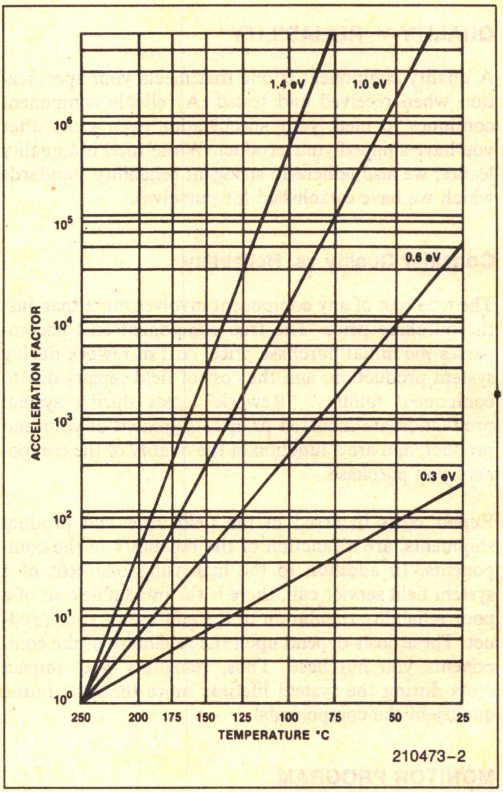


Figure 2. Arrhenius Plot

Table 1. Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mode	Each
Decode/Oxide/Basic Function	0.3
SBCL/SBCG/MBCL/MBCG	0.6
Contamination	1.0
Speed Degradation	0.3–1.0
Output	1.0
Intrinsic Charge Loss	1.4

Failure Definitions

Decode/Oxide/Basic Function—An Oxide Failure Related Fault
SBCL—Single Bit Charge Loss
SBCG—Single Bit Charge Gain
MBCL—Multiple Bit Charge Loss
MBCG—Multiple Bit Charge Gain
Contamination—Ionic Contamination Failure
Speed Degradation—Device Speed Degraded Over Test
Output—Output Buffer Nonfunctional

A typical lifetest bias and timing diagram is shown in Figure 3.

High Temperature 6.5V Dynamic Lifetest—This test is used to accelerate oxide breakdown failures. The test setup is identical to the one used for the dynamic life test except V_{CC} and V_{PP} are at 6.5V. The acceleration factor due to this test can be found in Figure 4. This data plus the standard dynamic lifetest data are used to calculate the 0.3 eV failure rate.

High Temperature Storage—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 99% programmed pattern to a 250°C bake (140° for plastic) with no applied bias. In addition to data retention, this test is used to detect mechanical reliability problems (e.g., bond integrity) and process instability. This test is sometimes referred to as *Data Retention Bake Test.*

Temperature Cycle—This test consists of cycling the temperature of the chamber housing the subject devices from −65°C to +150°C and back. Two hundred cycles are performed with a complete cycle taking 20 minutes. This test is to detect mechanical reliability problems and microcracks.

ESD Testing—This test is performed to validate the products tolerance to Electro Static Discharge damage. All products incorporate ESD protection networks on appropriate pins.

Two types of tests are performed. First, all devices are tested using Mil STD 883 test criteria. In addition, a charged device test is performed to further validate protection occurring during mechanical handling.

Programmability—Device programmability is routinely monitored through the process of programming the devices for product monitors and qualifications. Programmability is a distinct part of a product qual. All voltage combinations are qualified. Program margin is measured and tested on 100% of Intel EPROM products.

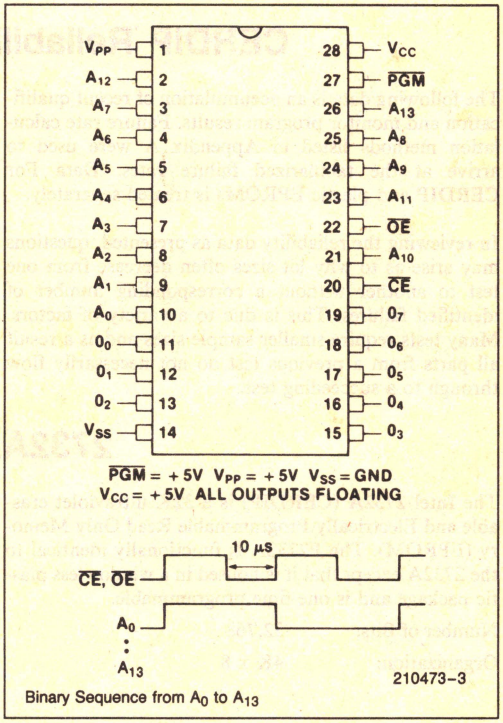


Figure 3. 2764A Lifetest Bias and Timing Diagram

Type	Supply Voltage (Volts)	Oxide Thickness (A)	Operating Stress (MV/CM)	Acceleration Factor at__% Over Stress			
				10%	20%	50%	100%
NMOS/PMOS	12	1100	1.1	5.9	35	7000	5×10^7
HMOS* E	5	700	0.714	3.2	10	320	99,500
HMOS* II E	5	325	1.25	7.5	55	23,700	5.6×10^8
CHMOS* II E	5	325	1.25	7.5	55	23,700	5.6×10^8

ASSUMES:
1. No Bias Generators
2. Depletion Loads

Figure 4. Time-dependent Oxide Failure Accelerations

*HMOS and CHMOS are patented processes of Intel Corporation.

REFERENCES

1. S. Rosenberg, D. Crook, B. Euzent, "16th Annual Proceedings of the International Reliability Physics Symposium," pp 19–25, 1978.
2. J. Caywood, B. Euzent, B. Shiner, "Data Retention in EPROMs," 1980 IEEE International Reliability Physics Symposium.
3. S. Rosenberg, B. Euzent, "HMOS Reliability" Reliability Report RR-18, INTEL Corporation, 1979.
4. N. Mielke, "New EPROM Data-Loss Mechanisms," 1983. International Reliability Physics Symposium.
5. R.M. Alexander, "Calculating Failure Rates From Stress Data," April 1984 International Reliability Physics Symposium.

NOTE:
The methodology for calculating failure rates is detailed in Appendix A.

CERDIP Reliability Data Summary

The following data is an accumulation of recent qualification and monitor program results. Failure rate calculation methods listed in Appendix A were used to arrive at the tabularized failure rates. Data For CERDIP and plastic EPROMs is treated separately.

In reviewing the reliability data as presented, questions may arise as to why lot sizes often decrease from one test to another without a corresponding number of identified failures. This is due to a variety of factors. Many tests require smaller sample sizes and as a result all parts from a previous test do not necessarily flow through to a succeeding test.

In addition, various parts are pulled from a sample lot when mechanical or handler failures occur. These "failures" are not a result of the specific test just completed but are nonetheless removed from the sample lot size and are not included in any failure rate calculation. It can also happen that a particular test is done incorrectly through human error or faulty test equipment and "invalid" failures are put aside for retesting at a later date, decreasing the lot size for a succeeding test. If these parts are found to be truly defective, they are treated as failures and listed. If they test out properly, they are removed from any calculation data base.

2732A/P2732A

The Intel 2732A (CERDIP) is a 32K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The P2732A is functionally identical to the 2732A except that it is housed in a windowless plastic package and is one-time programmable.

Number of Bits: 32,768

Organization: 4K x 8

Pin Out: 24 pin, JEDEC Approved Industry Standard

Die Size: 163 x 97 mil.

Process: HMOS-E

Cell Size: 11.5 x 8.75 μM

Programming Voltage: 21.0V

Technology NMOS

2732A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	16/23853	5/21395	1/2125	4/2162	—	—	—
1986	17/12941	15/12928	1/1495	0/1378	0/225	0/225	0/225
Total	23/36794	20/34323	2/3620	4/3540	0/225	0/225	0/225
	A	B	C	D			

2732A (Continued)

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1985	12/3030	4/3016	5/1605	—
1986	4/1804	4/1668	—	0/150
Total	16/4834	8/4684	5/1605	0/150
	E	F	G	

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
7.09E + 06	0.3 B.I.	3.68E + 07	2.45E + 07	3		
1.13E + 05	0.3*VAF	5.84E + 06	3.89E + 06	0		
			Total 0.3 eV Failures =	3	0.0098	0.0147
7.09E + 06	0.6 B.I.	1.91E + 08	8.49E + 07	10		
1.33E + 06	0.6 Bake	3.61E + 09	1.43E + 09	28		
1.13E + 05	0.6 HVELT	3.03E + 06	1.35E + 06	0		
			Total 0.6 eV Failures =	38	0.0011	0.0027
7.09E + 06	1.0 B.I.	1.72E + 09	4.44E + 08	14		
1.13E + 05	1.0 HVELT	2.73E + 07	7.04E + 06	0		
			Total 1.0 eV Failures =	14	0.0009	0.0035
			Combined Failure Rate:		0.0118	0.0209
			FITs:		117.63	208.73

48 Hour BI Infant Mortality 0.062%

Theta Ja = 55°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 80 mA

Delta T = 23.1 C
T(55) = 351.2 K
T(70) = 366.2 K
T(125) = 421.2 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT Accel. Factors:	0.3	5.191645	3.459451
	0.6	26.95318	11.96780
	1.0	242.2981	62.61679
250° Bake Accel. Factors:	0.3	N/A	N/A
	0.6	2722.141	1076.682
	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 10.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 4 MBCG
3 Speed Degrade
6 SBCL
1 Leakage
3 Basic Function
2 Oxide
4 Contamination

B. 2 Oxide
2 SBCL
1 Speed Degrade
14 Contamination
1 MBCG

C. 2 SBCL

D. 4 SBCL

E. 12 SBCL
3 MBCL
1 MBCL

F. 7 SBCL
1 MBCL

G. 5 SBCL

2764A/P2764A

The Intel 2764A (CERDIP) is a 64K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The P2764A is functionally identical to the 2764A except that it is housed in a windowless plastic package and is one-time programmable.

Number of Bits: 65,536

Organization: 8K x 8

Pin Out: 28 pin, JEDEC Approved Industry Standard

Die Size: 98 x 117 mils

Process: HMOS II-E

Cell Size: 6 x 6 μM

Programming Voltage: 12.5V

Technology: NMOS

2764A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs
1985	10/24277	1/24255	5/2450	1/2444
1986	6/17874	3/16758	2/1610	1/1607
Total	16/42151	4/41013	7/4060	2/4051
	A	B	C	D

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1985	4/2718	3/2712	0/1424	—
1986	3/1806	0/1930	—	0/250
Total	7/4524	3/4642	0/1424	0/250
	E	F		

2764A (Continued)

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
8.29E + 06	0.3 B.I.	4.85E + 07	3.13E + 07	4		
0.00E + 00	0.3*VAF	0.00E + 00	0.00E + 00	0		
			Total 0.3 eV Failures =	4	0.0108	0.0167
8.29E + 06	0.6 B.I.	2.83E + 08	1.18E + 08	9		
1.25E + 06	0.6 Bake	3.39E + 09	1.34E + 09	9		
0.00E + 00	0.6 HVELT	0.00E + 00	0.00E + 00	0		
			Total 0.6 eV Failures =	18	0.0005	0.0014
8.29E + 06	1.0 B.I.	2.98E + 09	6.94E + 08	0		
0.00E + 00	1.0 HVELT	0.00E + 00	0.00E + 00	0		
			Total 1.0 eV Failures =	0	0.0000	0.0001
			Combined Failure Rate:		0.0114	0.0182
			FITs:		113.57	181.91

48 Hour BI Infant Mortality 0.038%

Theta Ja = 48°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 40 mA

Delta T = 10.08 C
T(55) = 338.2 K
T(70) = 353.2 K
T(125) = 408.2 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT Accel. Factors:	0.3	5.841606	3.773111
	0.6	34.12436	14.23636
	1.0	359.0109	83.62421
250° Bake Accel. Factors:	0.3	N/A	N/A
	0.6	2722.141	1076.682
	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 3 Decode Failure
8 Speed Degrade
1 Output
4 SBCG

B. 2 SBCG
1 SBCL
1 MBCG

C. 3 SBCG
3 Speed Degrade
1 SBCL

D. 1 SBCL
1 Speed Degrade

E. 6 SBCL/SBCG
1 Speed Degrade

F. 3 SBCL

27C64/87C64

The Intel 27C64 and 87C64 are low power 64k ultraviolet erasable and Electrically Programmable Read Only Memories (EPROMs). For reliability purposes, both models are treated as one as their memory design and manufacturing processes are identical. The 87C64 incorporates an internal address latch, the 27C64 does not.

Number of Bits: 65,536

Organization: 8K x 8

Pin Out: 28 pin, JEDEC Approved Industry Standard

Die Size: 141 x 148 mils

Process: CHMOS II-E

Cell Size: 6 x 6 μM

Programming Voltage: 12.5V

Technology: CMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	3/7651	3/7624	0/805	0/801	—	—	—
1986	0/4245	1/4234	0/460	0/460	0/200	0/199	0/187
Total	3/11896	4/11858	0/1265	0/1261	0/200	0/199	0/187
	A	B					

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1985	11/866	4/835	—	0/175
1986	1/785	3/783	15/513	1/135
Total	12/1651	7/1618	15/513	1/310
	C	D	E	F

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.47E + 06	0.3 B.I.	1.56E + 07	9.86E + 06	2		
9.56E + 04	0.3*VAF	3.31E + 07	2.10E + 07	0		
			Total 0.3 eV Failures =	2	0.0064	0.0101
2.47E + 06	0.6 B.I.	9.82E + 07	3.93E + 07	0		
2.95E + 05	0.6 Bake	8.03E + 08	3.18E + 08	33		
9.56E + 04	0.6 HVELT	3.79E + 06	1.52E + 06	0		
			Total 0.6 eV Failures =	33	0.0039	0.0098
2.47E + 06	1.0 B.I.	1.14E + 09	2.49E + 08	0		
9.56E + 04	1.0 HVELT	4.41E + 07	9.61E + 06	0		
			Total 1.0 eV Failures =	0	0.0001	0.0004
			Combined Failure Rate:		0.0103	0.0203
			FITs:		103.48	202.57

48 Hour BI Infant Mortality 0.025%

27C64/87C64 (Continued)

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	46°C/Watt	Delta T = 2.415 C				
V_{CC} =	5.25 Volts	T(55) = 330.5 K	Bl/ELT	0.3	6.299620	3.988151
I_{CC} =	10 mA	T(70) = 345.5 K	Accel.	0.6	39.68522	15.90535
		T(125) = 400.5 K	Factors:	1.0	461.7228	100.5940
		T(250) = 523.1 K				
			250° Bake	0.3	N/A	N/A
		K = 8.62E-05 eV/K	Accel.	0.6	2722.141	1076.682
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1 Oxide Breakdown
1 SBCL
1 MBCG
B. 2 Oxide Breakdown (13)
2 Speed Degrade (13)
C. 10 SBCL
1 MBCL
1 I_{CC} (STBY) Failure
D. 7 SBCL
E. 15 SBCL
F. SBCG (non-package related)

27128A/P27128A

The Intel 27128A (CERDIP) is a 128K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The P27128A is functionally identical to the 27128A except that it is housed in a windowless plastic package and is one time programmable. These parts differ from the 27128 in that they require 12.5 Vpp vs. 21.0 Vpp and the process technology is HMOS II-E vs. HMOS-E.

Number of Bits: 131,072

Organization: 16K x 8

Pin Out: 28 pin, JEDEC Approved Industry Standard

Die Size: 169 x 117 mils

Process: HMOS II-E

Cell Size: 6 x 6 μM

Programming Voltage: 12.5V

Technology: NMOS

27128A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	1/5502	0/336	0/275	0/270	—	—	—
1986	1/4914	0/1031	0/216	0/72	0/100	0/100	0/100
Total	2/10416	0/1367	0/491	0/342	0/100	0/100	0/100
	A						

27128A (Continued)

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake				200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	
1985	0/389	0/389	0/388	—	—
1986	0/395	1/299	0/293	0/71	0/50
Total	0/784	1/688	0/681	0/71	0/50
		B			

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
4.98E + 05	0.3 B.I.	2.80E + 06	1.83E + 06	0		
5.00E + 04	0.3*VAF	1.55E + 07	1.01E + 07	0		
			Total 0.3 eV Failures =	0	0.0050	0.0077
4.98E + 05	0.6 B.I.	1.57E + 07	6.70E + 06	0		
3.46E + 05	0.6 Bake	9.43E + 08	3.73E + 08	0		
5.00E + 04	0.6 HVELT	1.58E + 06	6.73E + 05	0		
			Total 0.6 eV Failures =	0	0.0001	0.0002
4.98E + 05	1.0 B.I.	1.57E + 08	3.79E + 07	1		
5.00E + 04	1.0 HVELT	1.58E + 07	3.81E + 06	0		
			Total 1.0 eV Failures =	1	0.0012	0.0048
			Combined Failure Rate:		0.0063	0.0128
			FITs:		62.74	127.64

48 Hour BI Infant Mortality 0.019%

Theta Ja = 45°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 60 mA

Delta T = 14.17 C
T(55) = 342.3 K
T(70) = 357.3 K
T(125) = 412.3 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	5.621355	3.667994
Accel.	0.6	31.59964	13.45418
Factors:	1.0	315.8422	76.10777
250° Bake	0.3	N/A	N/A
Accel.	0.6	2722.141	1076.682
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:
A. 1 FAB Defect (0.5)
1 MBCL
B. 1 MBCL

27128B
(Preliminary)

The Intel 27128B is a 128K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). This part differs from the 27128A in that it is fabricated on a 15% linear shrink of the existing HMOS II-E process. The compaction of the design does not affect the active area of the EPROM transistor, only the spacing between transistors.

Number of Bits:	131,072
Organization:	16K x 8
Pin Out:	28 pin, JEDEC Approved (Industry Standard)
Die Size:	145 x 101 mils
Process:	HMOS II-E (Compacted)
Cell Size:	5 x 5 μM
Programming Voltage:	12.5V
Technology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest	
		168 Hrs	500 Hrs	1000 Hrs	500 Hrs	1000 Hrs
1986	1/2637	0/2619	0/342	0/342	0/130	0/130
	A					

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake		
	168 Hrs	500 Hrs	1000 Hrs
1986	0/150	0/150	0/150

Failure Rate Predictions: Due to the small number of actual device hours on this product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 1 SBCG

27128B (Continued)
(Preliminary)

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.92E + 05	0.3 B.I.	1.55E + 06	1.03E + 0	0		
2.37E + 04	0.3*VAF	6.92E + 06	4.58E + 0	0		
			Total 0.3 eV Failures =	0	0.0108	0.0163
2.92E + 05	0.6 B.I.	8.26E + 06	3.62E + 06	0		
4.89E + 04	0.6 Bake	1.33E + 08	5.26E + 07	1		
2.37E + 04	0.6 HVELT	6.70E + 05	2.94E + 05	0		
			Total 0.6 eV Failures =	1	0.0014	0.0036
2.92E + 05	1.0 B.I.	7.66E + 07	1.94E + 07	0		
2.37E + 04	1.0 HVELT	6.22E + 06	1.57E + 06	0		
			Total 1.0 eV Failures =	0	0.0000	0.0000
			Combined Failure Rate:		0.0122	0.0199
			FITs:		122.18	198.77

Theta Ja = 43°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 90 mA

Delta T = 20.31 C
T(55) = 348.4 K
T(70) = 363.4 K
T(125) = 418.4 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT Accel. Factors:	0.3	5.318766	3.521640
	0.6	28.28927	12.40195
	1.0	262.6453	66.44823
250° Bake Accel. Factors:	0.3	N/A	N/A
	0.6	2722.141	1076.682
	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1 Output Failure
B. 1 Intermittent CE Buffer Failure
C. 1 SBCL

27256

Intel 27256 (CERDIP) is a 256K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). A plastic production version, the P27256, will be available in mid 1985.

Number of Bits: 262,144

Organization: 32K x 8

Pin Out: 28 pin, JEDEC Approved Industry Standard

Die Size: 180 x 193 mils

Process: HMOS II-E

Cell Size: 6 x 6 μM

Programming Voltage: 12.5V

Technology: NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	9/24204	7/23465	4/3497	1/3384	0/100	0/100	—
1986	9/15839	10/15810	0/1650	2/1380	0/239	0/233	1/106
Total	18/40043	17/39275	4/5147	3/4764	0/339	0/333	1/106
	A	B	C	D			E

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake				200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	
1985	16/3125	13/3103	10/1179	—	0/550
1986	32/1805	10/1773	0/129	0/129	1/300
Total	48/4930	23/4876	10/1308	0/129	1/850
	F	G	H		I

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
8.80E + 06	0.3 B.I.	4.66E + 07	3.09E + 07	2		
9.14E + 04	0.3*VAF	2.66E + 07	1.77E + 07	1		
			Total 0.3 eV Failures =	3	0.0057	0.0086
8.80E + 06	0.6 B.I.	2.47E + 08	1.09E + 08	14		
1.26E + 06	0.6 Bake	3.42E + 09	1.35E + 09	81		
9.14E + 04	0.6 HVELT	2.56E + 06	1.13E + 06	0		
			Total 0.6 eV Failures =	95	0.0027	0.0067
8.80E + 06	1.0 B.I.	2.28E + 09	5.79E + 08	8		
9.14E + 04	1.0 HVELT	2.37E + 07	6.01E + 06	0		
			Total 1.0 eV Failures =	8	0.0004	0.0016
			Combined Failure Rate:		0.0088	0.0169
			FITs:		87.85	169.27

48 Hour BI Infant Mortality 0.045%

27256 (Continued)

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	44°C/Watt	Delta T = 20.79 C				
V_{CC} =	5.25 Volts	T(55) = 348.9 K	BI/ELT	0.3	5.296763	3.510907
I_{CC} =	90 mA	T(70) = 363.9 K	Accel.	0.6	28.05570	12.32646
		T(125) = 418.9 K	Factors:	1.0	259.0411	65.77555
		T(250) = 523.1 K				
			250° Bake	0.3	N/A	N/A
		K = 8.62E-05 eV/K	Accel.	0.6	2722.141	1076.682
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 7 Decode
3 Contamination
3 SBCL
1 SBCG
1 Basic Function
3 Speed Degrade

B. 8 SBCL
2 SBCG
1 Speed Degrade
6 Contamination

C. 1SBCG
1 MBCG
1 SBCL
1 MBCL

D. 1 Speed Degrade
1 SBCL
1 SBCG

E. 1 Oxide

F. 44 SBCL
4 MBCL

G. 22 SBCL
1 MBCL

H. 9 SBCL
1 MBCL

I. 1 Lifted Bond

27C256/N27C256

The Intel 27C256 (CERDIP) is a 256K ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). The N27C256 is functionally identical to the 27C256 except that it is housed in a windowless plastic leaded chip carrier (PLCC) package and is one-time programmable.

Number of Bits: 262,144

Organization: 32K x 8

Pin Out: 28 Pin JEDEC Approved (CERDIP), 32 Pin JEDEC Approved (PLCC)

Die Size: 199 x 216 mils

Process: CHMOS II-E

Cell Size: 6 x 6 μM

Programming Voltage: 12.5V

Technology: CMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	0/1059	1/1044	2/400	0/397	0/275	0/272	1/269
1986	2/5724	1/5702	0/690	0/575	0/300	0/300	0/249
Total	2/6783	2/6746	2/1090	0/972	0/575	0/572	1/518
	A	B	C				D

27C256 (Continued)

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake			200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	
1985	1/204	1/199	0/195	0/108
1986	0/772	0/771	0/638	0/153
Total	1/976	1/970	0/833	0/261
	E	F		

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
1.66E + 06 2.68E + 05	0.3 B.I. 0.3*VAF	1.05E + 07 9.38E + 07	6.65E + 06 5.92E + 07	2 0		
			Total 0.3 eV Failures =	2	0.0030	0.0047
1.66E + 06 4.40E + 05 2.68E + 05	0.6 B.I. 0.6 Bake 0.6 HVELT	6.70E + 07 1.20E + 09 1.08E + 07	2.67E + 07 4.74E + 08 4.32E + 06	1 2 1		
			Total 0.6 eV Failures =	4	0.0004	0.0010
1.66E + 06 2.68E + 05	1.0 B.I. 1.0 HVELT	7.89E + 08 1.28E + 08	1.71E + 08 2.76E + 07	1 0		
			Total 1.0 eV Failures =	1	0.0002	0.0010
			Combined Failure Rate:		0.0036	0.0068
			FITs:		36.06	67.68

48 Hour BI Infant Mortality 0.029%

Theta Ja = 36°C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 8 mA

Delta T = 1.512 C
T(55) = 329.6 K
T(70) = 344.6 K
T(125) = 399.6 K
T(250) = 523.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	6.357916	4.015194
Accel.	0.6	40.42309	16.12178
Factors:	1.0	476.1195	102.8857
250° Bake	0.3	N/A	N/A
Accel.	0.6	2722.141	1076.682
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 1 Speed Degrade
1 Oxide Breakdown
B. 1 Contamination (1.0)
1 Decoder Failure
C. 1 SBCG
1 Decoder Failure
D. 1 SBCL
E. 1 SBCG
F. 1 SBCL

27512/27513

The Intel 27512 and 27513 are 512K ultraviolet erasable and Electrically Programmable Read Only Memories (EPROMs). For reliability purposes, both models are treated as one since their design and manufacturing processes are identical. The 27512 is organized as a 64K x 8 device while the 27513 contains four separate 16K x 8 pages of memory.

Number of Bits: 524,288

Organization: 64K x 8 (27512), 16K x 8 x 4 pages (27513)

Pin Out: 28 pin, JEDEC Approved Industry Standard

Die Size: 185 x 317 mils

Process: HMOS II-E

Cell Size: 6 x 6 μM

Programming Voltage: 12.5V

Technology: NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	2/4074	1/3613	0/460	0/460	—	—	—
1986	8/12725	8/12709	2/1150	0/1032	0/53	0/53	0/53
Total	10/16799	9/16322	2/1610	0/1492	0/53	0/53	0/53
	A	B	C				

Table 2. Additional Qualification Tests

Year	Data Retention Bake		200 Temp Cycles
	48 Hrs	168 Hrs	
1985	2/516	2/512	—
1986	22/1535	8/1505	0/30
Total	24/2051	10/2017	0/30
	D	E	

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
3.24E + 06	0.3 B.I.	1.77E + 07	1.17E + 07	0		
2.65E + 04	0.3*VAF	7.98E + 06	5.25E + 0.6	0		
			Total 0.3 eV Failures =	0	0.0036	0.0054
3.24E + 06	0.6 B.I.	9.72E + 07	4.20E + 07	10		
3.40E + 05	0.6 Bake	9.27E + 08	3.67E + 08	34		
2.65E + 04	0.6 HVELT	7.95E + 05	3.43E + 05	0		
			Total 0.6 eV Failures =	44	0.0045	0.0114
3.24E + 06	1.0 B.I.	9.39E + 08	2.31E + 08	1		
2.65E + 04	1.0 HVELT	7.68E + 06	1.89E + 06	0		
			Total 1.0 eV Failures =	1	0.0002	0.0009
			Combined Failure Rate:		0.0083	0.0176
			FITs:		83.03	176.42

48 Hour BI Infant Mortality 0.059%

27512/27513 (Continued)

						Thermal Accel. Factors	
						55°C	70°C
Theta Ja =	36°C/Watt	Delta T	= 17.01 C				
V_{CC} =	5.25 Volts	T(55)	= 345.1 K	BI/ELT	0.3	5.477770	3.598834
I_{CC} =	90 mA	T(70)	= 360.1 K	Accel.	0.6	30.00596	12.95160
		T(125)	= 415.1 K	Factors:	1.0	289.7428	71.42870
		T(250)	= 523.1 K				
				250° Bake	0.3	N/A	N/A
		K = 8.62E-05 eV/K		Accel.	0.6	2722.141	1076.682
				Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 6 SBCL
3 Speed Degrade
1 MBCG

B. 7 SBCL
1 MBCL
1 Contamination

C. 2 SBCL

D. 14 SBCL
10 MBCL

E. 7 SBCL
3 MBCG

27512/27513
(6 Digit Suffixes)

All Intel 27512 and 27513 with six digit suffixes (i.e., 27512–200V05) are 512K ultraviolet erasable and Electrically Programmable Read Only Memories (EPROMs). These parts differ from the previously described 27512 and 27513 in that they are fabricated on a 15% linear shrink of the existing HMOS II-E process. The compaction of the design does not affect the active area of the EPROM transistor, only the spacing between transistor.

Number of Bits:	524,288
Organization:	64K x 8 (27512), 16K x 8 x 4 Pages (27513)
Pin Out:	28 Pin JEDEC Approved (Industry Standard)

Die Size:	160 x 270 mils
Process:	HMOS II-E (Compacted)
Cell Size:	5 x 5 μM
Programming Voltage:	12.5V
Technology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest				6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	2K Hrs	48 Hrs	168 Hrs	500 Hrs
1986	1/1066	0/1062	0/96	0/89	0/41	0/48	1/48	0/47
	A						B	

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake				Temp Cycles	
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	200 Hrs	1K Hrs
1986	1/100	0/99	0/97	0/97	0/50	0/50
	C					

27010/27011

(Preliminary)

The Intel 27010 and 27011 are 1Mbit ultraviolet erasable and Electrically Programmable Read Only Memories (EPROMs). For reliability purposes, both models are treated as one since their design and manufacturing processes are identical. The 27010 is organized as a 128K x 8 device while the 27011 contains eight separate 16K x 8 pages of memory.

Number of Bits:	1,048,576
Organization:	128K x 8 (27010) 8 x 16K x 8 (27011)
Pin Out:	28 Pin (27011) Pending JEDEC Approval 32 Pin (27010) Pending JEDEC Approval
Die Size:	274 x 283 mils
Process:	HMOS II-E
Cell Size:	5 x 5 μM
Programming Voltage:	12.5V
Technology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest	
		168 Hrs	500 Hrs
1986	0/688	0/667	0/300

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake		200 Temp Cycles
	48 Hrs	168 Hrs	
1986	2/109	2/104	0/35
	A	B	

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 2 SBCL

B. 1 SBCL
1 V_{PP} Open

27210
(Preliminary)

The Intel 27210 is a 1Mbit ultraviolet erasable and Electrically Programmable Read Only Memory (EPROM). This device features wordwide (x16) outputs.

Number of Bits:	1,048,576
Organization:	64K x 16
Pin Out:	40 Pin JEDEC Approved Industry Standard
Die Size:	282 x 312 Mils
Process:	HMOS II-E
Cell Size:	5x5 μM
Programming Voltage:	12.5V
Techonology:	NMOS

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1986	0/403	0/403	1/196	0/195	0/98	0/98	0/98
			A				

Table 2. Additional Qualification Tests

Year	250°C Data Retention Bake				200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	
1986	1/100	1/98	1/97	1/94	1/73
	B	C	D	E	F

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 1 SBCL
B. 1 SBCL
C. 1 SBCL
D. 1 SBCL
E. 1 SBCL
F. 1 Open Contact

Plastic Reliability Data Summary

INTRODUCTION

The following information is written to provide OTP (one time programmable) users with the description and reliability summary of Intel's plastic production EPROMs in both DIP and PLCC packages. It includes brief test descriptions, a description of plastic packaging compounds and the reliability data obtained during the qualification and subsequent product monitors of the P2732A, P2764A, N27C64/N87C64, P27128A, P27256 and N27C256 devices.

PLASTIC PACKAGE CHARACTERISTICS

The EPROM plastic package is composed of flame retardant plastic/epoxy. Intel uses Nitto HC-10, Type 2 epoxy which meets the rating requirements of US94V0 $\frac{1}{8}$" minimum. The die attach incorporates a silver-filled adhesive die attach on a silver spot plated leadframe. Bonding is accomplished through gold thermal compression bonding and lead finish is 60/40 solder dipped tin/lead.

EPROM ELECTRICAL CHARACTERISTICS

OTP EPROMs in plastic are tested to the same electrical/parametric levels as their counterparts in CERDIP. The characteristics include input/output voltage levels, speeds, leakage, and power requirement characteristics over the full commercial temperature operating range of 0°C–70°C. Performance capabilities are identical to that of CERDIP EPROMs with speeds to 200 ns currently available.

RELIABILITY/QUALITY STRESSES

High Temperature 125°C Dynamic Lifetest (HTDL)—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test, the memory is sequentially addressed and outputs are exercised but not monitored or loaded. A checkerboard data pattern is typically used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with failure analysis. In order to best determine long-term failure rates, all devices used for lifetesting are subjected to a standard Intel screening. The 48-hour burn-in results measure infant mortality and are not included in the failure rate calculations.

High Temperature Extended Lifetest (HTELT)—This test is also performed at 125°C but uses a smaller sample size. The parts are kept in the full active mode for the duration of the test with outputs driven. The test is intended to evaluate the long-term reliability of the product.

High Voltage 6.5V Extended Lifetest (HVELT)—This test is used to accelerate oxide breakdown failures. The test is set up identical to the one used for dynamic lifetest except for V_{CC} and V_{PP} which are raised to 6.5V. The acceleration factor for this configuration on Intel HMOS IIE product has been determined to be 55 and is applicable to the 0.3 eV failure mode components.

High Temperature Storage—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 99%+ program pattern to a 140°C bake with no applied bias. In addition to data retention, this test can also be used to detect mechanical reliability problems such as bond integrity or process instabilities. The test is sometimes referred to as a data retention bake test.

Programmability—Device programmability is routinely monitored through the process of programming the devices for product monitors and qualifications. Programmability is treated as a distinct part of a product qualification. All voltage combinations are qualified. Program margin is measured and tested on 100% of Intel EPROM products. The new Quick-Pulse Programming™ Algorithm has been extensively verified and the data easily surpasses the 99.5% programmability criteria of Intel's qualification requirements. Qualification results are presented in the following table:

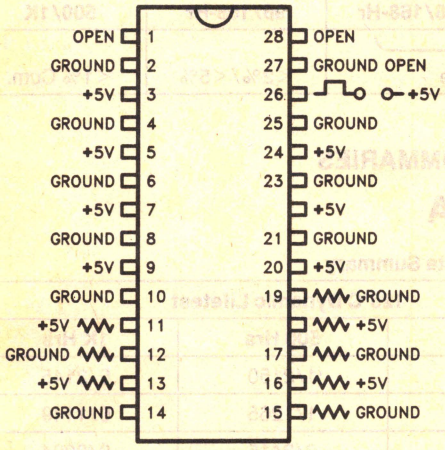
Product	Quality	# Fail	% Yield
P2764A	1800	0	100%
P27128A	1700	0	100%
P27256	8000	2*	99.97%

*Slow to program bits on both failures

MOISTURE RESISTANCE

Two types of moisture resistance testing are performed by Intel. The first is 85°C/85% relative humidity stressing and the second is steam stressing consisting of 121°C, 2 atm.

During the 85°C/85% relative humidity test, the devices are subjected to a high temperature, high humidity environment. The object of the test is to accelerate failure mechanisms through an electrolytic process. This is accomplished through a combination of moisture penetration of the plastic, voltage potentials and contamination which, if present, would combine with the moisture to act as an electrolyte. See Figure 1 for typical 85/85 Bias Diagram.

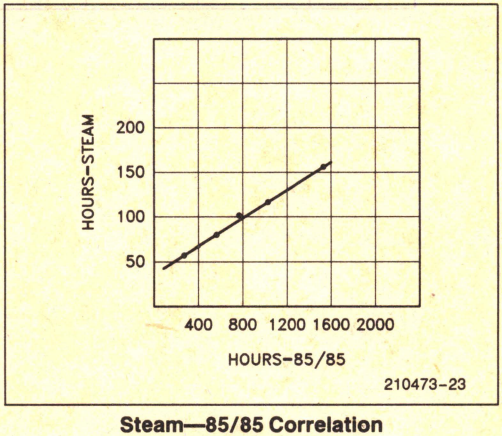


Pin	Pin Name	Stress
	(P2764A)	
1	V_{PP}/N.C.	Open
2	A12/N.C.	Ground
3	A7	+5V
4	A6	Ground
5	A5	+5V
6	A4	Ground
7	A3	+5V
8	A2	Ground
9	A1	+5V
10	A0	Ground
11	O0	+5V
12	O1	Ground
13	O2	+5V
14	Ground	Ground
15	O3	Ground
16	O4	+5V
17	O5	Ground
18	O6	+5V
19	O7	Ground
20	$\overline{CE}$	+5V
21	A10	Ground
22	$\overline{OE}$	+5V
23	A11	Ground
24	A9	+5V
25	A8	Ground
26	N.C./V_{CC}	+5V/Open
27	$\overline{PGM}$/N.C.	Ground
28	V_{CC}/N.C.	Open

Figure 1. Typical 85/85 Bias Diagram

Steam stressing accelerates moisture penetration through the plastic package material to the surface of the die. The objective of this test is to accelerate failures of the device as a result of moisture on the die surface. Corrosion, as typically seen in plastic encapsulated devices, is a very minor contributor to the EPROM failure mechanisms. Through cleanliness in sort, assembly, contamination free plastics, and multi-layer passivation schemes, corrosion has all but been eliminated as a failure mechanism. However, due to the floating gate storage cell composition, EPROMs have a distinctive failure mode which requires special considerations and solutions. The floating gate itself is a highly phosphorous doped structure on which electrons are stored, thus creating the non-volatile memory cell. Passivation defects or marginalities can allow moisture penetration to a single EPROM cell causing oxide deterioration, thus showing up as a charge loss failure. This becomes the predominant failure mode for EPROMs, opposed to corrosion which historically has been the dominant plastic mode of failure. Intel has developed a proprietary, multi-layer passivation which has successfully solved this problem.

Intel has achieved excellent correlation of steam stressing to 85°C/85% RH performance as a result of extensive failure mechanism characterization. We have found, due to this correlation, that steam stressing is an effective and much more time efficient measurement of product moisture reliability.



Steam—85/85 Correlation

QUALITY/RELIABILITY STANDARDS

The table below contains Intel's current requirements for qualification for plastic OTP EPROMs. The failure rate criteria has been established based on a survey of major customers world-wide. Intel consistently meets or exceeds these requirements.

HTDL 48-Hr	HTELT 168/500-Hr	140°C Bake 48/168/500-Hr	HVELT 48/168-Hr	Steam 96/168-Hr	85/85 500/1K
<.05%	<200 FITs Combined Failure Rate			<2%/<5%	<1% Cum.

PRODUCT SPECIFIC RELIABILITY DATA SUMMARIES

P2732A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs
1985	17/14560	1/14393	1/2150	0/2145
1986	6/7366	2/7358	1/1265	0/1149
Total	23/21926	3/21751	2/3415	0/3294
	A	B	C	

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake				85°C/85% RH		Steam	200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	96 Hrs	
1985	0/2594	0/2594	0/2594	0/2594	3/1649	7/1644	8/1476	0/703
1986	0/1290	0/1290	0/1290	1/1276	2/900	2/896	3/858	0/200
Total	0/3884	0/3884	0/3884	1/3870	5/2549	9/2540	11/2334	0/903
				D	E	F	G	

P2732A (Continued)

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
5.39E + 06	0.3 B.I.	2.31E + 07	1.62E + 07	1		
0.00E + 00	0.3*VAF	0.00E + 00	0.00E + 00	0		
			Total 0.3 eV Failures =	1	0.0087	0.0125
5.39E + 06	0.6 B.I.	9.92E + 07	4.87E + 07	3		
1.94E + 06	0.6 Bake	1.53E + 08	6.04E + 07	1		
0.00E + 00	0.6 HVELT	0.00E + 00	0.00E + 00	0		
			Total 0.6 eV Failures =	4	0.0021	0.0048
5.39E + 06	1.0 B.I.	6.91E + 08	2.11E + 08	1		
0.00E + 00	1.0 HVELT	0.00E + 00	0.00E + 00	0		
			Total 1.0 eV Failures =	1	0.0003	0.0010
			Combined Failure Rate:		0.0111	0.0182
			FITs:		111.03	182.20

48 Hour BI Infant Mortality 0.10%

Theta Ja = 113° C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 80 mA

Delta T = 47.46 C
T(55) = 375.6 K
T(70) = 390.6 K
T(125) = 445.6 K
T(140) = 413.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT Accel. Factors:	0.3	4.288910	3.004446
	0.6	18.39475	9.026699
	1.0	128.1808	39.13346
140° Bake Accel. Factors:	0.3	N/A	N/A
	0.6	78.68867	31.12355
	1.0	N/A	N/A

Voltage Accel. Factor (VAF) for HVELT on this process is = 10.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 2 Speed Degrade (1.0)
1 Ass'y Defect (Bond)
19 SBCL
1 MBCG

B. 1 SBCL
1 Speed Degrade
1 SBCG

C. 1 SBCG
1 Contamination (1.0)

D. 1 SBCG

E. 1 Corrosion
1 Cracked Die
1 Leakage
2 Passivation Defects

F. 3 Corrosion
1 SBCL
1 Lifted Bond
4 Passivation Defects

G. 6 SBCL
1 Leakage
2 Contamination
2 Passivation Defect

P2764A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs
1985	2/5740	0/3912	0/760	0/758
1986	3/5672	1/4837	0/805	0/688
Total	5/11412	1/8749	0/1565	0/1446
	A	B		

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake				Steam	200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	168 Hrs	
1985	0/816	0/816	0/816	0/814	—	
1986	0/903	0/903	0/903	0/903	10/1571	0/100
Total	0/1719	0/1719	0/1719	0/1717	10/1571	0/100

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.29E + 06	03 B.I.	1.21E + 07	8.01E + 06	0		
0.00E + 00	03*VAF	0.00E + 00	0.00E + 00	0		
			Total 0.3 eV Failures =	0	0.0076	0.0114
2.29E + 06	0.6 B.I.	6.34E + 07	2.80E + 07	1		
8.60E + 05	0.6 Bake	6.76E + 07	2.68E + 07	0		
0.00E + 00	0.6 HVELT	0.00E + 00	0.00E + 00	0		
			Total 0.6 eV Failures =	1	0.0015	0.0037
2.29E + 06	1.0 B.I.	5.80E + 08	1.48E + 08	0		
0.00E + 00	1.0 HVELT	0.00E + 00	0.00E + 00	0		
			Total 1.0 eV Failures =	0	0.0002	0.0006
			Combined Failure Rate:		0.0093	0.0157
			FITs:		92.91	157.40

48 Hour BI Infant Mortality 0.044%

P2764A (Continued)

					Thermal Accel. Factors	
					55°C	70°C
Theta Ja =	103° C/Watt	Delta T = 21.63 C				
V_{CC} =	5.25 Volts	T(55) = 349.7 K	BI/ELT	0.3	5.258072	3.492002
I_{CC} =	40 mA	T(70) = 364.7 K	Accel.	0.6	27.64732	12.19407
		T(125) = 419.7 K	Factors:	1.0	252.7873	64.60234
		T(140) = 413.1 K				
			140° Bake	0.3	N/A	N/A
		K = 8.62E-05 eV/K	Accel.	0.6	78.68867	31.12355
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 3 SBCL
2 Oxide

B. 1 SBCL

N27C64/N87C64

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest
		168 Hrs	500 Hrs	1K Hrs	500 Hrs
1986	0/300	0/300	0/150	0/150	0/140

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake		85°C/85% RH		Steam	200 Temp Cycles
	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	96 Hrs	
1986	0/297	0/297	1/300	0/298	1/300	0/234
			A		B	

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 1 Basic Function

B. 1 Output

P27128A

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1986	5/11068	3/11060	0/1530	2/1530	0/210	0/210	0/210
	A	B		C			

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake				85°C/85% RH		Steam	200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	168 Hrs	
1986	0/642	0/622	1/608	0/645	4/1062	12/1058	13/4200	0/125
			D		E	F		

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.60E + 06	0.3 B.I.	1.27E + 07	8.62E + 06	0		
1.05E + 05	0.3*VAF	2.83 + 07	1.92E + 07	0		
			Total 0.3 eV Failures =	0	0.0022	0.0033
2.60E + 06	0.6 B.I.	6.25E + 07	2.86E + 07	2		
3.07E + 05	0.6 Bake	2.42E + 07	9.56E + 06	1		
1.05E + 05	0.6 HVELT	2.52E + 06	1.16E + 06	0		
			Total 0.6 eV Failures =	3	0.0047	0.0106
2.60E + 06	1.0 B.I.	5.21E + 08	1.41E + 08	3		
1.05E + 05	1.0 HVELT	2.10E + 07	5.71E + 06	0		
			Total 1.0 eV Failures =	3	0.0008	0.0028
			Combined Failure Rate:	3	0.0077	0.0167
			FITs:		76.78	167.47

48 Hour BI Infant Mortality 0.045%

P27128A (Continued)

					Thermal Accel. Factors	
Theta Ja =	95° C/Watt	Delta T = 29.92 C			55°C	70°C
V_{CC} =	5.25 Volts	T(55) = 358.0 K	BI/ELT	0.3	4.903250	3.316731
I_{CC} =	60 mA	T(70) = 373.0 K	Accel.	0.6	24.04186	11.00070
		T(125) = 428.0 K	Factors:	1.0	200.2688	54.41278
		T(140) = 413.1 K				
			140° Bake	0.3	N/A	N/A
		K = 8.62E-05 eV/K	Accel.	0.6	78.68867	31.12355
			Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 3 Decode
1 Output
1 SBCL
B. 1 MBCG
1 MBCL
1 Speed Degrade
C. 2 Output
D. 1 SBCL
E. 1 SBCL
1 Decode
2 Open
F. 1 Output
3 Decode
3 Leakage
6 Open

P27256

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1985	2/1969	0/1964	0/345	0/345	—	—	—
1986	26/8075	3/8016	4/1035	1/913	1/96	0/95	0/95
Total	28/10044	3/9980	4/1380	1/1258	1/96	0/95	0/95
	A	B	C	D	E		

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake				85°C/85% RH		Steam	200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	1K Hrs	500 Hrs	1000 Hrs	168 Hrs	
1985	0/487	0/487	0/487	0/478	2/298	8/296	—	—
1986	0/1405	0/1405	1/1405	2/1288	3/896	7/891	101/11972	0/175
Total	0/1892	0/1892	1/1892	2/1766	5/1194	15/1187	101/11972	
			F	G	H	I		

P27256 (Continued)

Table 3. Failure Rate Predictions

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hrs (60% UCL)	
		55°C	70°C		55°C	70°C
2.28E + 06	0.3 B.I.	1.05E + 07	7.24E + 06	3		
4.75E + 04	0.3*VAF	1.20E + 07	8.28 + 06	0		
			Total 0.3 eV Failures =	3	0.0185	0.0269
2.28E + 06	0.6 B.I.	4.85E + 07	2.29E + 07	5		
9.46E + 05	0.6 Bake	7.44E + 07	2.94E + 07	3		
4.75E + 04	0.6 HVELT	1.01E + 06	4.77E + 05	1		
			Total 0.6 eV Failures =	9	0.0084	0.0198
2.28E + 06	1.0 B.I.	3.72E + 08	1.07E + 08	0		
4.75E + 04	1.0 HVELT	7.74E + 06	2.22E + 06	0		
			Total 1.0 eV Failures =	0	0.0002	0.0008
			Combined Failure Rate:		0.0272	0.0476
			FITs:		271.85	475.55

48 Hour BI Infant Mortality 0.28%

Theta Ja = 90° C/Watt
V_{CC} = 5.25 Volts
I_{CC} = 80 mA

Delta T = 37.8 C
T(55) = 365.9 K
T(70) = 380.9 K
T(125) = 435.9 K
T(140) = 431.1 K

K = 8.62E-05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	4.607027	3.167630
Accel.	0.6	21.22470	10.03388
Factors:	1.0	162.7056	46.67829
140° Bake	0.3	N/A	N/A
Accel.	0.6	78.68867	31.12355
Factors:	1.0	N/A	N/A

Voltage Accel. Factor (VAF)
for HVELT on this process is = 55.00

NOTE:
FIT = Failures in Time. 1 FIT = 1 failure per 10^9 device hours.

Failure Analysis:

A. 24 SBCL
1 SBCG
3 Decode
B. 1 SBCL
2 Decode
C. 2 SBCG
1 MBCG
1 Decode
D. 1 SBCL
E. 1 SBCL
F. 1 SBCL
G. 1 SBCL
1 MBCL
H. 3 SBCL
2 Corrosion
I. 13 Corrosion
2 SBCL

N27C256

Table 1. Reliability Data Summary

Year	Burn-In 48 Hrs	125°C Dynamic Lifetest			6.5V Dynamic Lifetest		
		168 Hrs	500 Hrs	1K Hrs	48 Hrs	168 Hrs	500 Hrs
1986	3/678	1/637	1/300	3/291	0/125	0/125	0/123
	A	B	C	D			

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake			85°C/85% RH		Steam		200 Temp Cycles
	48 Hrs	168 Hrs	500 Hrs	500 Hrs	1000 Hrs	96 Hrs	168 Hrs	
1986	0/125	0/125	0/125	1/149	1/147	3/300	1/150	0/50
				E		F	G	

Failure Rate Predictions: Due to the small number of actual device hours on this new product, a detailed reliability prediction would not be meaningful.

Failure Analysis:

A. 2 Leakage
1 Open Pin
B. 1 Basic Function
C. 1 Basic Function
D. 2 Basic Function
1 Leakage
E. 1 Basic Function
F. 1 Basic Function
2 Leakage
G. 1 Basic Function

APPENDIX A
Failure Rate Calculations for 60% Upper Confidence Level

Step 1. Accumulate data from 48 hours of burn-in through lifetest of each lot. (Note: 48 hour burn-in results measure infant mortality and are not included in the failure rate calculation.)

Step 2. Determine the failure mechanism for each failure and assign an activation energy (E_A) corresponding to each failure mechanism. (See Table 1 below.)

Table 1. Failure Mechanism Activation Energies Relevant to EPROMs

Failure Mode	Activation Energy
Defective bit charge gain/loss	0.6 eV
Oxide breakdown	0.3 eV
Silicon defects	0.3 eV
Contamination	1.0–1.2 eV
Intrinsic charge loss	1.4 eV

Step 3. Calculate the total number of device hours from 48 hours of burn-in through lifetest.

Example: 125°C Burn-In/Lifetest and a 2 lot sample

$$\frac{X}{Y} = \frac{\text{\# failures}}{\text{total \# devices}}$$

	48 Hours	168 Hours	500 Hours	1K Hours	2K Hours
Lot #1	0/1000	1/1000	0/999	0/998	0/994
Lot #2	0/221	0/201	1/201	1/100	0/99
Totals	0/1221	1/1201	1/1200	1/1098	0/1093

Device Hours = (Number of Devices) (Number of Hours)

Total Device Hours = 1201 (168 hrs – 48 hrs) + 1200 (500 hrs – 168 hrs)

+ 1098 (1000 hrs – 500 hrs) + 1093 (2000 hrs – 1000 hrs)

= 1201 (120 hrs) + 1200 (332 hrs) + 1098 (500 hrs)

+ 1093 (1000 hrs)

= 2.185×10^6 Device Hours .

Step 4. Use E_A tables to find the equivalent device hours at a desired temperature for each activation energy (failure mechanism), or use the Arrhenius relation.

$$R = A \bullet \exp\left[\frac{E_A}{KT}\right]$$

K = 8.617×10^{-5} eV/°Kelvin (Boltzmann's constant)
A = proportionality constant
R = mean rate to failure
E_A = activation energy
T = temperature in Kelvin

$$\frac{R_1}{R_2} = \frac{A \bullet \exp\left[\frac{E_A}{KT_1}\right]}{A \bullet \exp\left[\frac{E_A}{KT_2}\right]} = \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

$A_1 = A_2 = A$ for the same failure mechanism (i.e., same E_A)

$$R_1 = R_2 \bullet \exp\left[\left(\frac{E_A}{K}\right)\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

For example: For $E_A = 0.6$ eV, $T_2 = 398.15°K$, $T_1 = 328.15°K$

$$R_2 = .024\, R_1, \text{ or } R_1 = 41.7\, R_2$$

Therefore, 1 hour at 125°C is equivalent to 41.7 hours at 55°C for a failure mechanism of activation energy E_A = 0.6 eV. Then 41.7 is the thermal acceleration factor for ΔT.

Step 5. Organize the burn-in/lifetest data by E_A, Total Device Hours at the burn-in/lifetest temperature T_2, Thermal Acceleration Factors for each failure mechanism (E_A), Number of Failures for each failure mechanism, and the calculated equivalent device hours at the desired operating temperature T_1.

NOTE:
The rise in junction temperature due to the thermal resistivity of the package (θ_{JA}) must be added to the desired and actual burn-in/lifetest temperatures.

$$T_{test} = T_J + T_{Ambient} = \theta_{JA}\,(IV @ T_{Ambient}) + T_{Ambient}$$

E_A (eV)	Total Device Hrs @ T_2	Acceleration Factors	# Fail	Equivalent Hours @ T_1
0.3	T.D.H.	X	N_1	X (T.D.H.)
0.6	T.D.H.	Y	N_2	Y (T.D.H.)
1.0	T.D.H.	Z	N_3	Z (T.D.H.)

Using the data table and the equation below, the failure rates for individual failure mechanisms and the total combined failure rate can be predicted. The total combined failure rate is just the sum of the individual failure rates for each failure mechanism.

For a 60% UCL:

$$\%\ \text{Fail/1K Hours} = \left[\frac{1.049\,(\#\text{failures for a particular } E_A) + 1.0305}{\text{Equivalent Hrs @ } T_1}\right]\left[10^5\right]$$

Example 1:

Assume for this example, that I_{CC} active is 57 mA at $T_{Ambient}$ = 125°C and I_{CC} active is 65 mA at $T_{Ambient}$ = 55°C.

Also assume that θ_{JA} = 35°C/W.

Then,

T_2 = (35°C/W) (57 mA) (5V) + 125°C

≈ 135°C = 408.15°K

T_1 = (35°C/W) (60 mA) (5V) + 55°C

≈ 65°C = 338.15°K

E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours at 55°C	# Fail	55°C % Fail/ 1K Hrs
0.3	2.185×10^6	5.85	1.278×10^7	0	0.0081
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
				Total Combined Failure Rate =	0.0126
				=	126 FITs

Example 2:

Assume that an additional lot of 800 HMOS*IIE devices is burned in using a 6.5V lifetest. Using Table 2 below, a voltage acceleration factor of 55 results from a 20% overstress (5.5V to 6.5V).

	48 Hours	168 Hours	500 Hours
Lot #3	0/800	1/800	0/799

Device Hours = 800 (48 hrs − 0 hrs) + 800 (168 hrs − 48 hrs) + 799 (500 hrs − 168 hrs)
= 3.997×10^5

Table 2. Time-Dependent Oxide Failure Accelerations

Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/CM)	Acceleration Factor at ____% Over Stress			
				10%	20%	50%	100%
NMOS/PMOS	12	1100	1.1	5.9	35	7000	5×10^7
HMOS*E	5	700	0.714	3.2	10	320	99,500
HMOS* II E	5	325	1.25	7.5	55	23,700	5.6×10^8
CHMOS* II E	5	325	1.25	7.5	55	23,700	5.6×10^8

ASSUMES:
1. No Bias Generators
2. Depletion Loads

*HMOS & CHMOS are patented processes of Intel Corporation.

Since this voltage accelerated stress is used to predict an oxide breakdown failure rate, the 5.5V burn-in/lifetest 55°C equivalent hours for $E_A = 0.3$ eV are added to the 6.5V burn-in/lifetest 55°C equivalent hours as follows:

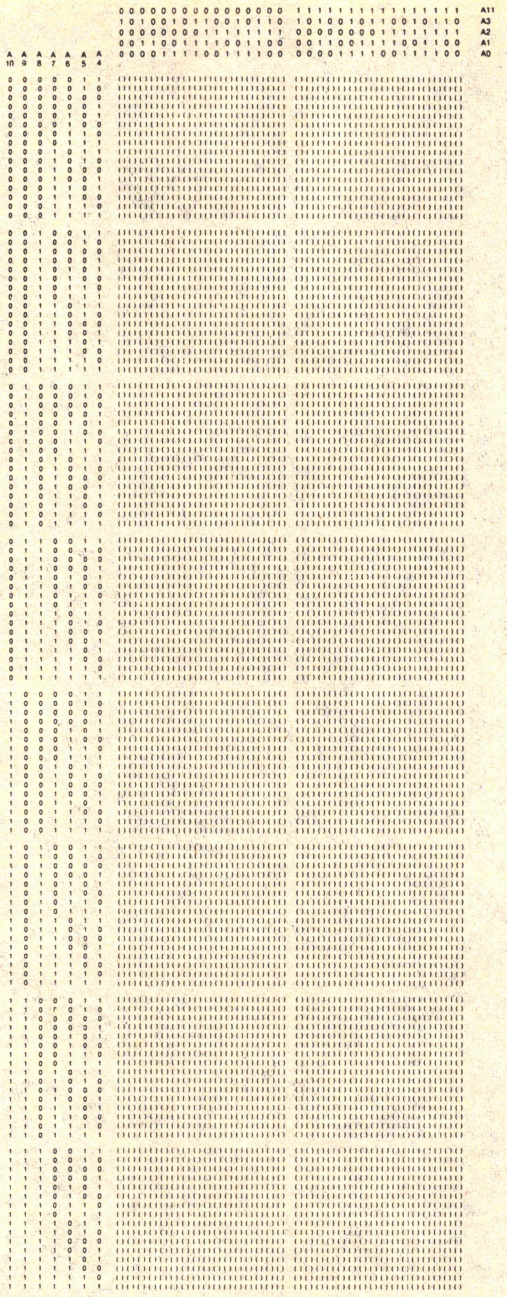
125°C Burn-In/Lifetest	E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C
5.5V	0.3	2.185×10^6	5.85	1.278×10^7
6.5V	0.3	3.997×10^5	(5.85 x 55)	1.286×10^8
			Total Equivalent $E_A = 0.3$ eV Device Hours =	1.414×10^8

The following failure rate predictions include the total equivalent 55°C, $E_A = 0.3$ eV device hours found above:

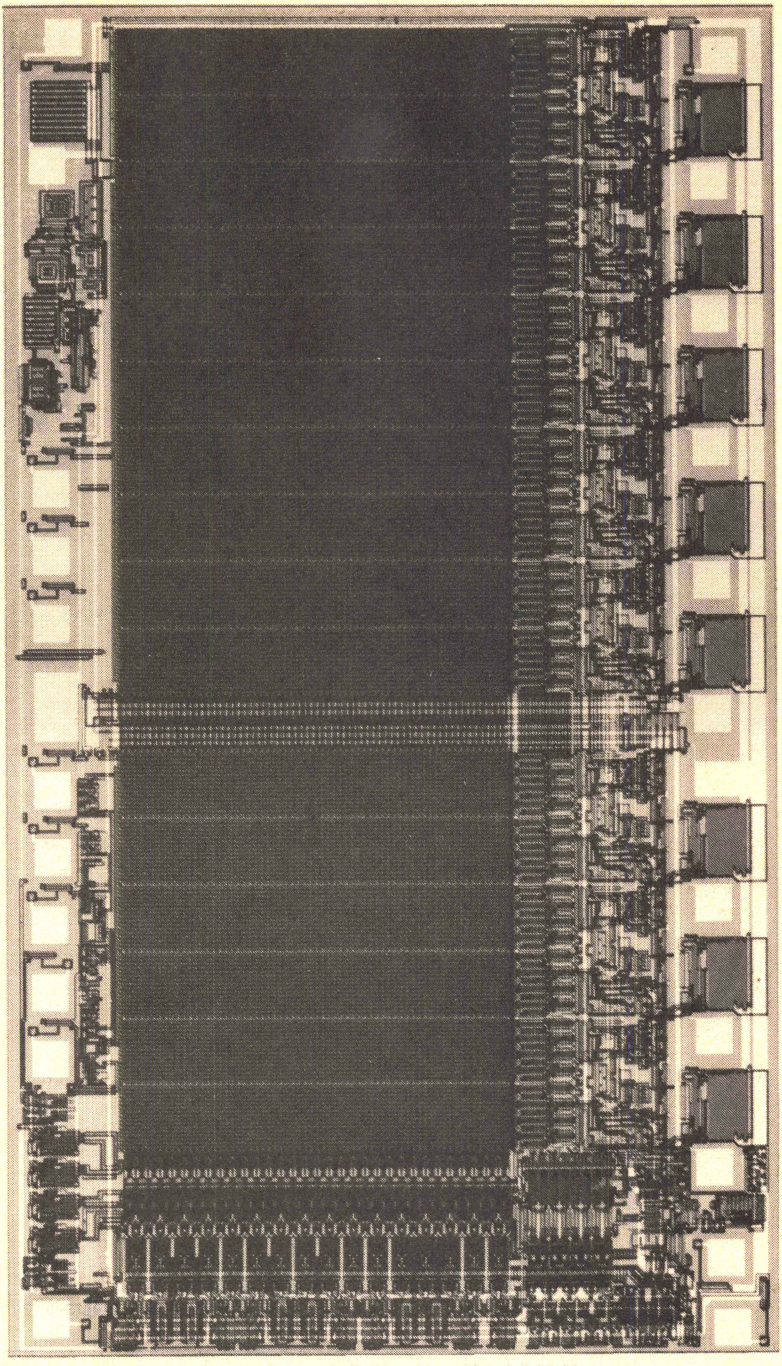
E_A (eV)	Actual Device Hours @ 125°C	Acceleration Factors for 135°C to 65°C	Equivalent Hours @ 55°C	# Fail	55°C % Fail/ 1K Hours
0.3	2.185×10^6	5.85	—	—	—
0.3 + 55(1)	3.997×10^5	(5.85 x 55)	1.414×10^8	1	0.0015
0.6	2.185×10^6	34.18	7.468×10^7	2	0.0042
1.0	2.185×10^6	359.93	7.864×10^8	1	0.0003
			Total Combined Failure Rate =		0.0060
			=		60 FITs

NOTES:
(1) The notation 0.3 + 55 is used to show that 6.5V and 5.5V burn-in/lifetest equivalent hours have been combined.
(2) Additional information on calculating failure rates is contained in the April 2, 1984 International Reliability Physics Symposium editorial entitled "Calculating Failure Rates from Stress Data" by Robert M. Alexander.

APPENDIX B
EPROM Bit Maps and Die Photos



2732A Bit Map (1 of 8 Outputs Shown)



210473-6

2732A Die Photograph

Column Selects

	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}	Y_{16}	Y_{17}	Y_{18}	Y_{19}	Y_{20}	Y_{21}	Y_{22}	Y_{23}	Y_{24}	Y_{25}	Y_{26}	Y_{27}	Y_{28}	Y_{29}	Y_{30}	Y_{31}
A_2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
A_1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A_0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A_{10}	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A_{11}	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0

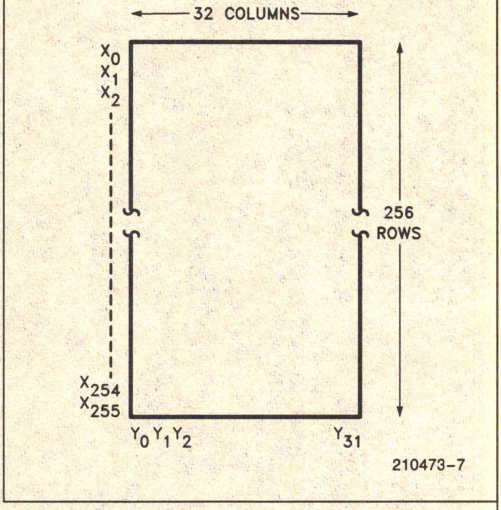
Row Selects

	X_0	X_1	X_2	X_3	X_4	X_5	X_{253}	X_{254}	X_{255}
A_7	0	0	0	0	0	0	1	1	1
A_6	0	0	0	0	0	0	1	1	1
A_5	0	0	0	0	0	0	1	1	1
A_4	0	0	0	0	0	0	1	1	1
A_3	0	0	0	0	0	0	1	1	1
A_{12}	0	0	0	0	1	1	1	1	1
A_9	0	0	1	1	0	0	0	1	1
A_8	0	1	0	1	0	1	1	0	1

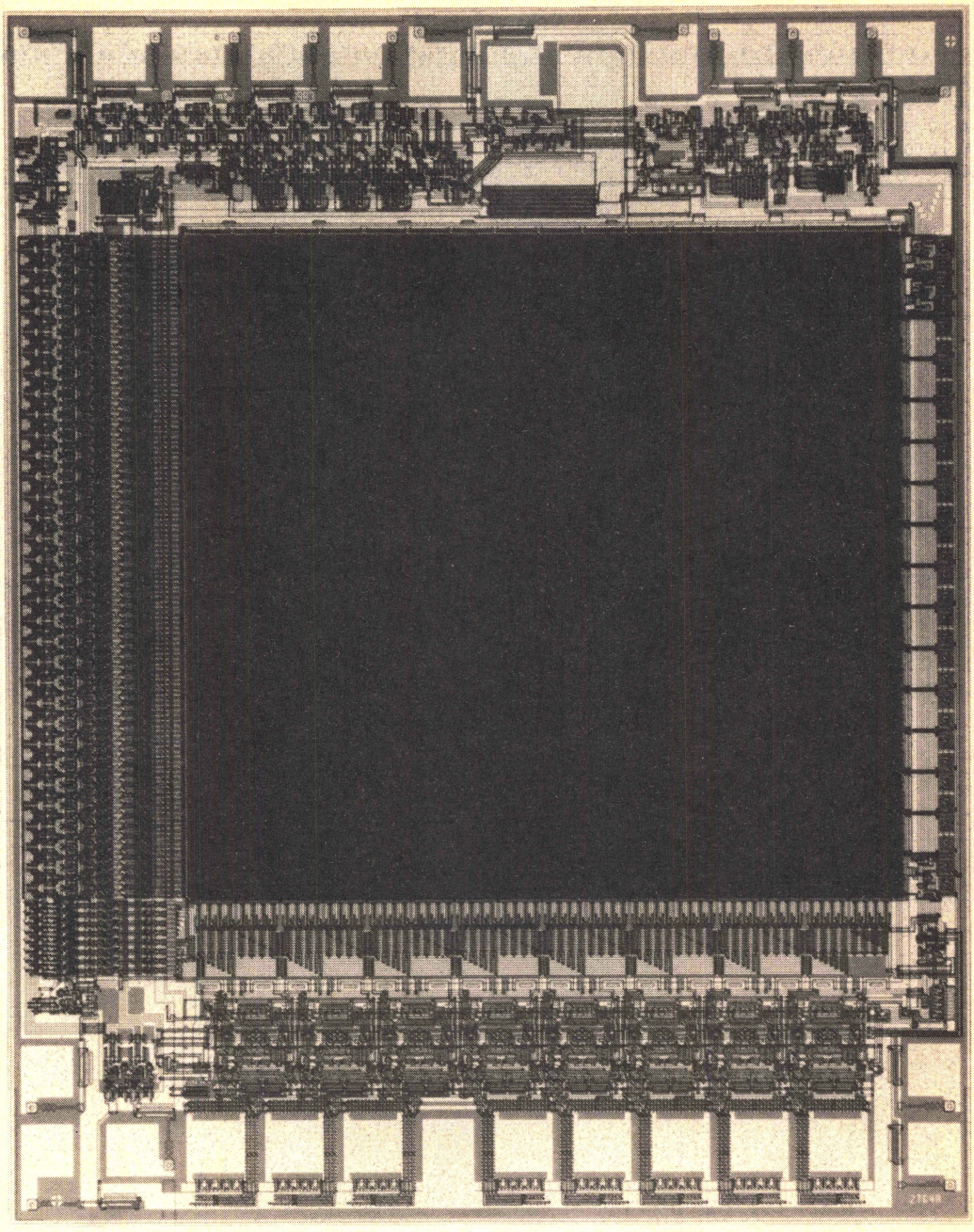
Array Organization

ROW SELECT	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
	Column Select							

Bit Map for One Output (Same for All Outputs)



2764A Bit Map



210473-8

2764A Die Photograph

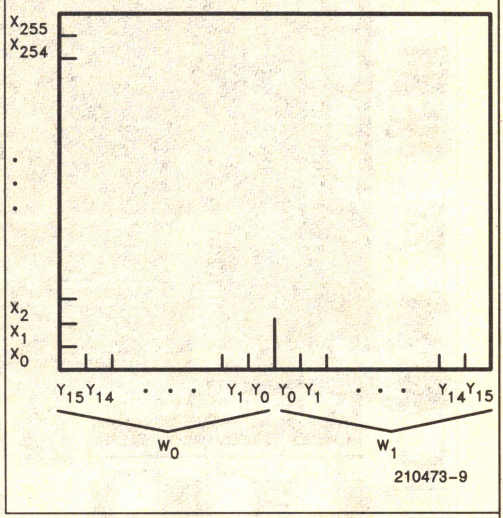
Address Decoding

	X Decode			Z Decode			R Decode			Y Decode				W Decode	
	A_{12}	A_7	A_6	A_{11}	A_9	A_8	A_5	A_4		A_{10}	A_0	A_1	A_3		A_2
X_0	0	0	0	0	0	0	0	0	Y_0	0	0	0	0	W_0	0
X_1	0	0	0	0	0	0	0	1	Y_1	0	0	0	1	W_1	1
X_2	0	0	0	0	0	0	1	0	Y_2	0	0	1	0		
•					•				•						
•					•				•						
•					•				•						
X_{254}	1	1	1	1	1	1	1	0	Y_{14}	1	1	1	0		
X_{255}	1	1	1	1	1	1	1	1	Y_{15}	1	1	1	1		

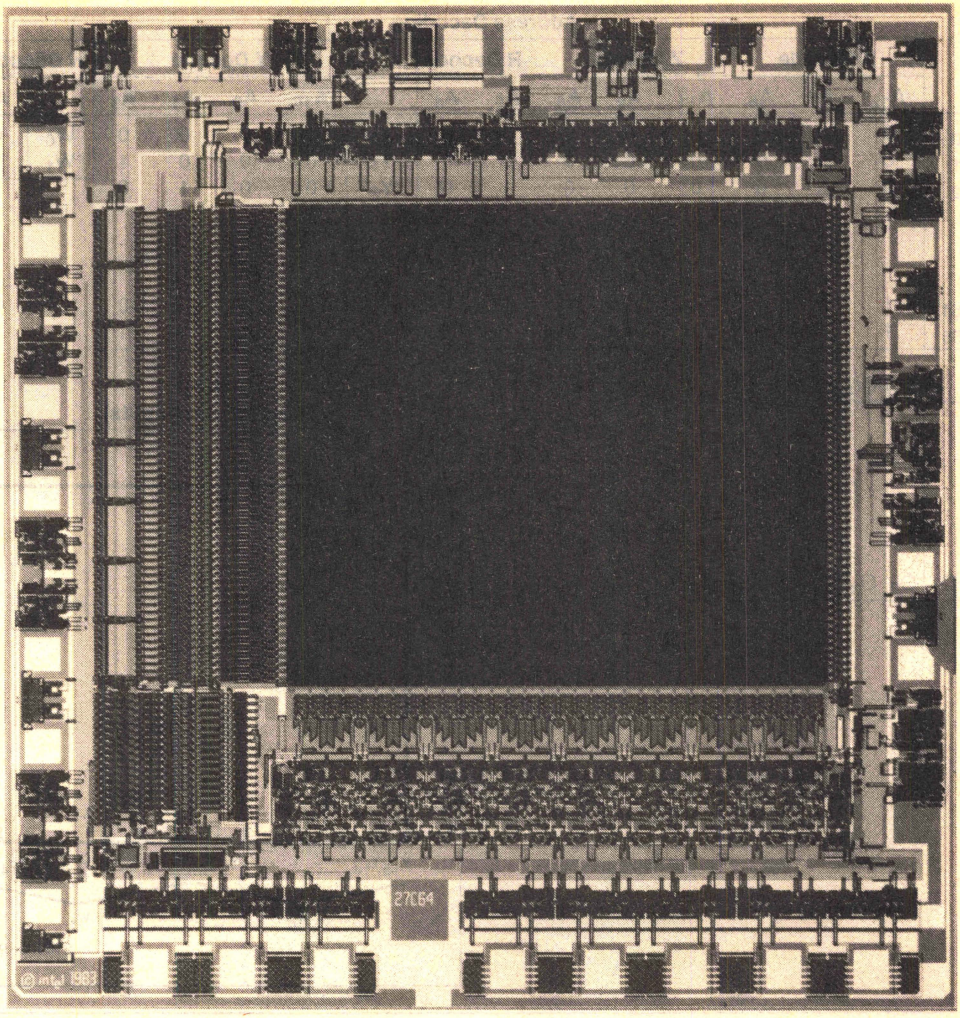
Array Organization

O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7

Bit Map
(Same for All Outputs)

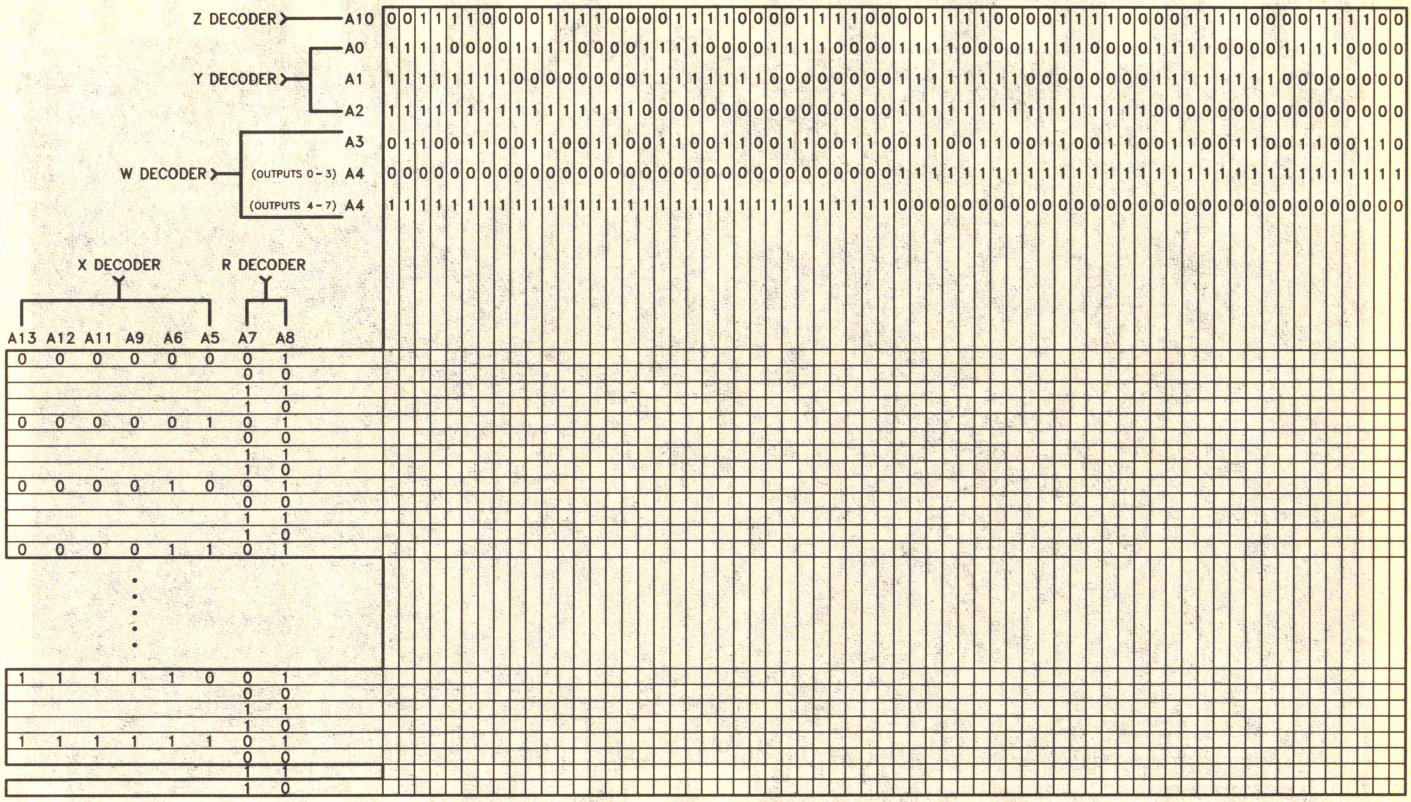


27C64 Bit Map

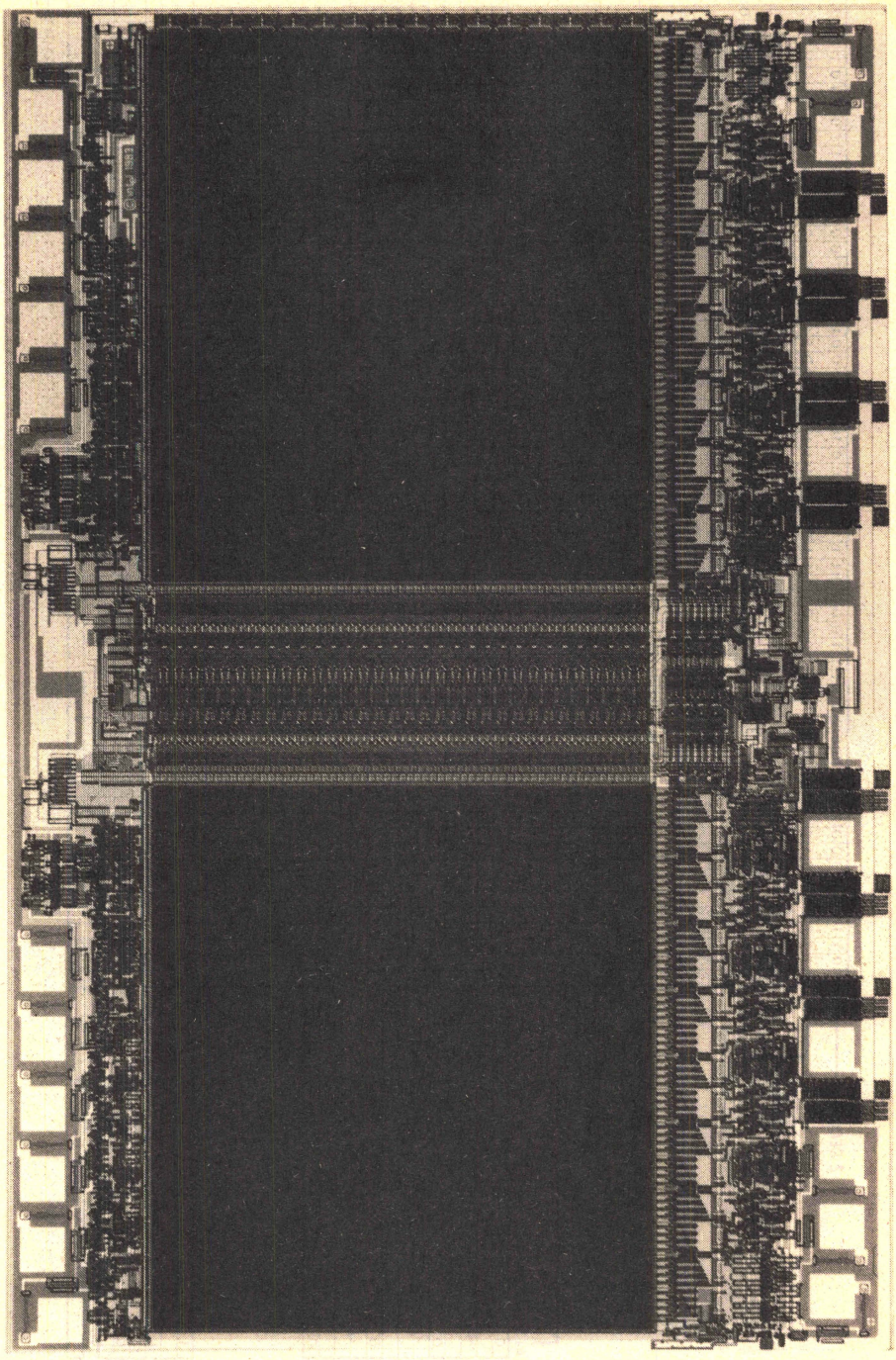


210473-10

27C64 Die Photograph


Z DECODER
A10
Y DECODER
A0
A1
A2
W DECODER
A3
(OUTPUTS 0-3) A4
(OUTPUTS 4-7) A4
X DECODER
R DECODER
A13 A12 A11 A9 A6 A5 A7 A8

210473-14



210473-15

27128A Die Photograph

Address Decoding

Y Decode

	A_4	A_{10}	A_1	A_2
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•		•		
•		•		
•		•		
Y_{15}	1	1	1	1

W Decode

	A_0	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

X Decode

	A_{14}	A_{13}	A_{12}	A_8	A_7	A_6
X_0	0	0	0	0	0	0
X_1	0	0	0	0	0	0
X_2	0	0	0	0	0	0
•				•		
•				•		
•				•		
X_{511}	1	1	1	1	1	1

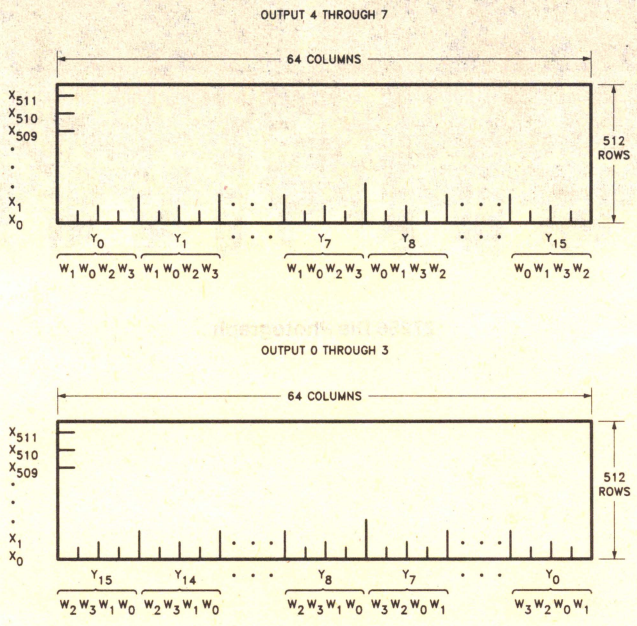
R Decode

	A_{11}	A_9	A_5
X_0	0	0	0
X_1	0	0	1
X_2	0	1	0
X_{511}	1	1	1

Array Organization

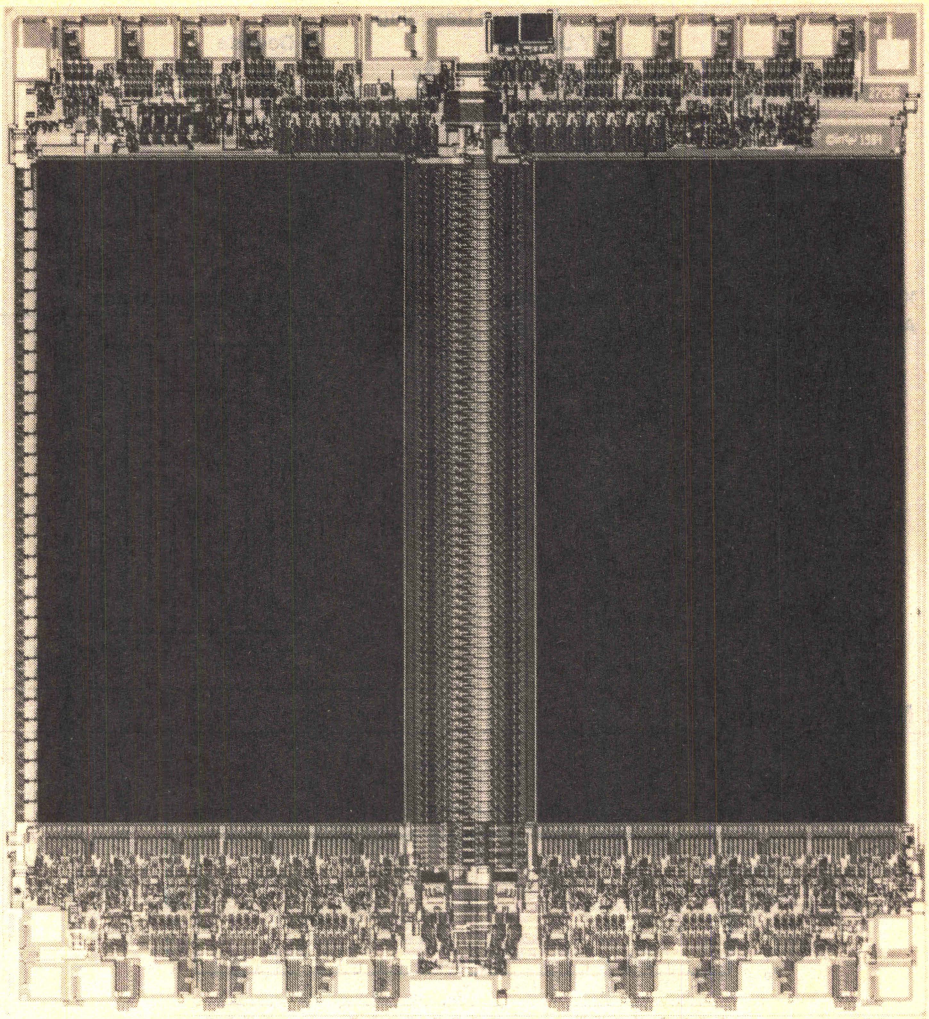
210473-16

Bit Map



210473-17

27256 Bit Map



210473-18

27256 Die Photograph

Address Decoding

4 Decode

	A_2	A_1	A_0	A_{10}
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•				
•				
•				
Y_{15}	1	1	1	1

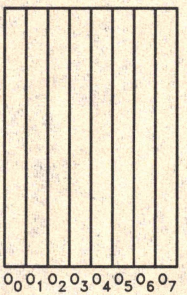
W Decode

	A_4	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

X Decode

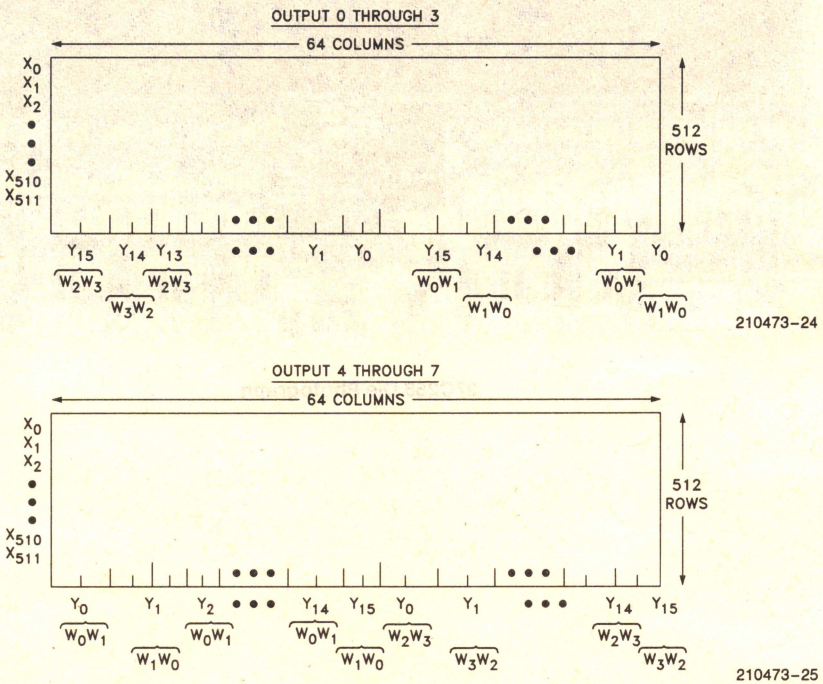
	A_{14}	A_{13}	A_{12}	A_7	A_6	A_5	A_{11}	A_9	A_8
X_0	0	0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0	0	1
X_2	0	0	0	0	0	0	0	1	0
•									
•									
X_{510}	1	1	1	1	1	1	1	1	0
X_{511}	1	1	1	1	1	1	1	1	1

Array Organization



210473-16

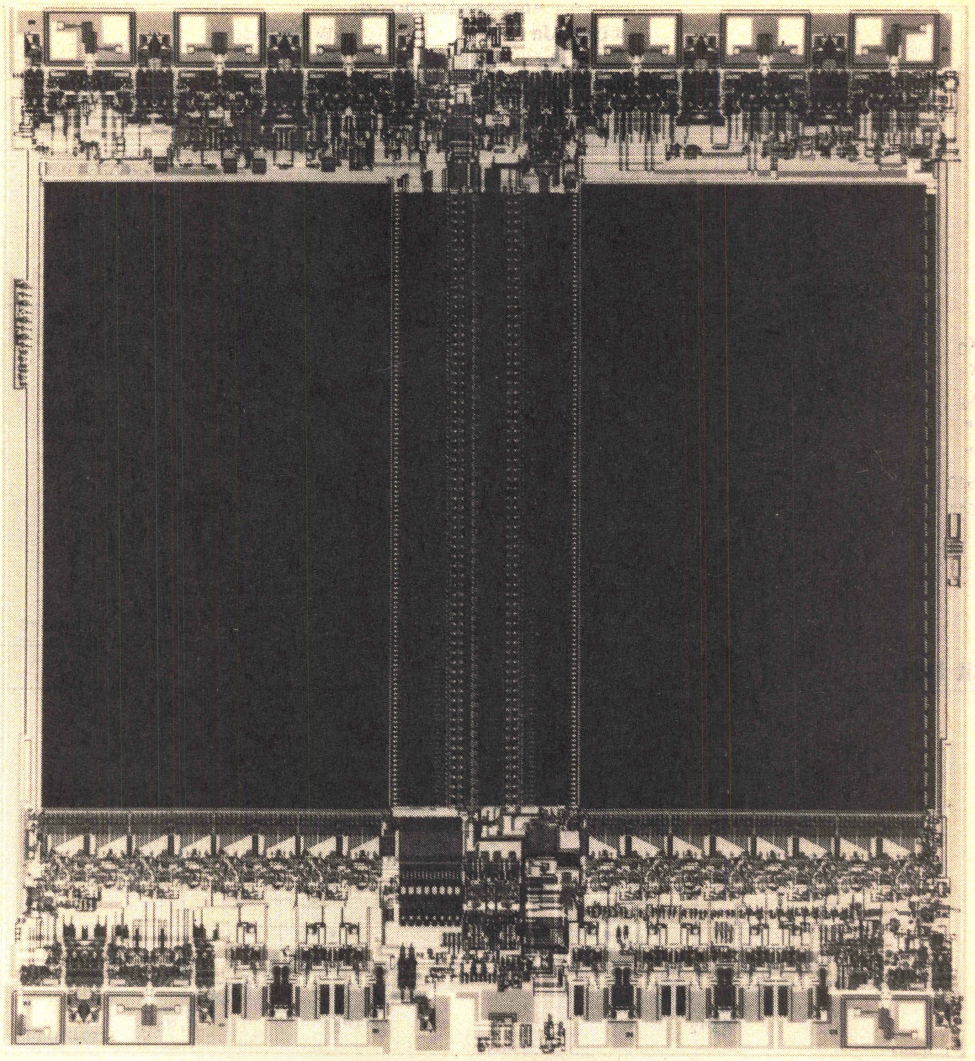
Bit Map


OUTPUT 0 THROUGH 3
64 COLUMNS
512 ROWS
X_0 X_1 X_2 X_{510} X_{511}
Y_{15} Y_{14} Y_{13} Y_1 Y_0 Y_{15} Y_{14} Y_1 Y_0
W_2W_3 W_3W_2 W_2W_3 W_0W_1 W_1W_0 W_0W_1 W_1W_0
OUTPUT 4 THROUGH 7
64 COLUMNS
512 ROWS
X_0 X_1 X_2 X_{510} X_{511}
Y_0 Y_1 Y_2 Y_{14} Y_{15} Y_0 Y_1 Y_{14} Y_{15}
W_0W_1 W_1W_0 W_0W_1 W_0W_1 W_1W_0 W_2W_3 W_3W_2 W_2W_3 W_3W_2

210473-24

210473-25

27C256 Bit Map



210473-26

27C256 Die Photograph

Address Decoding

Y Decode

	A_4	A_{10}	A_1	A_2
Y_0	0	0	0	0
Y_1	0	0	0	1
Y_2	0	0	1	0
•				
•				
•				
Y_{15}	1	1	1	1

W Decode

	A_0	A_3
W_0	0	0
W_1	0	1
W_2	1	0
W_3	1	1

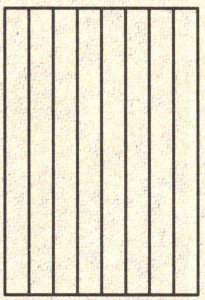
X Decode

	A_{15}	A_{14}	A_{13}	A_{12}	A_8	A_7	A_6
X_0	0	0	0	0	0	0	0
X_1	0	0	0	0	0	0	0
X_2	0	0	0	0	0	0	0
•			•				•
•			•				•
•			•				•
X_{1023}	1	1	1	1	1	1	1

R Decode

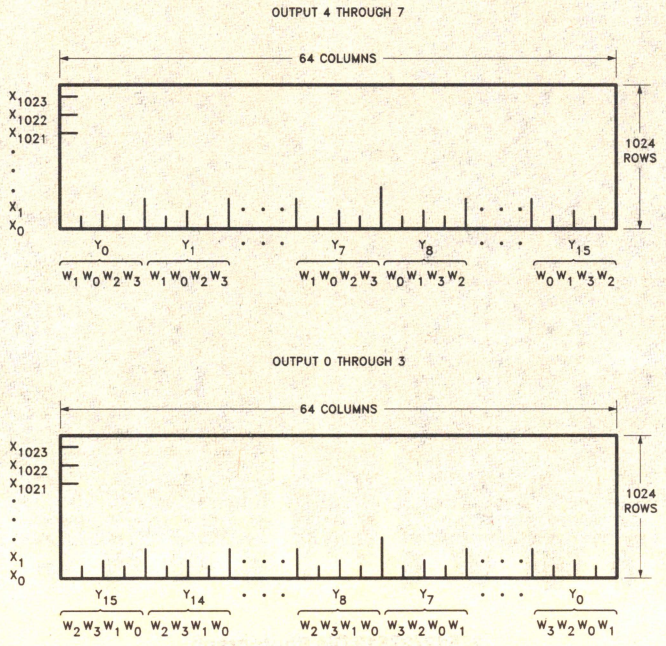
A_{11}	A_9	A_5
0	0	0
0	0	1
0	1	0
•		•
•		•
•		•
1	1	1

Array Organization



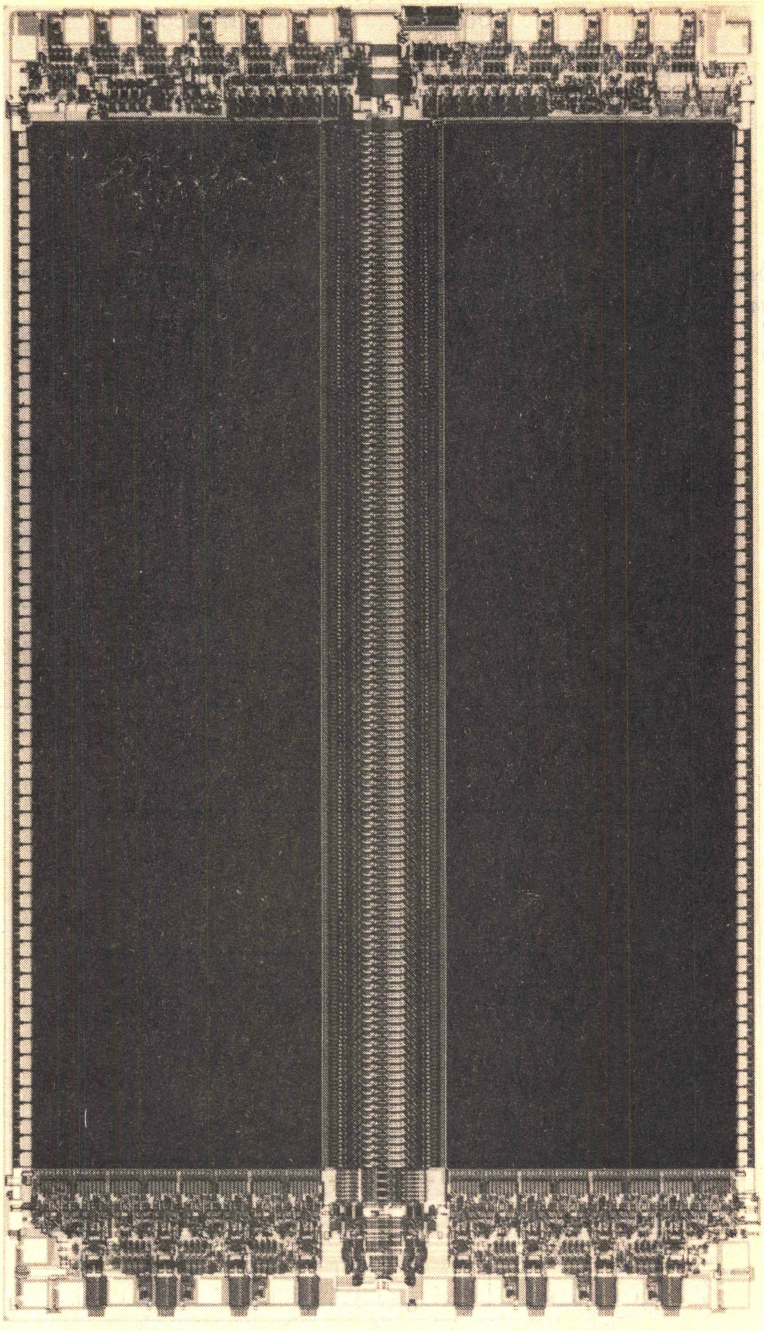
210473-19

Bit Map



210473-20

27512/27513 Bit Map



210473-21

27512/27513 Die Photograph

27010 Row Decoding

Row	A_3	A_4	A_{12}	A_{15}	A_{16}	A_{14}	A_{11}	A_{13}	A_9	A_8
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

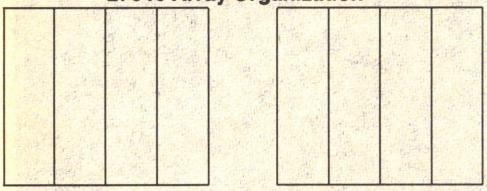
X Decode: A_{16}, A_{15}, A_{14}, A_{12}, A_{11}, A_4 and A_3
R Decode: A_{13}, A_9 and A_8

27010 Column Decoding

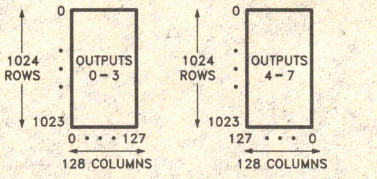
Column	A_2	A_1	A_7	A_6	A_5	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_7, A_6 and A_5
Z Decode: A_{10}

27010 Array Organization



27010 Row & Column Layout



210473-27

Figure 5. 27010 Bit Map

27011 Row Decoding

Row	$\overline{D_0}$	$\overline{D_1}$	A_6	A_7	A_{12}	A_8	$\overline{D_2}$	A_9	A_{13}	A_{11}
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	1	0
•					•					
•					•					
•					•					
1023	1	1	1	1	1	1	1	1	1	1

X Decode: D_2, D_1, D_0, A_{12}, A_8, A_7 and A_6
R Decode: A_{13}, A_{11} and A_9

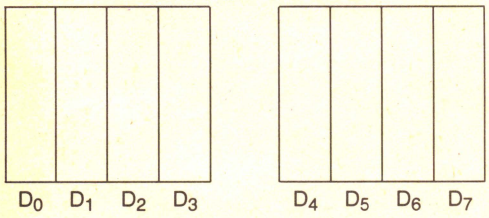
NOTE:
$\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ are complemented page-select write input data.
e.g., $\overline{D_2}$, $\overline{D_1}$, $\overline{D_0}$ = 000 corresponds to page data 07H.

27011 Column Decoding

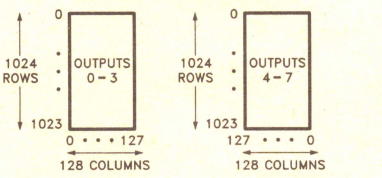
Column	A_2	A_1	A_5	A_4	A_3	A_{10}	A_0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
•				•			
•				•			
•				•			
127	1	1	1	1	1	1	1

W Decode: A_2, A_1 and A_0
Y Decode: A_5, A_4 and A_3
Z Decode: A_{10}

27011 Array Organization

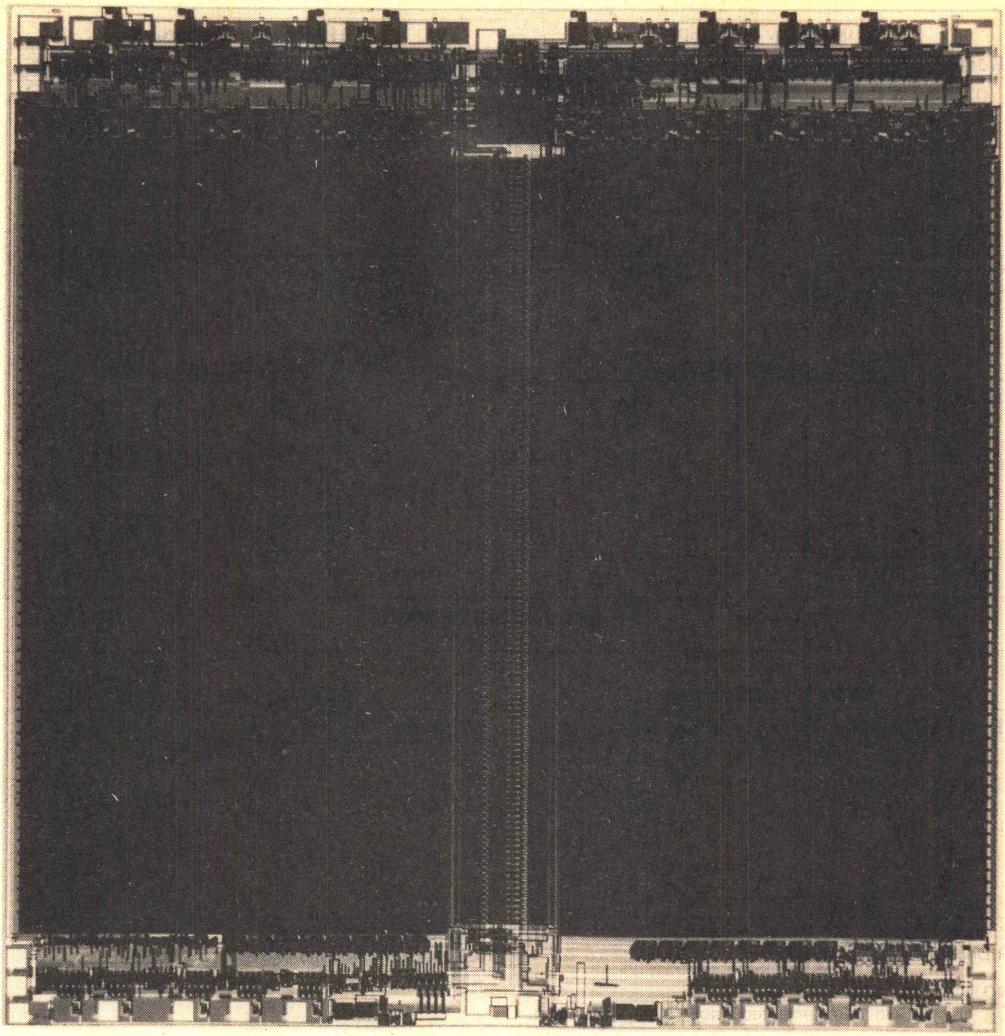


27011 Row and Column Layout



210473-28

Figure 6. 27011 Bit Map



210473-29

27010/27011 Die Photograph

27210 Row Decoding

Row	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_{15}	A_{14}	A_{13}
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	1	0
•					•				
•					•				
•					•				
511	1	1	1	1	1	1	1	1	1

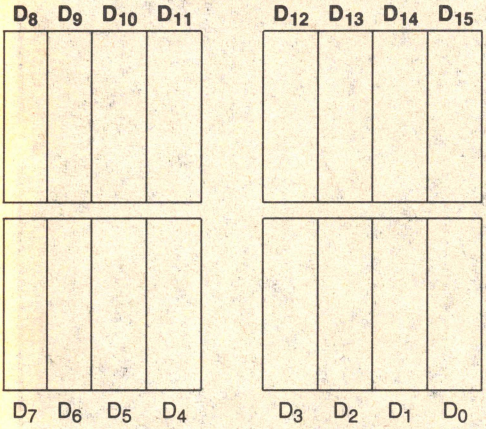
R Decode: A_{15}, A_{14} and A_{13}
X Decode: A_{12}, A_{11}, A_{10}, A_9, A_8 and A_7

27210 Column Decoding

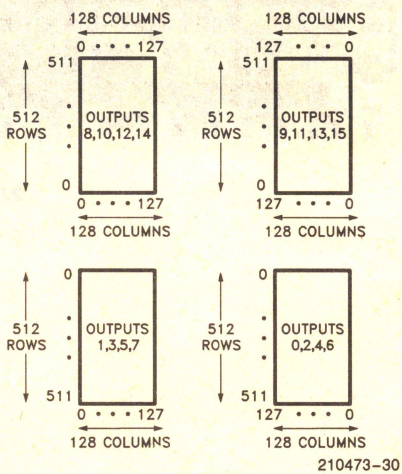
Y Decode	A_3	A_2	A_1	A_0	W Decode	A_6	A_5	A_4
Y_0	0	0	0	0	W_0	0	0	0
Y_1	0	0	0	1	W_1	0	0	1
Y_2	0	0	1	0	W_2	0	1	0
•		•			•		•	
•		•			•		•	
•		•			•		•	
Y_{15}	1	1	1	1	W_7	1	1	1

Column	W		Y	Column	W		Y
0	W_0	>	Y_{15}	64	W_4	>	Y_{15}
1	W_1			65	W_5		
2	W_1	>	Y_{14}	66	W_5	>	Y_{14}
3	W_0			67	W_4		
•	•		•	•	•		•
•	•		•	•	•		•
•	•		•	•	•		•
30	W_1	>	Y_0	94	W_5	>	Y_0
31	W_0			95	W_4		
32	W_2	>	Y_0	96	W_6	>	Y_0
33	W_3			97	W_7		
34	W_3	>	Y_1	98	W_7	>	Y_1
35	W_2			99	W_6		
•	•		•	•	•		•
•	•		•	•	•		•
•	•		•	•	•		•
62	W_3	>	Y_{15}	126	W_7	>	Y_{15}
63	W_2			127	W_6		

27210 Array Organization

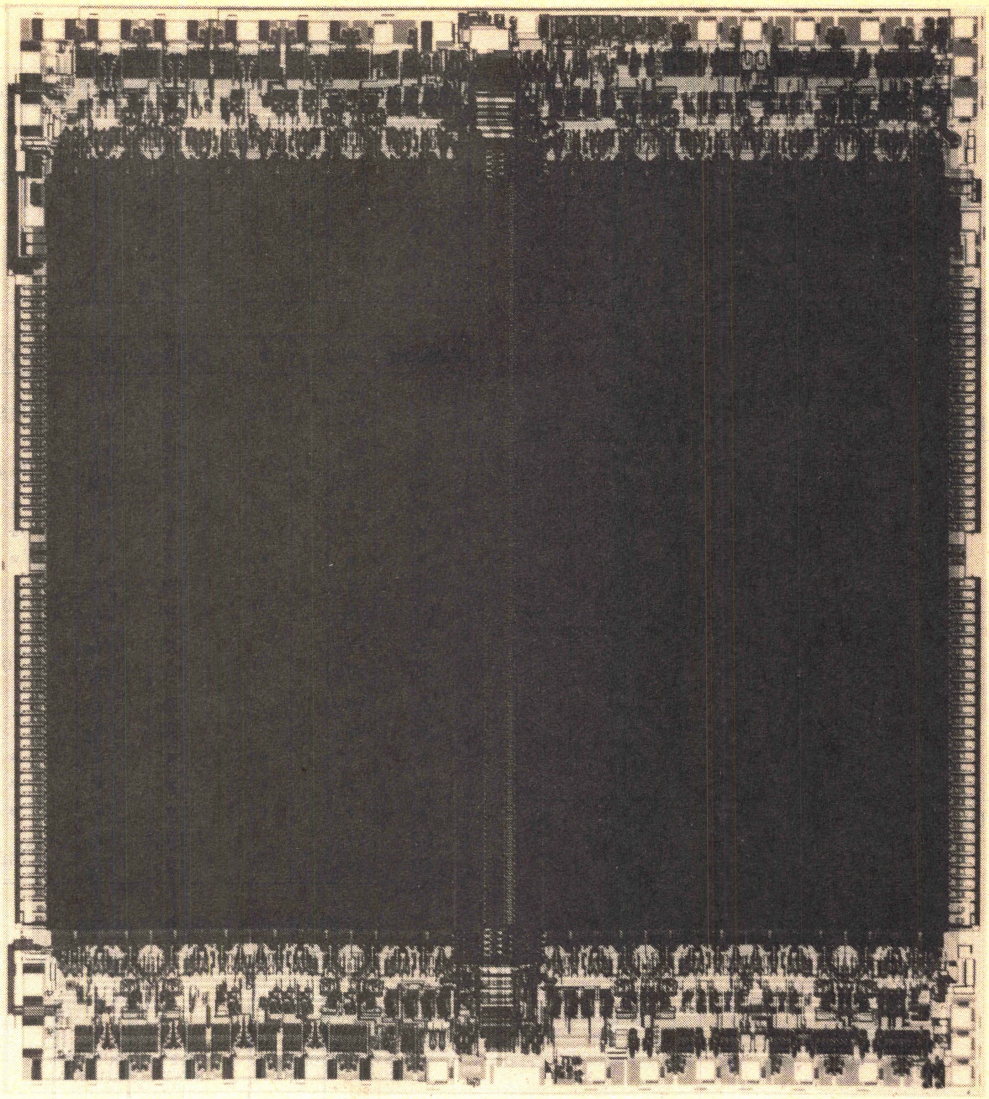


27210 Row & Column Layout



210473-30

Figure 9. 27210 Bit Map



210473-31

27010 Die Photograph

intel

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EPROMs Adapt To Emerging Developments In Technologies, Configurations, Packages

BY
LAWRENCE PALLEY
EPROM MARKETING MANAGER
INTEL CORPORATION

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EPROMs Adapt To Emerging Developments In Technologies, Configurations, Packages

CMOS EPROMs Evolve To Meet Growing System Needs

By Lawrence Palley

Changes in digital-system-memory architectures and production methodologies are driving changes in the traditional EPROM market. An accelerated transition to systems with easily run, built-in feature sets (programs) requires denser components for compactness. At the same time, an increasing focus on "design for manufacturability" requires components with lower costs and high reliability. In both cases, alternatives are being derived with EPROMs that are now evolving to meet a growing variety of system needs. This evolution is exemplified by CMOS technologies, plastic packaging and page-addressed design configurations.

This author is EPROM Marketing Manager at Intel Corp., Folsom, California.

The use of digital computing is now extending beyond those with engineering or technical backgrounds. Today, the power of data processing must be accessible to businessmen, consumers, and non-electronic technicians. Quick and reliable execution of canned application programs is a must. Instructions for electronic-system operation must be readily accessible and the barrier of working with the machine reduced.

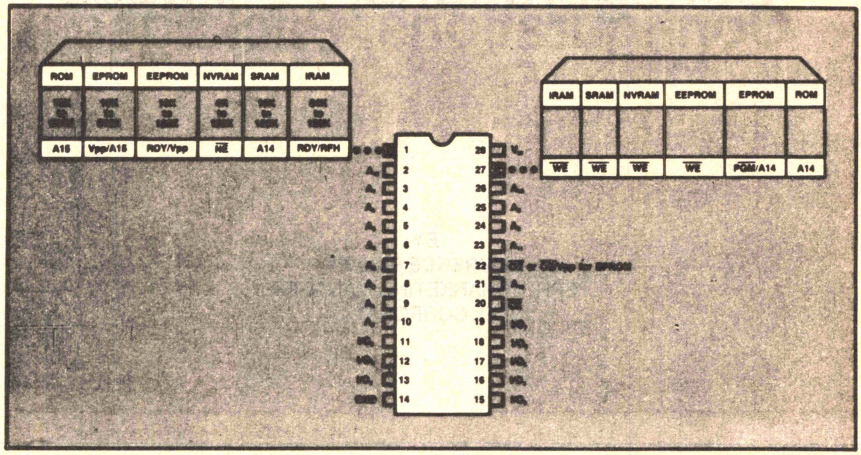
An analogy can be made with the automobile. Early cars were difficult to operate. Users had to understand the operation of the engine and drive mechanics. They had to go through extensive start-up procedures (open the choke, turn the crank, etc.). And when the automobile frequently broke down, the user generally had to know how to fix it.

Today, cars include many "user-friendly" features-automatic transmissions, electronic ignition, etc., which make them simple to use. In general, drivers have little interest in the automobile's inner engine and mechanical workings. They want to use the car for its benefit (getting around town) and expect it to accomplish its purpose reliably.

Computing Arena

A similar situation has occurred in the computing arena. Large amounts of software have been incorporated integrally into digital equipment. Such integral software now includes bootstrap programs, operting systems, diagnostics, instructions on use, and even dedicated applications. Users need no longer be trained on the inner workings of the computer, but rather focus on obtaining the desired output. All the operations are made simpler by the software.

Various methods have been used to incorporate this software into systems, but the most common has been an extension of the concept of downloading disk-based software to RAM. More recently, the placement of this software in non-volatile semiconductor memories has increased (converting software into firmware).



The universal memory site pin configuration enables designers to mix and match ROMs, EPROMs, EEPROMs, NVRAMs, IRAMs and static RAMs by simply changing jumper connections.

The firmware alternative offers substantial benefits to both users and manufacturers. To run a program the user can use dedicated keys on the keyboard. The microprocessor then directly accesses the program, and does not have to encounter problems such as lost or erased program disks.

Aiding The Manufacturer

To the manufacturer, adding diagnostics and documentation to the firmware enables quick debugging of system problems and reduces customer questions on operation. The addition of applications software also enables the manufacturer to sell a complete, integrated system, specifically tailored to his customer base.

One additional, and less obvious advantage to the manufacturer is the added level of software security maintained by firmware. Not only is the software further removed from illegal copying, but it is also removed from the inadvertent user, one who could erase or alter it into an unusable form.

Firmware-intensive systems, with ROM or EPROM, have been extensively used in applications with realtime-processing needs. Instruments, telecommunications equipment, and industrial controllers use large amounts of firmware to perform their various tasks. Additionally, they incorporate diagnostics and menu-driven operator instructions to simplify operation.

One of the older limitations on adding firmware to a system was its usage of the processor's memory space. Earlier 8-bit processors were only capable of addressing 64 kbytes of program or data directly. A 32-kbyte applications program would use half of this area. Therefore, the best use of this area was to implement it with RAM and rely on disk memory for the firmware. Programs would then be swapped in and out of this memory space.

New processors, using 16-bit internal architectures, are able to address much larger memory spaces. Typically, these processors address upward of 1 Mbyte directly. A fixed 256-kbyte non-volatile memory system, using four 27512 EPROMs for instance, would leave more than enough RAM memory for directly accessible data storage.

An alternative for microcontrollers and 8-bit microprocessors is to use a page-addressed system such as that designed into the 27513 EPROM. This device effectively fits 64 kbytes of firmware into a 16-kbyte address space. Processors and controllers with 64-kbyte address limits can expand a 16-kbyte built-in feature set (stored in a 27128 EPROM) to 64 kbytes, without hardware modification.

The ease of hardware upgrade, from 27128 to 27513, is made possible by the continuing use of the 28-pin universal-memory site. This site enables designers to mix and match their choice of ROMs, EPROMs, NVRAMs, iRAMs, and static RAMs by changing jumper considerations. The universal socket has provisions for address, data, and function pins on all these devices. Memory sizes up to 512 kbits (or 64 kbytes) are provided for with 16 address pins. Read access to the memories is simplified using the site's two-line control architecture.

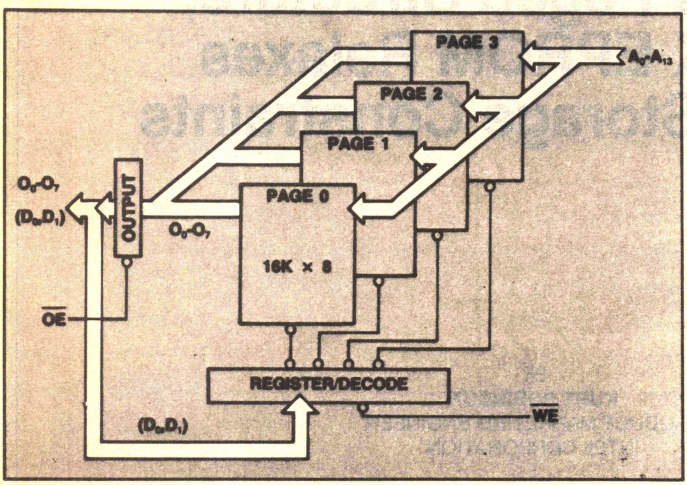
The universal-memory site offers flexibility to designers. A memory board, designed with these sockets, can be used on multiple systems.

High-Volume Production

A major change for EPROMs has been their move from prototyping memories to memories used in production. Their overall cost effectiveness vs. ROM alternatives has increased as the technology has matured. Plastic-packaging technology for EPROMs promises to continue this transition.

Plastic is an advantage for high-volume production where auto-insertion equipment is used. The plastic package will not chip or crack. The windowless package also means that no covering must be applied to prevent erasure when exposed to ambient ultraviolet light.

The plastic-production EPROM (sometimes called OTP) is shipped in an unprogrammed state so that it can be programmed during the actual production run. It offers the same advantages of a windowed EPROM in production-inventory flexibility, fast production startup and reduced ROM obsolescence risk. It also comes at a reduced cost from the windowed version.



Intel's 27513 EPROM incorporates a page-addressed system that puts 64 kbytes of firmware into a 16-kbyte address space without hardware modification.

CMOS Invasion

The traditional CMOS applications in low-power or portable systems can now be designed with EPROMs. Intel's 27C64 requires less than a third of the active power of NMOS EPROMs and an order of magnitude less power when in the standby mode. The use of the CMOS EPROMs eliminates the need for complex and costly power-switching circuitry, as needed with NMOS EPROMs in these applications.

The high voltages (higher than V_{cc}) used to program EPROMs require CMOS designs to pay special attention to latch-up characteristics. Intel's CHMOS-EPROM fabrication process uses EPI processing and guard-ring structures to reduce latch-up susceptibility to high voltages and input/output noise spikes. Specifications guarantee latch-up immunity to more than 1-V margins around all power supply voltages, and currents in excess of 100 mA. ●

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With Its Paged Structure, A 512K EPROM Relaxes System Storage Constraints

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With its paged structure, a 512k EPROM relaxes system storage constraints

The limits imposed by the addressing range of today's 8-bit microprocessors are removed by a page-addressed EPROM that acts like four 128-kbit chips.

Inventive system designers know that advanced software features could prolong the usefulness of their 8-bit microprocessor-based systems. Though the idea is an attractive one, adding those changes to program memory would often strain the 64-kbyte addressing range of the microprocessor.

Today's 512-kbit EPROMs have the higher capacity but would consume the entire address space of the 8-bit machines. A new twist—a 512-kbit EPROM organized as four 16-kbyte pages—quadruples the program storage available to an 8-bit system. Indeed, 16-bit systems can benefit from using it.

As important, the entire chip looks to the system like a 128-kbit EPROM, which it can easily replace. Upgrading a system in this way entails little or no software modification, while building a new one with the device reduces circuit complexity and permits the use of less costly and more mature system components.

The byte-wide 27513 is a paged version of the 27512 512-kbit EPROM. Only 14 of its 16 address bits are needed to access it s full 64 kbytes, since it reserves on-chip latches for the two highest-order bits. Its 16-kbyte page size satisfies a variety of system requirements. A smaller page would entail too frequent page changes. A larger one would leave too little room for addressing RAM—which in a reprepresentative 8085-based system requires 48 kbytes of the microprocessor's 64-kbyte address space (Fig. 1). In fact, the microprocessor treats the EPROM as if it were a fourth bank of 16-kbyte RAM and selects it by writing to a 2-to-4 decoder.

Kurt Robinson, Intel Corp.

Kurt Robinson has served for five years with Intel's nonvolatile memory division, which recently moved to Folsom, Calif. Starting as an EPROM product engineer, he later joined the programmable memory marketing group as an applications engineer. Subsequently he advanced to senior product marketing engineer. His BSEE is from Cornell and his MBA from the University of Santa Clara.

The main difference

The primary operational difference between the paged 512-kbit device and linearly addressed EPROMs, including the 27512, lies in page selection. First the microprocessor sends the EPROM 2-bit page data over the lowest-order data bits, D_0 and D_1. Next it enables the memory by setting the Chip Enable ($\overline{CE}$) line low via the 2-to-4 decoder. Then it brings the Write Enable line ($\overline{WE}$) low also, thus clocking the page data into the chip's 2-bit address latch. Thereafter the newly selected 16-kbyte page can be accessed during conventional EPROM read cycles. The address inputs during page selection are in a "don't care" state.

During power-up, the EPROM automatically resets itself to page 0 as if the data 00 were being written into D_1 and D_0. A circuit for clearing the page latch remains active until V_{CC} exceeds

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4 V. Above that level, system control signals remain sufficiently stable to avoid inadvertent page selection.

The 4-V level is also low enough to prevent a low-going power-supply glitch from accidentally clearing the page latch. The worst-case voltage for V_{CC} is 4.5 V. The 4 V that clears the page also sets a 500-mV noise margin against supply undershoot, without presenting any danger of resetting the current page to 0.

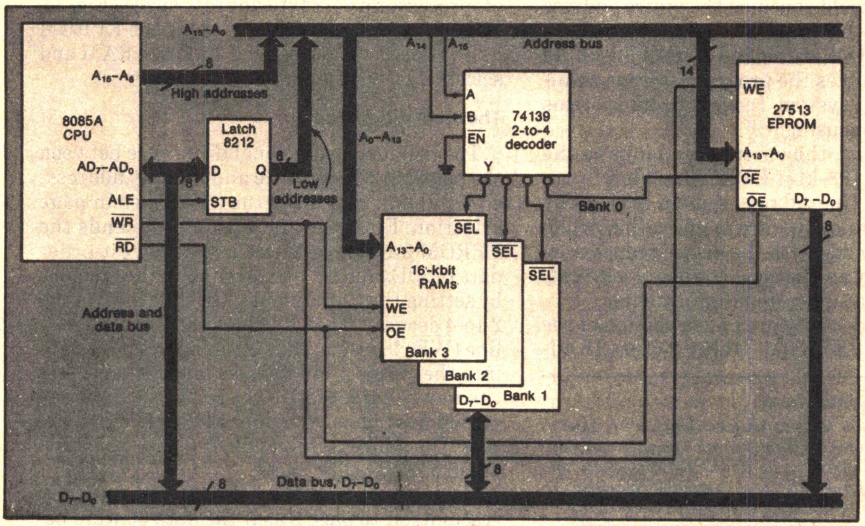
Programming the 27513 utilizes a proprietary algorithm supplied with all 12.5-V HMOS EPROMs, including the 27512. This algorithm creates 1-ms programming pulses until the byte has been verified, after which it gives a programming overpulse margin of three times the number of initial pulses. A page-select write operation is included at the start of the program and at every subsequent page boundary thereafter. (Fig. 2).

The chip's programming voltage, V_{PP}, is multiplexed with the Output Enable line ($\overline{OE}$), and the combined line ($\overline{OE}/V_{PP}$) is brought to 12.5 V for programming and to a TTL low level for verification, as in a normal read. If the chip is disabled ($\overline{CE}$ goes to a TTL high) while $\overline{OE}/V_{PP}$ is at 12.5 V, programming stops.

After each page has been programmed, it undergoes a page-selection write operation, with the write parameters tested in a manner similar to that for static RAMs. Because the chip's page latch is a write-only register, the programmed data is not read back. Instead the memory must be checked for a successful page change. Unique data must appear in at least one physical address on each page; checking that address on each page and finding the unique data confirms that the page programming was successful. Though testing of the write cycle entails reading from specific addresses, an actual write operation is independent of the address inputs.

Simple to substitute

The EPROM chip has a socket footprint almost identical to that of a 128k EPROM, meaning that it can easily be substituted for the smaller device in an existing system. However, some changes in board design are required. For example, the 512k EPROM assigns pin 27 to the Write Enable control signal, as in the JEDEC standard for byte-wide RAMs. In contrast, a



1. An 8085-based system equipped with 48 kbytes of RAM has room only for a 16-kbyte block of EPROM. But the 27513 EPROM packs four such blocks into the space previously occupied by a 128-kbit part. The EPROM resides in memory space from 0000_{16} to $3FFF_{16}$; the RAM occupies addresses 4000_{16} to $FFFF_{16}$.

128k EPROM's pin 27 is set for the program function and is tied to 5 V or V_{CC}. The origin of the Write Enable signal of the 27513 varies, since the chip encounters situations in which code and data must share the same memory map but are selected independently through dedicated selection lines or decoded status signals from the processor.

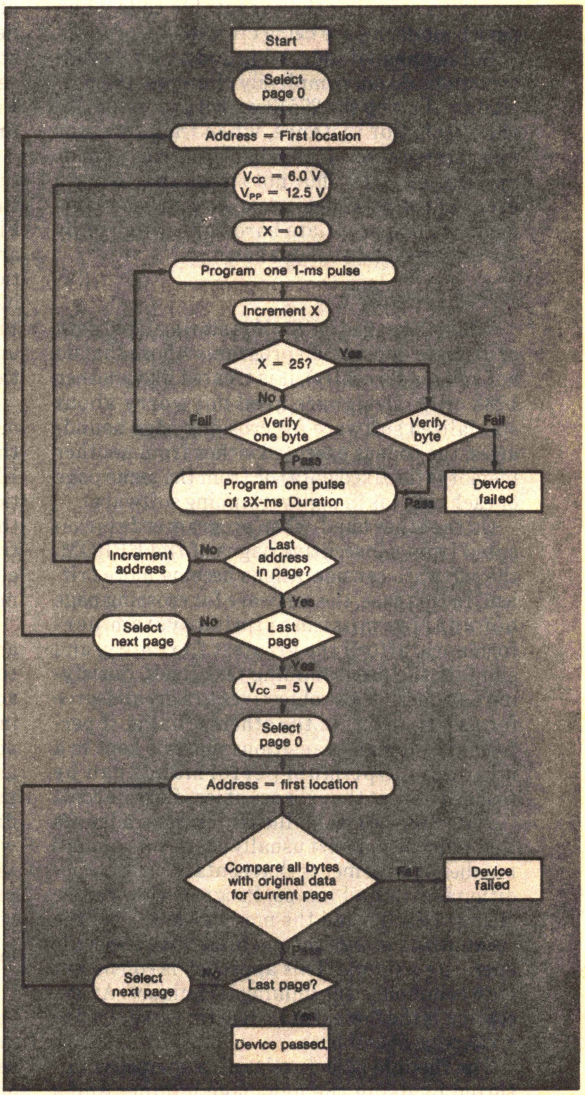
Upgrading a circuit to the 512k EPROM from one designed for a 128k EPROM is dramatically simplified if the socket has been laid out according to the so-called universal site for byte-wide memories. That arrangement brings address and control lines close to the socket, so that different configurations can be selected through jumpers. Designers can access V_{CC} (for tying the program pin of 64k and 128k EPROMs to 5 V) and $\overline{WE}$ (for byte-wide RAMs) through the universal pin 27. Thus if the socket follows this standard arrangement, the 27513 can be substituted for lower-capacity devices by changing just one jumper.

Superior 16-bit control, too

The paged EPROM can solve the limited addressing range of both 8-bit and 16-bit microprocessor-based systems. That holds true especially for firmware-intensive jobs that tax the 16-bit chip's seemingly adequate addressing range of a megabyte or more assigned to EPROM.

For example, a system tackling frequent transactions can actually eat up most of its total memory address space, which can reach about 16 Mbytes. It may use high-order address lines for specialized I/O and still have enough room for a megabyte each of RAM and EPROM. The code changes required to modify the extremely complex functions of transaction processing might cause even the megabyte of EPROM to overflow. With the 27513, code can be chopped to more manageable levels or rearranged into different memory configurations.

The 512k chip is not suited to all 16-bit systems. Indeed, executing code in the consecutive pages of the segmented chip poses a real challenge to the software programmer of, say, the 80186, which has internal segmented addresses. A high-performance processor like that also prefetches several instructions, making it difficult to know which page in the paged 512k chip



2. A proprietary programming algorithm performs a page-selection write operation at the end of each page in the 27513. The algorithm generates 1-ms pulses until 8 bits have been verified; an overpulse that lasts three times longer than the number of initial pulses gives an extra program margin.

would be sourcing the executable code when page boundaries are being crossed.

But segmented addressing and prefetched instructions do not completely eliminate the possibility of using the 27513 with a processor like the 80186. For instance, when the processor must access several large banks of fixed data or application code—but not simultaneously—a group of these 512k chips can be set to the same page by an appropriate hardware switch or by operating-system commands.

Software concerns

When the paged EPROM is storing fixed data or discrete application programs (those that do not run concurrently), it is treated like another 128k chip. Designers need not worry about specialized software for crossing page boundaries; the code is executed either from another memory (for fixed data) or from the same page of each chip (as in nonoverlapping software).

On the other hand, when program code is executed from consecutive pages of the EPROM, the software considerations become more critical. In this case, the software for crossing page boundaries must maximize system performance, afford the greatest flexibility, and simplify the programming task itself. Satisfying any one of those objectives to a great degree forms a trade-off in the others. That is, if performance jumps, transitions must be kept to a minimum. Optimum performance can be reached only at the expense of less flexible code.

A flexible program illustrates the trade-offs that must be made. It usually comprises a small number of statements that contain several conditional calls and jumps. Program flow can be changed easily, and the modular nature of the subroutines makes the modification of specific operations simple. This approach is consistent with common programming techniques. An exception is the few extra instructions required to cross page boundaries.

The flexible structure's call sequence is initiated by using the new page number and a lookup table, called offset, for the subroutine address (Fig. 3a). The command Call is issued and the new page selected. However, the current page number remains unchanged. Next, the subroutine Call Address is obtained from the new-page lookup table, as indexed by the offset table. After a jump to Call Address in the new page, a return is made by jumping to the instruction RETR. The current page number is read, and the chip is reset to the previous page. Finally the program goes back to Return Address in the original page.

If the program branches to a new section of the program and there is no need to return to the previous page, a jump sequence begins. First, the offset table and the new page number are loaded, and the program moves to instruction JUMPR. The new page is now selected and its number stored in the current page location. The jump address is found in the new page lookup table, based on the offset table. A jump is then made to Jump Address in the new page.

Subroutine lookup tables are essential to this most advanced method of page selection, one that involves storing the lookup tables in the EPROM chip itself and reserving a small section of RAM for page-selection code. Although the technique demands more code for the page transitions, the overall amount is reduced by eliminating redundant instructions for common subroutines.

The look-up tables contain the page number and the offset address from which a given routine is called. Within the page containing the actual subroutine code, another lookup table, indexed by the offset value, holds the physical address of the routine. Thus the page number and offset information contained in the other pages remain constant, but the physical address of the actual subroutine can be relocated within its page, even if the code changes. The instructions for handling the page transitions are preloaded into a reserved section of RAM when the system is initialized.

Interrupts anywhere

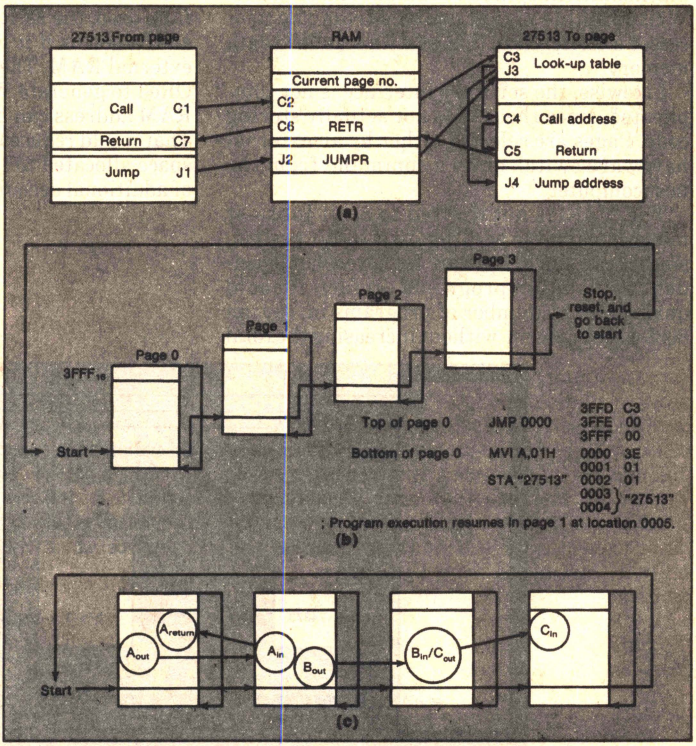
Interrupt routines can be executed from any page of the EPROM if the current page information is retained. After the interrupt has been serviced, the EPROM is reset to the page and address that were current when the interrupt occurred. Here again, the instructions for handling the page transitions and for calling the interrupt subroutine are preloaded into reserved RAM.

As with the flexible programming structure, designers are typically trying to make their

program code more efficient by squeezing the greatest number of operations into each instruction. Those are critical concerns for systems that place program code in standard 128-kbit EPROMs, but they become much more relaxed when seen in terms of the 27513's fourfold increase in capacity. Some designers might choose straight-line programming where jumps and calls are avoided. The 27513 excels in that situation, i.e. where flexibility and compactness of code are sacrificed for an overall increase in execution speed (Fig. 3b). A true straight-line program contains no calls or jumps; the code for any repeated function is replicated each time.

Though a program that uses no branching may appear impractical, another approach that places all subroutines in the same page as the call and jump commands that refer to them is not impractical. With that technique, frequent operations are stored on every page—but only once. In either case, page transitions occur only at the end of a page or when the program is jumping back to the beginning. Small instruction sets at the start and end of each page actually shift the pages.

If the page transitions occur frequently but at relatively few points in the program, another scheme—one of moderate complexity—duplicates the set of instructions at the straight-line



3. The program structure of the 27513 can take three forms. A flexible program requires more code for page transitions and eliminates redundant instructions for frequently called subroutines (a). The straight-line approach affords the fastest performance (b). A modification of that structure maintains the speed but adds branching code to deal with jumps between page boundaries (c).

program's page boundaries. In that manner, page transitions occur through dedicated portals of code (Fig. 3c).

Enlarging fixed storage

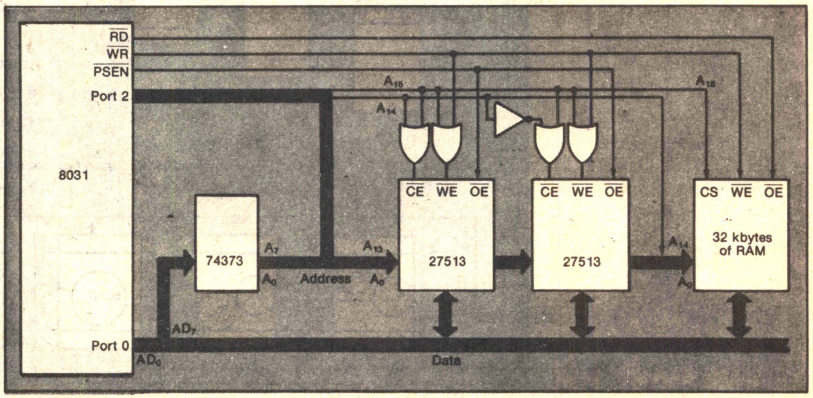
Though the 512k chip will undoubtedly be called to duty for code-expanding missions in popular 8-bit processors, its hardware interface proves equally suitable for applications requiring more storage of fixed data. Suppose that the chip is substituting for several 128-kbit EPROMs in an 8051-based dot-matrix printer. The chip itself provides enough extra storage space that designers can add three new character sets (for example, scientific marks, mathematical symbols, custom shapes). The Write Enable signal derives from the processor's Write/Read line, as with standard data memory.

Likewise, the software interface is not complicated, since the chip is not actually storing code. Pages are selected either by an external hardware switch or by a command from the host computer.

The 27513 is not limited to 8-bit jobs—it makes a valuable addition to a 16-bit system, since it can store firmware for several independent application programs. In fact, it could quadruple the number of programs in, say, an 8088-based system, without increasing the total amount of physical address space allocated to EPROM. And because the programs are not used simultaneously, the system interface is simple. Each program is selected in much the same manner as for the 8051 character-set storage application.

Even a complex chore, such as storing firmware-intensive 8031 applications, need not be a formidable task with the chip (Fig. 4). The 8031 has a special $\overline{\text{PSEN}}$ (Program Store Enable) signal to enable the output of external program memory. Because data cannot be written to the standard program memory, the designer must make sure that the 27513 is subjected to the necessary page-selection write operation.

If the external data memory of the 8031 is not fully used, the EPROM chip's page latch can be addressed as if it were a lower-order bank of external RAM. The A_{15} and $\overline{\text{WR}}$ signals can be ORed to generate $\overline{\text{WE}}$; alternatively, a specific RAM address can be decoded to generate $\overline{\text{WE}}$. That would reduce the amount of RAM address space allocated to the 27513 but at the expense of additional decoding circuitry. □



4. Although some processors do not make a perfect match for the 27513, provision can be made for the EPROM's requirements. Here the memory's page latch is addressed as if the chip were a low-order bank of external RAM. ORing the processor's A_{15} and $\overline{\text{WR}}$ signals generates the 27513's $\overline{\text{WE}}$ signal; line A_{15} determines whether the RAM or EPROMs are selected. Chip-enable signals for the 27513s are decoded from lines A_{14} and A_{15}.

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AR-406

Use simple circuits, algorithms to program 512k-bit EPROMs

Simple interface circuitry and programming algorithms let you program the 27512 and 27513 512k-bit EPROMs rapidly and reliably.

Kurt Robinson, *Intel Corp*

Although the latest high-capacity, 512k-bit EPROMs are a logical extension of previous, smaller-capacity EPROMs, you'll need new hardware and software to program them, because the chip-select and programming lines are slightly more complex than those of the earlier devices. You can use some simple interface circuitry and programming algorithms to program 512k-bit 27512 and 27513 EPROMs rapidly and reliably.

To program the 512k-bit EPROMs, you need to use a synthesis of the techniques developed for lower-capacity EPROMs. The 512k-bit EPROMs' programming modes are identical to those of 32k-bit EPROMs, and their algorithms are compatible with those of 256k-bit EPROMs. Further, the 512k-bit EPROMs' multiplexed programming-supply/output-enable pin makes their read and program-verify modes identical, because you must bring $\overline{OE}/V_{PP}$ to a TTL low to enable data output.

Note that because of its page-addressed scheme, the 27513 has slightly different programming requirements from those of the 27512: When you program the 27513, you must select a new page at each 16k-byte boundary. **Table 1** gives the operating modes for 512k-bit EPROMs, including the 27513's page-select write mode.

TABLE 1—512k-BIT-EPROM OPERATING MODES

PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	$\overline{WE}$ (27)	V_{CC} (28)	OUTPUTS (13, 15-19)	INPUT/OUTPUTS (11, 12)
READ	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	V_{IH}	V_{CC}	HIGH Z	HIGH Z
STANDBY	V_{IH}	X	X	V_{CC}	HIGH Z	HIGH Z
INTELLIGENT PROGRAMMING	V_{IL}	V_{PP}	V_{IH}	V_{CC}	D_{IN}	D_{IN}
PROGRAM INHIBIT	V_{IH}	V_{PP}	V_{IH}	V_{CC}	HIGH Z	HIGH Z
PAGE-SELECT WRITE*	V_{IL}	V_{IH}	V_{IL}		HIGH Z	PAGE D_{IN}

NOTES:
X CAN BE V_{IH} OR V_{IL}
ADDRESSES ARE DON'T CARE FOR PAGE SELECTION.
*PAGE-ADDRESSED DEVICE (27513) ONLY

PAGE D_{IN} PAGE-SELECTION DATA

INPUT/OUTPUT (PIN)	D_1/O_1 (12)	D_0/O_0 (11)
PAGE SELECTION		
SELECT PAGE 0	V_{IL}	V_{IL}
SELECT PAGE 1	V_{IL}	V_{IH}
SELECT PAGE 2	V_{IH}	V_{IL}
SELECT PAGE 3	V_{IH}	V_{IH}

As with earlier large-capacity EPROMs, the 512k-bit EPROMs' adaptive-programming algorithms require you to raise the standard 5V supply (V_{CC}) to 6V during programming and to supply a higher voltage to the programming pin. This higher supply voltage ensures

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The 512k-bit EPROMs' programming modes are identical to those of 32k-bit EPROMs.

that the EPROM will have an adequate programming margin.

Of course, most systems provide EPROM V_{CC} power through the 5V supply common to all components. Because other components are typically not guaranteed to operate at higher voltages, you'll need to implement an isolation circuit for EPROM V_{CC} during EPROM programming. Such a circuit is similar to the circuit required to switch programming-supply pins to high voltage.

The most important difference between programming 512k-bit EPROMs and programming other types of EPROMs is that the V_{PP} and $\overline{OE}$ functions are multiplexed in the 512k-bit devices. For example, the $\overline{OE}/V_{PP}$ lines bused to 512k-bit EPROMs select one of three levels: high voltage (for programming), TTL high, and TTL low (both during read operations). In contrast, V_{PP}-switching circuits for programming 256k-bit EPROMs select one of two constant, dc levels: either V_{CC} (in read modes) or high voltage (during programming). The circuit in **Fig 1** accomplishes the switching task for 512k-bit EPROMs.

Fig 2 shows 512k-bit EPROM-programming waveforms, including appropriate control signals, for the switching circuitry. Although the software that drives these signals is fairly straightforward, the sequence in

Page-addressing mandates EPROM-specific software

Page-addressing creates problems in writing the software that you burn into the 512k-bit 27513 EPROM. Fortunately, you can solve these problems by adding simple instructions to your programs. These assembler macroinstructions (macros) allow continuous code execution across page boundaries and simplify programs that exceed the 16k-byte page length.

Crossing boundaries

There are three basic applications for a page-addressed EPROM. In the simplest of these applications, a 27513 directly replaces 128k-bit EPROMs with a fourfold expansion of memory pages. The operating system treats each page as if it were a standard 128k-bit EPROM. Because the operating system uses the code contained in different pages independently, it needs no page transitions during execution of the chosen application program. Consequently, no special page-handling instructions need to be incorporated into the application code.

The other two schemes are page-handling schemes that involve executing a single program across page boundaries. The simplest boundary crossings occur when 8-bit μPs have code requirements that exceed their 64k-byte addressing ranges. A 16k-byte EPROM page allows you to transcend the 64k-byte boundary, while still leaving room for other types of memory.

Fourfold increase

Because the 27513 has four times the capacity of a standard 128k-bit EPROM, you can use a different program structure with the 27513. The abundant code space allows you to unfold the program from a typical structured program to a purely straight-line organization. With this approach, you duplicate subroutines everywhere they are needed in the main program flow, eliminating all jumps and calls—especially those from one page to another. The resulting straight-line flow offers the highest performance. Code for handling page transitions occurs only at page boundaries, and the program loops back to the beginning when it reaches the end of the fourth page. A generalized 27513 structure for the page-handling code is

- Program execution begins a few locations up from the starting address of the page.
- The last instruction in each page is a jump to the beginning of that page.
- The code at the beginning of the page instructs the processor to select a new page.
- The next instruction executes from the next physical address (but actually from the next page). This address is the same physical address as the starting location in the previous page.

The third paging method pro-

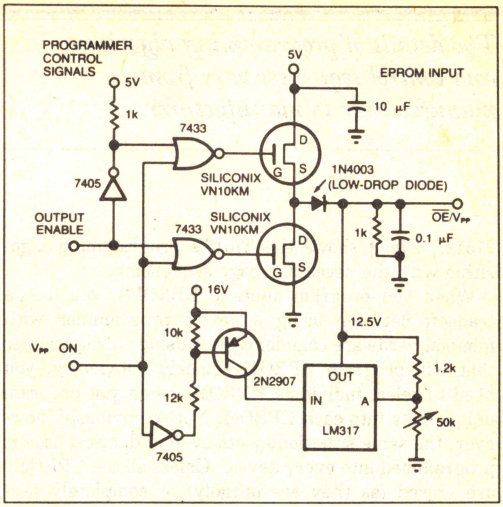


*Fig 1—**This level-selecting circuit provides** the fast, clean switching you need to program and verify 512k-bit EPROMs.*

which the signals are applied depends on the programming algorithm the manufacturer specifies.

For example, Intel's programming algorithm initially tracks the number of 1-msec pulses required for the first successful verification. The algorithm then requires that you multiply the interval by 3 to yield a single overpulse. This overpulse boosts the memory cells in that byte to the highest programming margin the chip can withstand without degradation.

Except for some extra steps that handle page transitions, the programming algorithm for the page-addressed EPROM (the 27513) is identical to the algorithm for the continuously addressed EPROM (the

duces the most flexible structure, but its complexity creates the greatest need for standard assembler macros for generating the page-changing code. This approach is most consistent with standard structured-programming techniques. Characteristics of structured programs include modularized routines, numerous jumps and calls, and ready servicing of interrupts. You'll need software tools to generate special code whenever a jump or call involves crossing page boundaries. The tools also must relocate the physical addresses and associated memory pages when the program is modified.

In this approach, the foundation for structured programs consists of a look-up table, three subroutines, and a register or stack location for tracking the current page. The look-up table holds the page number and the physical address (within the selected page) for the routine being called or jumped to. The three subroutines, duplicated in each page (or loaded into RAM), perform jumps, calls, and returns from calls. Generalized descriptions for these subroutines are

- *Call*—You call this routine instead of calling a subroutine directly. The routine requires a look-up-table pointer associated with the subroutine you want to jump to. Because the program must return to the original page, *Call* stores the current page in a current-page register or RAM location. *Call* gets the page number and relative physical address of the called routine and issues commands to change to the new page. *Call*'s remaining instructions are executed from a new page (which implies that *Call* occupies identical physical addresses in each page). Finally, *Call* jumps to the physical address of the called routine.
- *Jump* is exactly like *Call* except that you unconditionally jump to it instead of calling it. Before jumping to the routine's physical address within the new page, *Jump* updates the current page register (or stack location) to the page number of the new page, which you just selected.
- *Return*—You jump to this routine instead of simply executing a return instruction to return from a subroutine call. *Return* obtains the previous page number from the current-page register. (Note that the current-page information was not changed when the *Call* routine executed.) *Return* issues instructions to reselect the previous page. Finally, because you called the *Call* routine initially, *Return* executes a standard return command and resets the program counter to the proper return address.

The details of programming algorithms and control sequences vary from manufacturer to manufacturer.

27512). **Fig 3** shows the 27513's programming algorithm with the necessary page sequencing.

When you program multiple EPROMs, you face a tradeoff between using a device programmer with minimal hardware complexity and using a programmer that will program EPROMs quickly. Obviously, you need to select individual EPROMs when you program unique data into each EPROM. Not so obviously, however, the same situation exists even if identical data is programmed into every device. Unless all the EPROMs are erased (as they are initially) or completely programmed (as they are in the end), they will produce different data during the intermediate stages of adaptive-programming processes. When you read from more than one device at the intermediate stages of adaptive programming, the partially programmed EPROMs will contend for the data bus.

Separate $\overline{CE}$s reduce complexity

Because of the 2-line output control employed on the 512k-bit EPROMs, you have the choice of isolating the EPROMs with either separate $\overline{CE}$ or separate $\overline{OE}/V_{PP}$ control lines. It's better to have separate $\overline{CE}$s, because they eliminate additional complexity in the circuitry needed to switch between the programming-supply voltage (V_{PP}) and output enable ($\overline{OE}$) functions. Sepa-

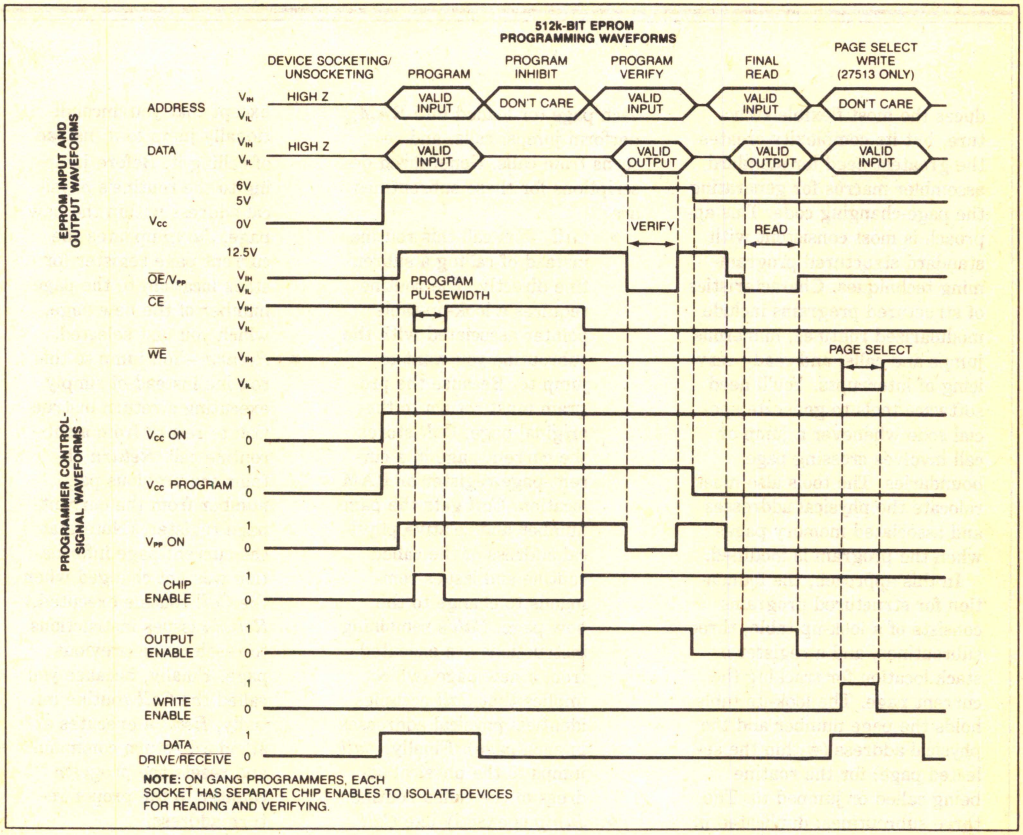


***Fig 2—Although the signals for programming 512k-bit** EPROMs are fairly straightforward, the sequence in which you apply the signals depends on the programming algorithm the manufacturer specifies. (These waveforms apply to Intel chips.)*

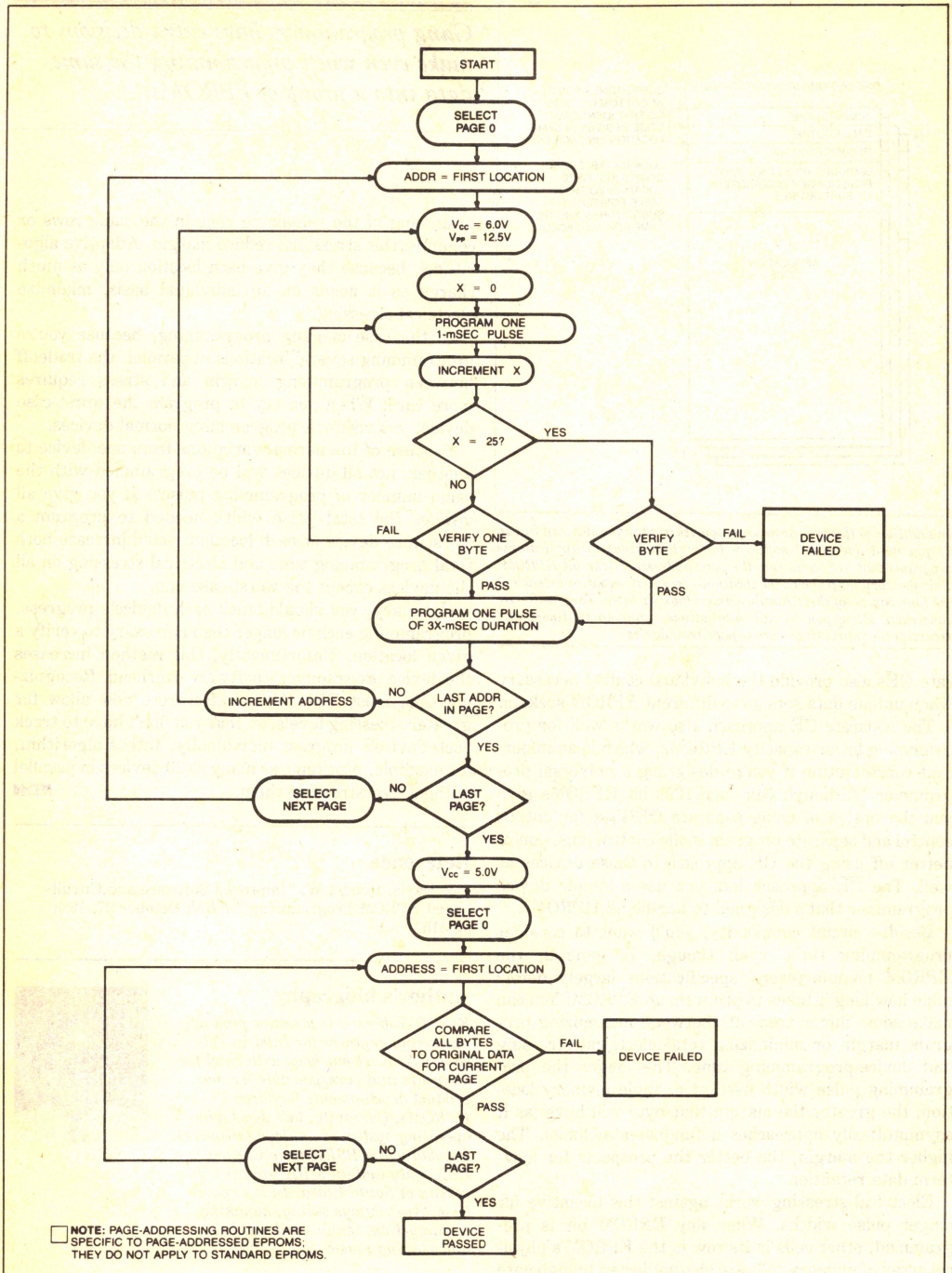
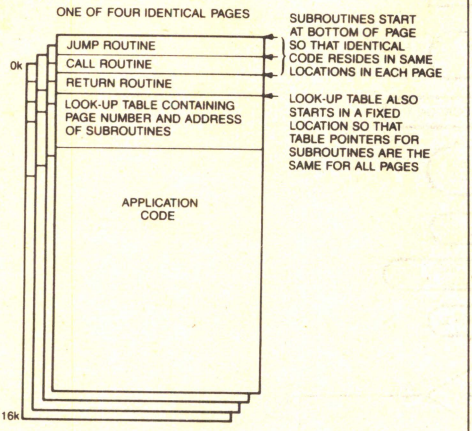


Fig 3—This flowchart illustrates the additions *you must make to the programming algorithm to accommodate the page-addressed, 512k-bit EPROM (the 27513). The shaded steps of the flowchart select a new page when appropriate.*


ONE OF FOUR IDENTICAL PAGES
JUMP ROUTINE
CALL ROUTINE
RETURN ROUTINE
LOOK-UP TABLE CONTAINING PAGE NUMBER AND ADDRESS OF SUBROUTINES
APPLICATION CODE
0k
16k
SUBROUTINES START AT BOTTOM OF PAGE SO THAT IDENTICAL CODE RESIDES IN SAME LOCATIONS IN EACH PAGE
LOOK-UP TABLE ALSO STARTS IN A FIXED LOCATION SO THAT TABLE POINTERS FOR SUBROUTINES ARE THE SAME FOR ALL PAGES

***In addition to the programming-algorithm changes** outlined in **Fig 3**, you need additional software for certain kinds of applications programs that are burnt into the page-addressed, 512k-bit EPROM. This memory map shows the location—repeated verbatim on each of the four pages—of three routines and a look-up table. These software constructs allow you to call subroutines, jump to routines, and return from subroutines across page boundaries.*

rate $\overline{CE}$s also provide the individual control necessary when unique data sets go to different EPROM sockets.

The separate-$\overline{CE}$ approach also works well for programming lower-capacity EPROMs, which is an important consideration if you're designing a universal programmer. Although 64k- and 128k-bit EPROMs give you the option of using separate $\overline{OE}/V_{PP}$s for output control and separate program-mode control pins, you're better off using the $\overline{CE}$ approach in those devices as well. The $\overline{CE}$ approach lets you use a simple device programmer that's designed to handle all EPROMs.

Besides circuit complexity, you'll want to consider programming time, even though, in general, the EPROM manufacturers' specifications largely determine how long it takes to program an EPROM. You can make some minor tradeoffs between maximizing program margin or minimizing total electrical stressing and device-programming time. The longer the programming pulse width used at a single memory location, the greater the margin that byte will have (as it asymptotically approaches a fundamental limit). The higher the margin, the better the prospects for long-term data retention.

Electrical stressing works against this incentive for longer pulse widths. When any EPROM bit is programmed, other cells in its row in the EPROM's physical array of memory cells are also subjected to high gate voltage. Likewise, cells in the same column are subjected to high drain voltage. The first cells to be programmed are subsequently stressed during the programming of the remaining cells in the same rows or columns; this stress can reduce margin. Adaptive algorithms, because they give each location only as much charge as it needs on an individual basis, minimize electrical stressing.

Gang programmers have extra decisions to make even when programming the same data into a group of EPROMs.

In the case of gang programming, because you're programming several locations in parallel, the tradeoff between programming margin and stress requires more care: When you try to program the worst-case device, you risk overprogramming normal devices.

Because of the normal variations from one device to another, not all devices will be programmed with the same number of programming pulses. If you give all devices the total pulse width needed to program a worst-case device at each location, you'll increase both total programming time and electrical stressing on all the devices except the worst-case one.

Optimally, you should track each device's progress, programming each no longer than necessary to verify a given location. Unfortunately, this method increases the device programmer's software overhead. Recognizing this, most EPROM manufacturers now allow for greater stressing levels, so that you don't have to track each device's progress individually. Intel's algorithm, for example, programs as many as 20 devices in parallel without overstressing them. **EDN**

Reference

1. Davis, Robert W, "Improved Software and Circuits Speed EPROM Programming," *EDN*, October 27, 1983, pg 315.

Author's biography

Kurt B Robinson is a senior product-marketing engineer for Intel in Folsom, CA. Kurt has been with Intel for six years and is responsible for new product developments for large EPROMs. Currently, he's developing operating systems in silicon (siliware). He obtained a BSEE from Cornell University and an MBA from the University of Santa Clara. In his spare time, Kurt enjoys skiing, kayaking, motorcycling, tennis, sailboarding, and playing music.

Marriage Of CMOS And PLCC Sparking Rapid Change In Mounting Memories

By Alan Hanson

The surge in circuit complexity over the past year or two has pushed the standard DIP size beyond workable dimensions, and rendered it obsolete where high lead count is required.

Meanwhile, the semiconductor industry's shift to CMOS processing for memories, as well as other ICs, is helping usher in the era of surface-mountable packages. Chief among these packages for memories is the plastic-leaded chip carrier (PLCC).

The technology for surface mountables and CMOS processing emerged from shaky beginnings. Although surface-mount packaging has been available for nearly two decades, its potential has just begun to be realized.

Several technical problems hampered its early acceptance: the need for automated factory equipment; prohibitively high packaging costs; and the lack of necessary construction tools.

As of 1984, only 6 percent of all components used in the United States were surface-mount types. Industry analysts predict, however, that with the increase in packaging options, the availability of development tools and the rising demand for surface-mountable devices, more than 25 percent of components will be surface mounted by 1988. And an estimated 128 million of the 600 million PLCCs manufactured in 1988 are expected to be memories.

CMOS has had to fight a similar battle. Prohibitively high cost, inherently low performance (metal gates) and lack of a complete lineup of products necessary to provide low-power system solutions were the chief reasons for CMOS' slow start. But, these problems have now been overcome and the number of products combining CMOS technology and surface-mount packages is accelerating rapidly.

PLCC Inroads

The decision to move from insertion (through-hole) to surface-mount technology is not an easy one. The available options are somewhat confusing:

- Are space constraints a problem?
- Is more functionality required?
- Will surface mounting make a more competitive product?
- Will manufacturing-cost savings be realized?
- Is the proper assembly equipment already available?
- Do components meet JEDEC standards?
- Will socketing be required?

The drive for smaller, more functional and more competitive products is forcing many engineers to scale down existing designs; to strive for VLSI solutions; and to use PLCC packages and other surface-mount packaging options, which can reduce board size dramatically.

Decisions as to which surface-mount option to use are usually based on board-size restrictions. In general, PLCCs minimize the area footprint on a board for lead counts ranging from 28 to 124.

One example of the space-saving ability of a PLCC package is Intel's new 32-lead PLCC package which it is developing for its 64k and 256k CHMOS EPROMS. The PLCC measures 0.45 × 0.55 inch, whereas the 28-pin DIP that would normally be used here measures 1.4 × 0.6 inch. The reduction in area footprint is 70 percent.

The contact area for chip leads can be closer for a PLCC device because the mounting holes mandatory for insertion devices are eliminated. Surface mounting also allows components to be placed and soldered on both sides of a pc board where through-hole mounting is not employed. Depending on the complexity and type of components required in the board layout, a 35- to 60-percent reduction in board size is possible.

To minimize total chip requirements, manufacturers of products such as EPROMs are incorporating an address latch on the address and data pins to allow direct interface with a microcontroller or microprocessor. This eliminates the need for an external latch, as well as reducing board size.

Surface-mount elements can also reduce component weight as much as 75 percent.

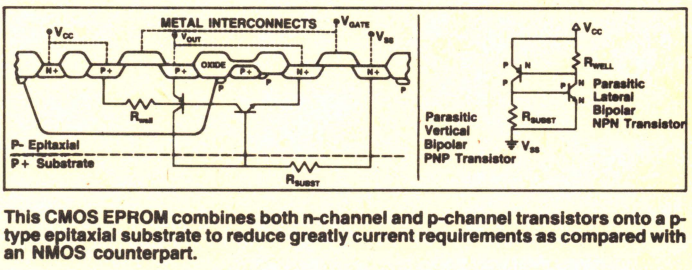
Lightweight PLCC packages tend to be ideal for high-vibration industrial and automotive applications, as well as for portable applications.

Surface mounting requires a substantial investment in capital equipment. New techniques for soldering components to boards (i.e., vapor phase or wave soldering) must be considered and automated machinery such as pick-and-place assemblers must be employed—new pick-and-place machinery employing vacuum pickup has been developed to handle the wide array of different sized packages available for surface mounting.

Today, many different machines are available. Their processing capacity ranges anywhere from 500 to 500,000 devices per hour. (Surface-mounting technology is even used in small-volume, custom facilities, such as for making portable medical equipment, where the devices are manually soldered to boards.)

The benefits of factory-automated assembly are numerous. Less floor space is required. Since raw materials are contained in smaller packages, storage space is diminished. Lighter-weight components reduce shipping and handling expenses. Space-saving benefits can be achieved in the layout of the assembly equipment itself. Some manufacturers have been able to reduce the required factory floor space by as much as 25 percent. Other cost savings include a reduced labor force, the ability to maintain a no-shutdown assembly, improved reliability and reduction of inspection and rework.

These benefits must outweigh, of course, the costs of automating the factory, as well as the cost of restructuring and retraining.



This CMOS EPROM combines both n-channel and p-channel transistors onto a p-type epitaxial substrate to reduce greatly current requirements as compared with an NMOS counterpart.

Electronic Engineering Times — Monday, September 30, 1985

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When choosing between packaging alternatives, consideration should always be given to industry-wide standardization to avoid unnecessary design mismatching and insure upgradeability. For example, the 32-lead PLCC package was chosen for high-density EPROMs because as much as 512 kbits of address space is easily contained within this package size. Furthermore, PLCC devices with as many as 124 J-type leads have been registered with JEDEC, the standard-setting body for the industry.

A J-type lead extends out of the four sides of a PLCC package and is tucked under the body into small pockets. It was chosen as the industry-standard lead type as opposed to gull wing for several reasons. A minimum-area footprint is best achieved with a J-lead—gull wings extend horizontally out from the body of the package, increasing the required area footprint of the component. Because of their extended leads, gull-wing devices are also at greater risk to damage during assembly or transporting.

J-type leads are also more aptly suited for socketing, which may be particularly important for memory components subject to periodic updates. The J-lead PLCC does, however, have its drawbacks, the most noticeable being the difficulty encountered in inspecting solder joints.

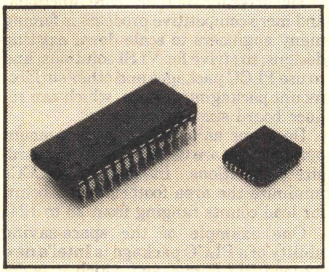
The next step for design engineers who have decided to use PLCC components is to investigate the available process-technology alternatives.

CMOS And PLCC Packaging

Applications ideal for both CMOS parts and PLCC packages lie in low-power portable products in space-constrained environments. Examples can easily be found in the automotive, telecommunication and portable-instrument markets.

Alan Hanson is product marketing engineer, Intel Corp., Folsom, Calif.

CMOS' greatest strength lies in its low-power properties. For example, Intel's 27C64 CHMOS EPROM, which combines both n-channel and p-channel transistors onto a p-type epitaxial substrate, maintains a maximum operating current of 10 mA, standby current of 100 mA and offers 200-ns total access time. Its NMOS counterpart would require six times more active current, 200 times greater standby current and would offer no improvement to total access time.



Both the 28-pin DIP and 32-lead PLCC can hold anywhere from 32k to 512k EPROMs. But, the carrier is roughly a third smaller.

PLCC packages are essential in portable applications because of their space-saving and lightweight features. Minimizing component packaging size, however, achieves little if used in conjunction with bulky power supplies, batteries and cooling devices. Because of its low-power requirements, CMOS helps minimize the need for large power supplies and cooling devices, as well as enhancing PLCC-device reliability.

Because of their reduced package size and plastic construction, PLCCs are poor heat conductors compared with the larger DIP packages. So heat-related breakdowns are more likely—heat dissipation is generally a function of package material, length and construction of leads, package surface area and, of course, the power consumed by the devices.

In improving the overall integrity and reliability of surface-mountable components, methods must be employed to deal with thermal-management problems. The chief way to accomplish this for PLCCs is to reduce the resistance to heat flow from the active junction to the atmosphere.

Thermal resistance ranges from about 40C° per watt for a 68-lead PLCC package to more than 100C° per watt for the 20-lead device. Copper alloy leads, modified substrate materials, and special heat sinks are being used at the package and board levels to maximize heat conduction.

In VLSI applications where increased device functionality is required, thermal management becomes an acute problem. As functionality increases, power demands likewise increase. The resulting higher operating temperatures may result in severe degradation to device operation and performance.

CMOS offers a solution to thermal-management problems. For example, the 27C64, with a maximum operating current of 10 mA, generates 50 mW of heat—a sixth the amount of its NMOS counterpart.

Depending on the particular design and application, special heat-sink designs and/or cooling fans can be reduced or even eliminated with CMOS parts.

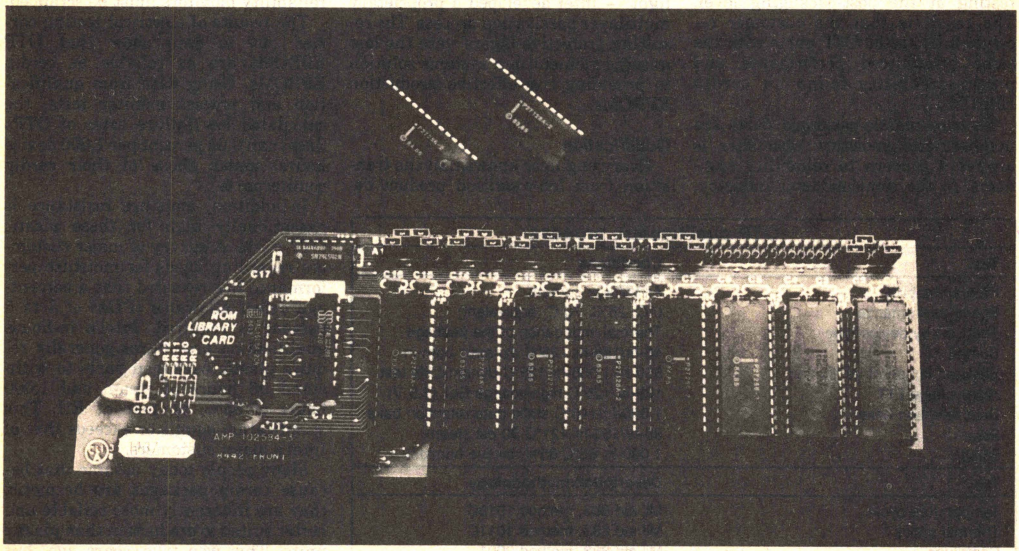
CMOS is particularly valuable in extended-temperature environments, such as automotive engine-control applications where operating temperatures range from −40°C to 80°C and as high as 125°C. In these applications, CMOS may be the only way to provide reliable device operation.

CMOS also brings to a PLCC package wider V_{CC} tolerances and HMOS compatability.

Support tools such as testing, soldering and programming equipment have also become available for CMOS-based surface-mount designs. **EET**

One-Time Programmable EPROMs

Plastic-packaged OTP EPROMs can offer the same performance as their cerdip counterparts, while being more cost-effective.



***1. Eight OTP EPROMs** of varying densities stuffed in this EPROM library board store bootstrap code, the microprocessor instruction set, and EPROM programming algorithms.*

By Richard Immekus and Richard Foehringer, Memory Components Div., Intel Corp., Folsom, Calif.

Ultraviolet EPROMs (erasable, programmable read-only memory), introduced in the early 1970s, have encountered phenomenal acceptance in the marketplace in the past few years. Annual usage is measured today in the hundreds of millions of units.

Where once EPROMs were used primarily in R&D environments and preproduction phases of a new product, today they are found in a multitude of mass-produced products ranging from telephones and video games to automobiles and home computers. The penetration into markets once dominated by masked ROMs is both due to their inherent flexibility of EPROMs (they can be programmed at a moment's notice) and the rapid convergence of EPROM and ROM prices over the last few years.

OTPs and test

A type of device known as "one-time programmable" (OTP) EPROMs offers the same performance as its cerdip counterpart, yet is inherently more cost-effective. In addition, these plastic production EPROMs can now be programmed nearly 100 times faster than cerdips. This dramatically reduces throughput time and paves the way for cost-effective, automated on-line programming.

Although most memory products (ROMs, DRAMs, SRAMs, etc.) have been available in plastic for years, this has not been the case with EPROMs. The essential characteristic of these devices, i.e., their UV-erasibility, made packaging them in plastic extremely difficult. Some early attempts were made by various manufacturers to produce plastic parts that incorporate a "window," similar to cerdip parts. These windows, however, tended to fall out or leak during steam and moisture testing and never proved reliable.

Without the window, the UV-erasability feature of an EPROM is lost and a major barrier to manufacturing OTP parts is erected. To be useful to the customer, EPROMs must be received in a blank state, yet still be tested during the manufacturing pro-

Order Number: 295016-001

cess to verify that they comply to published specifications and that each cell can in fact be programmed. Thus, verification entails programming, testing, and erasure. Intel has succeeded in refining its testing methodology to the point that each die is individually and thoroughly tested at the wafer level; the wafer is then UV-erased. In addition, proprietary innovative test modes have been incorporated into the EPROM design to allow performance testing at the post-packaging level. The result is that the customer receives fully tested OTP parts with the same guaranteed performance and programmability found on cerdip EPROMs.

Because plastic-packaged parts are non-hermetic, moisture resistance is always a concern to reliability engineers. In the semiconductor industry, nitride is very commonly used as a passivation layer and moisture barrier on ICs. With EPROMs, however, standard nitride passivation is not acceptable due to its non-UV-transmissive composition. In addition, EPROMs have a special sensitivity to moisture not found in any other state-of-the-art NMOS product.

Due to the nature of the storage cell in an EPROM structure, data is maintained in a non-volatile state via charges trapped on a phosphorus-doped floating polysilicon gate. Entry of moisture is due to passivation defects or passivation process marginalities and causes oxide damage, thereby creating a leakage path for the charge cell. Such occurrences can readily be induced via steam "pressure cooker" testing or extended 85°C, 85 percent RH exposure, and are manifested as charge-loss failures.

In order to provide OTP parts that can withstand the effects of moisture and steam — i.e., exhibit no evidence of corrosion or charge loss and still be erased properly when exposed to UV light — Intel developed a proprietary multilayer passivation process. The resulting protective layers were the last missing element in a systems solution to providing cost-effective production EPROMs.

Qualification

Every engineer knows that the transition from lab-condition product design to mass production in a high-volume manufacturing environment is difficult at best. To minimize risks and ensure reproduceability, Intel takes each new product through a rigorous qualification procedure (see table) in which exhaustive tests, both destructive and non-destructive, are performed for both electrical and mechanical testing. Substantial amounts of electrical data are collected and scrutinized, and failures are analyzed to the last detail.

To ensure the quality and reliability of its products, Intel follows a "zero defects" program. Reliability monitors (Fig. 2) and lot-quality inspection sampling are carried out on each and every manufacturing lot. Electrical and visual inspection is performed to a 0.1 percent acceptable quality level (AQL).

Not only is outgoing quality sampled and verified, but programmability, infant mortality and long-term reliability are monitored on a weekly basis. These tests are conducted on finished products and, since OTPs are non-erasable, all devices used for quality and reliability monitors must be scrapped.

The results of electrical testing carried out to date show that OTP EPROMs are as reliable as cerdip EPROMs. Using data from qualification and process monitor tests, the calculated low failure rates of OTPs (less than 0.02 percent per 1,000 device hours) match those of their cerdip counterparts.

In addition, moisture resistance is exceptionally high for these plastic OTP parts. A survey of major customers regarding needs for moisture performance has revealed that a percentage defect allowable (PDA) of 3 to 5 percent is required. Intel's in-house qualification procedures generally require plastic packaged parts to withstand 96 hours of steam and 1,000 hours of 85°C, 85 percent RH. This specification equals or exceeds that of Intel's major customers.

Many people today assume that because cerdip packages are hermetic, they are inherently more reliable and better suited to production than plastic units. This was true years ago, but with the advent of automated assembly lines, and particularly autoinsertion equipment, a problem with cerdip usage began to emerge. It was found that cerdip packages occasionally chip or crack if not handled properly. Plastic packaged components, however, do not experience this deficiency.

Today, plastic EPROMs are prevalent in most computers, video games, modems, printers, electronic typewriters, and other products. The increasing demand for highly automated assembly lines and production flow demanded by these items will lead to increasing use of plastic packaged components at the expense of cerdip packages.

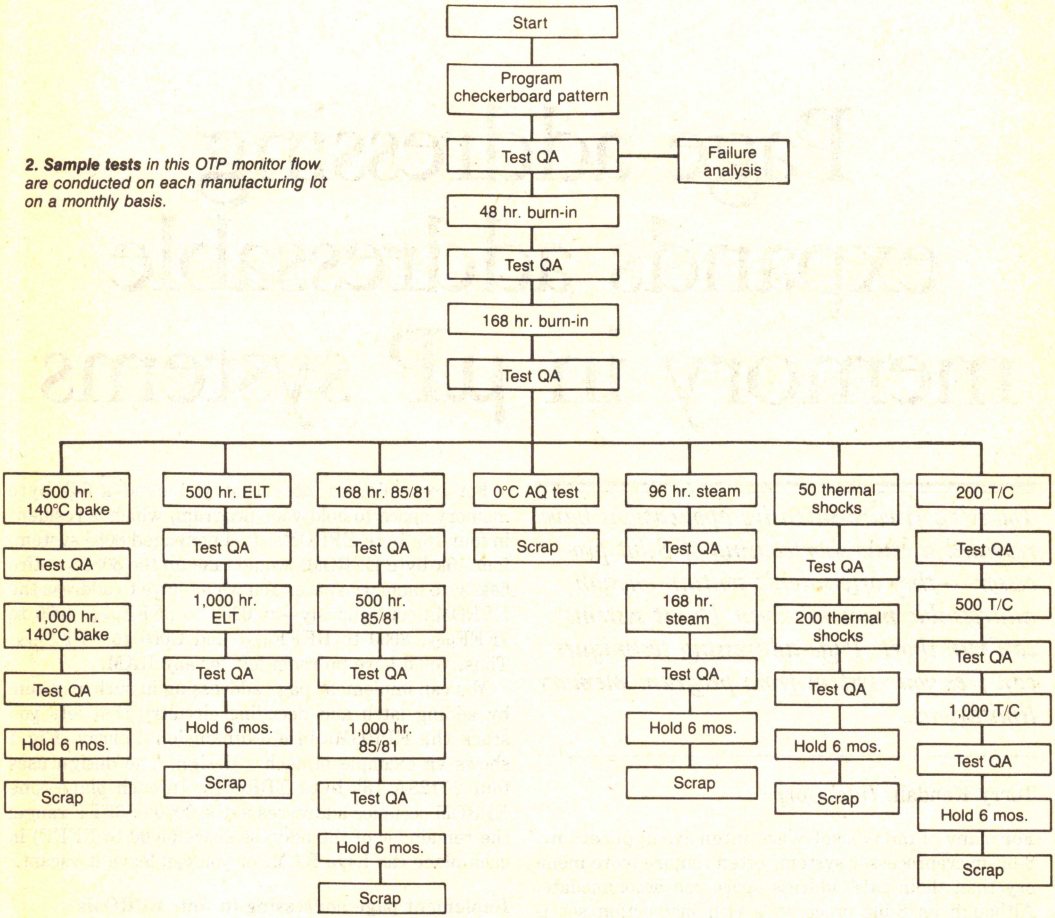
Fast programming issues

Earlier it was stated that OTP production EPROMs can be programmed almost two orders of magnitude faster

OTP qualification process

Test	Conditions
Programmability	All voltage corners
Speed performance	0°C, 25°C, 70°C (equivalent)
Theta JA by device type	Thermal impedance of the package
Burn-in	48-hr/168-hr 125°C dynamic burn-in
Elevated temperature life test	500-hr/1,000-hr 125°C dynamic life test
High-voltage ELT	168-hr/125°C high-voltage ELT (6.5 V)
Data retention bake	1,000-hr/140°C static data retention bake
Steam	96-hr/168-hr 121°C 30 psi steam
85/85	1,000-hr 85°C/85% relative humidity
Test*	**Description/methodology**
Temperature cycle	Mil std 883, method 1010C
Thermal shock	Mil std 883, method 1011C
Centrifuge	Mil std 883, method 2001
Bond pull	Mil std 883, method 2011
Die shear	Mil std 883, method 2019
Lead fatigue	Mil std 883, method 2004
Solderability	In-house, 2-hr 170°C, 1-hr steam

*Tests conducted to determine the mechanical worthiness of Intel's 28-pin OTP package.



***2. Sample tests** in this OTP monitor flow are conducted on each manufacturing lot on a monthly basis.*

than cerdip equivalents. When one considers that most 256K EPROMs generally program in four to six minutes and that an OTP such as the P27256 can be programmed in less than four seconds, one begins to realize the magnitude of the time savings and increased throughput potentially available to the user with OTPs, without a corresponding compromising of device reliability.

A new approach, designated by Intel as the Quick-Pulse Programming algorithm, permits these faster programming speeds through the use of much shorter pulses than required by previous programming algorithms. For example, Intel's earlier Intelligent programming algorithm, which is still required for cerdip parts, uses a one millisecond pulse and an overpulse scheme. By contrast, the Quick-Pulse Programming algorithm usually needs only a short 0.1 millisecond pulse with no overpulse. Increased Vpp latch-up protection is designed into these new OTP devices, and when V_{pp} and V_{cc} are raised program cell margin increases. ■

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Page addressing expands addressable memory in μP systems

Today's software-intensive applications have revealed a basic shortcoming of 8-bit processors—they often don't contain enough addressable memory. Even 16-bit systems can run short. Page-addressing techniques can free your system from program-memory limitations.

Terry Kendall, *Intel Corp*

For many of today's software-intensive applications, 8-bit microprocessor systems often require more memory than their μPs' address space can accommodate. Although an 8-bit processor's rich instruction set is usually adequate for most applications, the 64k-byte memory space of commonly used 8085s, Z80s, and 6800s can't accommodate enough RAM and flexible program memory for many modern applications. In fact, because firmware inhabits so much memory space, even 16-bit systems can run short of RAM. You can free both new and existing systems from program-memory limitations by using EPROMs, algorithms, and circuit techniques that let you implement page addressing.

Using page addressing to expand RAM is a well-established technique. You synthesize extra address lines by latching bits from the data lines that identify the page numbers.

For example, suppose that you need a 64k-byte memory space to hold your program, which is resident in four 16k-byte EPROMs. In a nonpaged 8085 system, four 16k-byte EPROMs would take up the 8085's entire 64k-byte memory space. You would have to address the EPROMs contiguously—at 0000 to $3FFF_{HEX}$, 4000 to $7FFF_{HEX}$, 8000 to $BFFF_{HEX}$, and C000 to $FFFF_{HEX}$. Thus, you'd have no room left for any RAM.

You can implement page addressing in such a system by adding latch and decoding circuitry that lets you stack the EPROMs in a 3-dimensional array. **Fig 1** shows an example of such a design. The design uses four 27128A 16k-byte EPROMs. In each plane, one EPROM occupies addresses in the 0000 to 3FFF range; the remainder of the address space (4000 to FFFF) in each plane can have RAM, or you can leave it vacant.

Implement page addressing in four EPROMs

Address decoder IC_{2A} generates EPROM and RAM block-select signals. When address lines A_{14} and A_{15} are TTL-low, IC_{2A}'s Y_0 output goes low, enabling decoder IC_{2B}. The value in IC_3's 2-bit latch selects one 27128A. To change IC_3's value, all you need to do is write a page number (0, 1, 2, or 3) to any address within the EPROM space, 0000H to 3FFFH. IC_{2A}'s Y_0 output will be low and the Write signal, $\overline{WR}$, will strobe a new page number (data bits D_0 and D_1) into IC_3, taking advantage of the EPROM's inherently free writable address space. During write operations, the EPROMs ignore any information on the data bus.

The R_1/C_1 network solves an important program-

Order Number: 295018-001

An 8-bit μP's 64k-byte memory capacity often can't hold enough RAM and program memory for many modern applications.

memory page-switching problem: that of boot-up initialization. At power-up, IC_3's latches are reset and page 0 is automatically selected. The microprocessor will always boot up at the same starting page.

Although it does expand the system's addressable memory, the design in **Fig 1** is not an ideal one. For one thing, putting so many devices on a board can impose capacitive and dc loading on address, data, and control lines, and can cause access-time and fanout degradation. It can also consume a lot of power and take up a lot of pc-board space. Further, the design doesn't let you easily add more program memory.

Replace four EPROMs with one

You can simplify the design by replacing the four 27128A EPROMs in **Fig 1** with a single 27512 EPROM, as shown in **Fig 2**. The 27512 contains a decoder equivalent to IC_{2B} that selects pages depending on the values of address lines A_{14} and A_{15}. Because it has fewer chips, the circuit in **Fig 2** exhibits less bus loading, consumes less power, and occupies less circuit board space than does **Fig 1**'s circuit.

Like the design in **Fig 1**, the design in **Fig 2** is not an ideal solution to the problem of expanding addressable memory: Although both these designs give your system added program memory, neither lets you easily expand the program memory further.

An ideal way to solve the problem would be to design an even simpler system that will permit future memory expansion. You can derive such a design from the circuit in **Fig 2** by replacing the circuitry inside the dashed line—latch IC_3, OR gate IC_4, the R_1/C_1 reset circuit, and the 27512 EPROM—with one 27513 or 27011 page-addressed EPROM (see **Fig 3**).

You can also derive the design in **Fig 3** directly from the circuit in **Fig 1**; this scheme lets you add address-

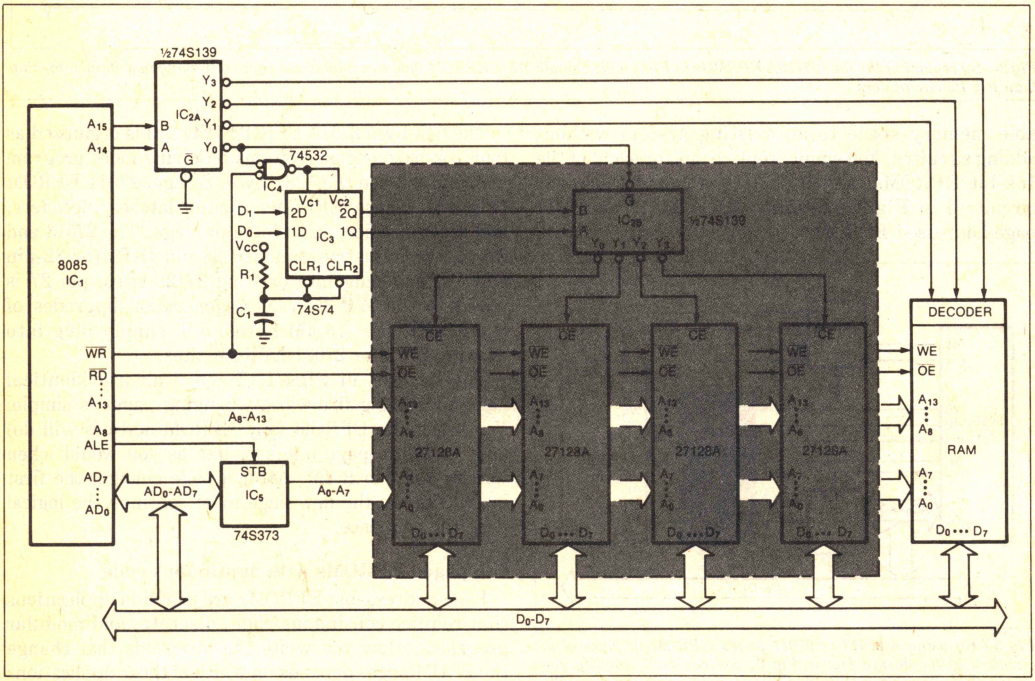

Fig 1—This block diagram of a typical 8-bit μP system *uses bank-switching techniques to provide a 3-dimensional array of EPROMs. The latch and decoding circuitry lets you select one 16k-byte EPROM bank at a time. You can reduce the amount of circuitry in the design by replacing the circuitry in the dashed box with a single 27512 EPROM.*

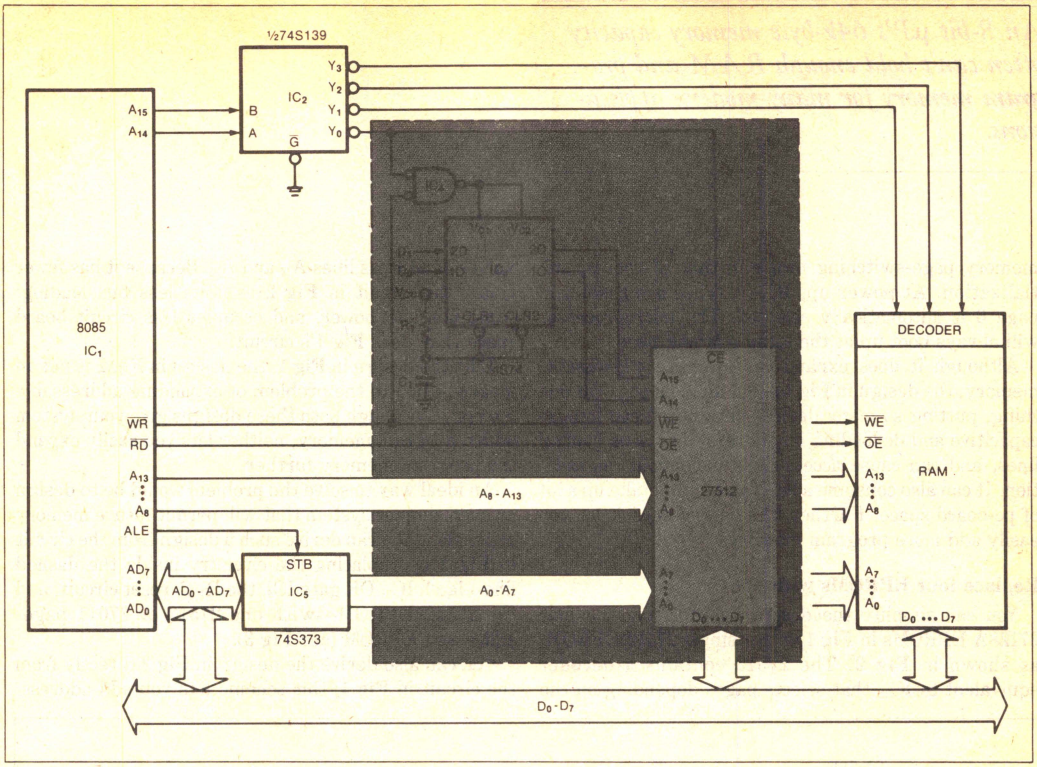

Fig 2—By replacing the four 27128A EPROMs in Fig 1 with a single 27512 EPROM, you can implement page addressing in a simpler fashion than Fig 1's circuit does.

able memory space to an existing system without adding circuitry. You simply replace one (or each) of the 16k-bit EPROMs (and IC_{2B}, IC_3, IC_4, and the reset circuitry) in **Fig 1**'s design with a 27513 or 27011 page-addressed EPROM.

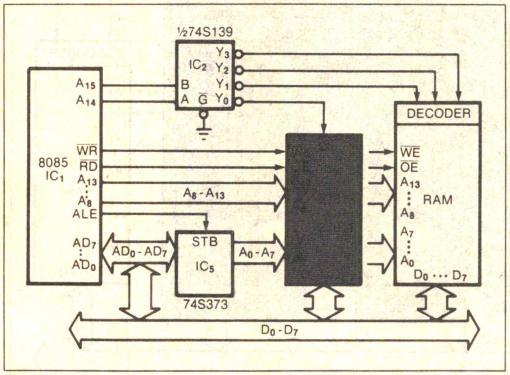

***Fig 3—By using a 27513 or 27011 paged EPROM** in place of the circuitry in the dashed box in **Fig 2**, you can both simplify your system design and provide an easily expandable memory space. This design can also be derived directly from the one in **Fig 1**: You merely replace one of **Fig 1**'s 27128A EPROMs and the paging-support circuitry with a 27513 or 27011 EPROM.*

The 64k-byte 27513 EPROM **(Fig 4a)** is organized as four 16k-byte pages. Systems requiring more program memory can use the 128k-byte, 8-page, 27011 EPROM **(Fig 4b)**. These EPROMs contain latches, decoders, and reset circuitry in a single package. The 27513 and 27011 use industry-standard 28-pin DIPs (or 32-pin PLCCs) and plug into existing 27128 sites; pin 27 is wired to the $\overline{WR}$ line. Next-generation upgrades of these EPROMs (to 4M bytes) will simply plug into existing 27513 or 27011 EPROM sites.

The designs in **Figs 1, 2** and **3** all use identical page-addressing firmware. Changing pages is simple: You select the EPROM (any EPROM address will do) and write the page number, just as you would when writing data to RAM. After a page change, the first instruction on the new page must continue the logical program sequence.

Use paged EPROMs with continuous code

Page-addressable EPROMs are useful in applications that require continuous-code, discrete, and modular programs. How you write the programs that change the PROM pages depends on which of these applications you're running.

Continuous code, for example, does not use subroutines that reside on other pages. A continuous-code

Page addressing synthesizes extra address lines by latching bits from the data lines that identify the page numbers.

program runs from beginning to end, changing pages only when it encounters page boundaries. A single statement (such as **Segment 1,** below) at the end of each 16k-byte page directs the program to the beginning of that page. Then a 2-line segment (**Segment 2**) at the beginning of each page changes the page.

At power-up, the paged EPROM automatically resets to page 0. Page 0's page-change instructions cause the program execution to begin on page 1 at location 0005H. Note that the page-change instructions are at identical locations on each page.

```
SEGMENT 1
ADDRESS     STATEMENT
3FFD        JMP  CHANGEPG

SEGMENT 2
0000        CHANGEPG  MVI  A (next page number 1, 2, 3, or 0)
0002                  STA  0000H          ;write page number to EPROM
....
```

Discrete programs that you use one at a time can reside within the same program space, one on each page. For example, a personal computer can use separate pages (overlays) to hold its operating system, diagnostic routines, high-level languages, and specialized software packages.

Word-processing, spreadsheet, and CAD applications require large amounts of RAM. Paged-EPROM overlays can hold these firmware packages, leaving the RAM free for user data. A software command or function key selects a new application by directing the

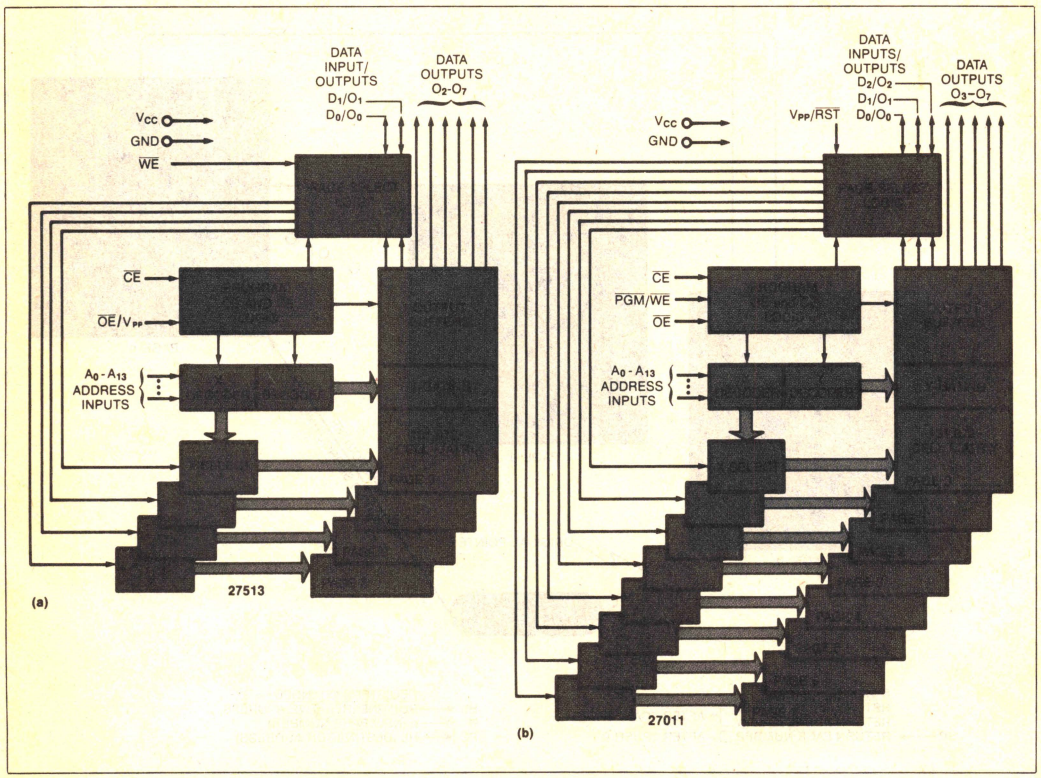

Fig 4—These paged EPROMs each provide 16k bytes per page. *The 4-page 27513 EPROM* ***(a)*** *yields a total memory space of 64k bytes; the 8-page 27011* ***(b)*** *provides 128k bytes.*

microprocessor to the routine in **Segment 3**. Each page must contain these instructions—at identical locations. After a page change, the program flow continues, uninterrupted, on the new page.

Most software is written in modular form. Subroutines call one another or are linked by a central driving routine. Calls and jumps don't access routines on another page directly; they must do so indirectly. A calling routine supplies the destination's address and page number to a universal page-turning routine. The universal Call/Jump routine accomplishes the page change and jumps to the destination.

To implement page addressing in any of the three systems illustrated, you can choose from three paging algorithms: the manual, look-up-table, and automatic paging algorithms. Although the algorithms are illustrated here by 8085 code, they adapt easily to 8-, 16-, or 32-bit systems.

SEGMENT 3

```
SOURCE      STATEMENT
APPONE      LXI    H (address of page 0 application)
            MVI    M,00  ;"M"(HL register) points to EPROM, so change
                         ;page to 0. Next instruction is on page zero.
            PCHL         ;program counter gets "HL". Jump to routine.

APPTWO      LXI    H (application-two (page 1) starting address.)
            MVI    M,01
            PCHL
etc.
```

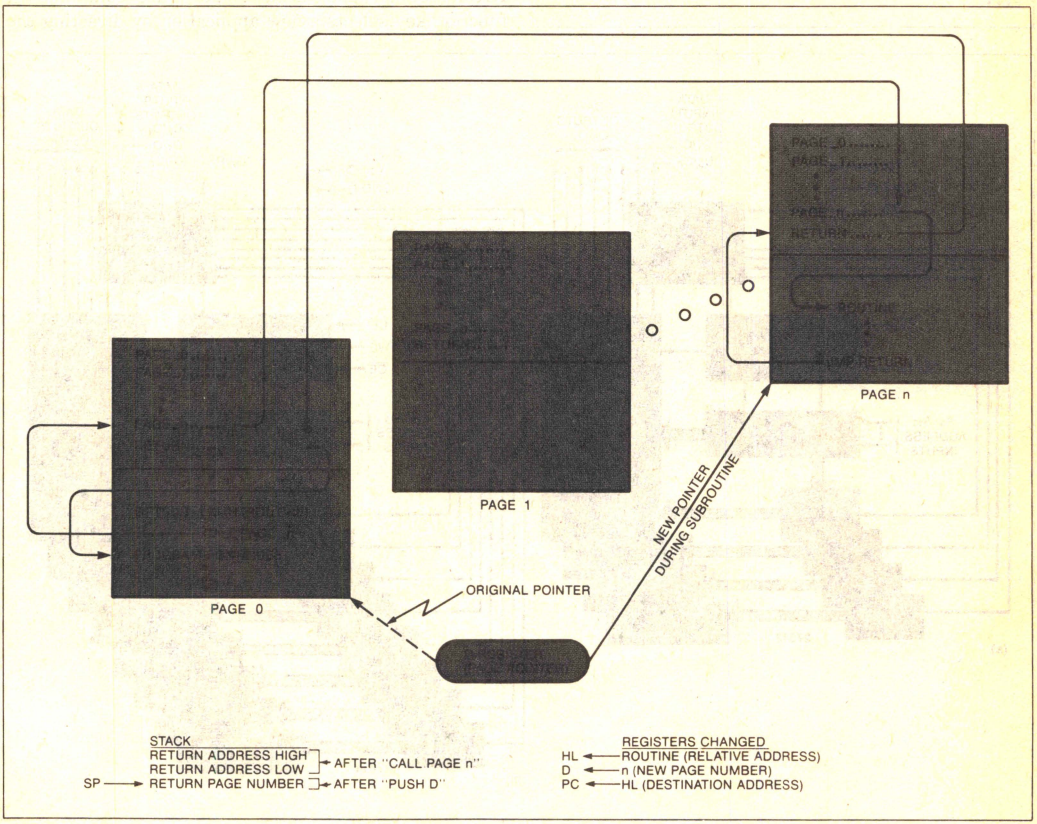

Fig 5—Manual paging requires a page-changing subroutine. *The programmer determines the page in which each routine resides and calls the paging subroutine, using the appropriate page number as an argument. This figure shows the flow of control.*

You can condense more program memory into a system by using page addressing within one EPROM instead of standard addressing within a group of EPROMs.

When you use the manual-paging algorithm, you determine the pages and relative locations for subroutines. This information is manually placed in Call instructions, which access subroutines on other pages. Manual paging is an easily understood approach that lets you change pages quickly and allows you to upgrade easily to higher-density EPROMs. It does have certain disadvantages, however. For one thing, you must know the page and relative location of every call and jump. Further, the assembler has difficulty in assigning addresses to labels that are referenced in overlapping memory pages.

The user supplies the destination's page and relative address for each call or jump. In the following 8085 examples, the D register remembers the present page number (initialized to page 0, 00H, during boot-up) and the HL register points to the destination. The statements in **Segment 4** call a routine on another page.

Instead of ending a routine with a return instruction, you end it with the following instruction:

JMP RETURN

Page-change and return routines (**Segment 5**) are located at the same address on every page.

Jumps to destinations on other pages can also use these page-change routines. The statements in **Segment 6** perform a jump. **Fig 5** shows how a program using the manual-paging algorithm calls a routine.

```
SEGMENT 4
SOURCE      STATEMENT
GETSUB      LXI     H(routine)  ;"HL" gets destination.
            CALL    PAGEn       ;call paging routine (n = 0, 1, 2, . . .) that
                                ;turns to the subroutine's page.

SEGMENT 5
SOURCE      STATEMENT
PAGE0       PUSH    D           ;save present page.
TURNTO0     MVI     D,00        ;new page.
            MOV     M,D         ;change the page.
            PCHL                ;program counter gets destination.

PAGE1       PUSH    D
TURNTO1     MVI     D,01
            MOV     M,D
            PCHL
              o
              o
              o
RETURN      POP     D           ;retrieve old page.
            POP     H           ;retrieve return address.
            MOV     M,D         ;change page.
            PCHL                ;program counter gets return address.

SEGMENT 6
            LXI   H(destination)  ;"HL" gets destination's address.
            JMP   TURNTOn         ;jump to paging routine (n = 0, 1, 2, . . .).
```

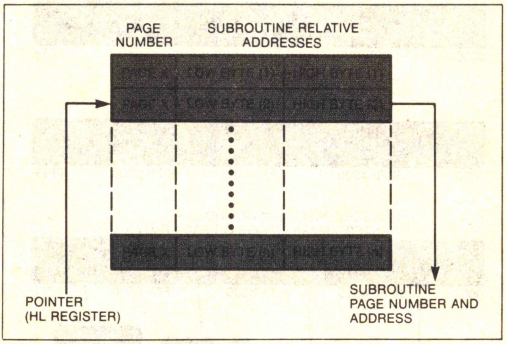

***Fig 6—You can use a look-up table** to locate the page number and address of each routine that is resident in the EPROM. Intel μPs require you to store the address bytes in the order shown here (low, high).*

Assembling the program takes two steps. First, you write code for each page as a distinct, 16k-byte program. This procedure anticipates the duplicate-addressing problems inherent in the stacked-page format. The assembler's first pass generates errors for labels that reside on other pages. Second, you merge the label tables for all pages, creating a master table. Then the assembler reassembles all the pages correctly by using this master table.

Look-up-table paging

If your programs require the use of global subroutines, consider using the look-up-table paging technique. (A global subroutine is a subroutine that's located on one page but can be accessed from any page.) In this technique, the global subroutines' page and address numbers are assembled into a look-up table. The look-up table allows random calls and jumps to routines on any page.

To access subroutines across page boundaries, you supply pointers to the table entries that contain each routine's destination address and page number. A pointer extracts location information during subroutine calls. **Fig 6** shows the look-up-table approach.

Call instructions load a pointer with the look-up table location that, in turn, points to the subroutine. A special call routine existing at identical locations on all pages extracts the page and relative address by using the pointer. It then changes the page and jumps to the destination. A return routine transfers control to the

To implement page-addressing, you can choose from three paging algorithms: manual paging, a look-up-table method, and automatic paging.

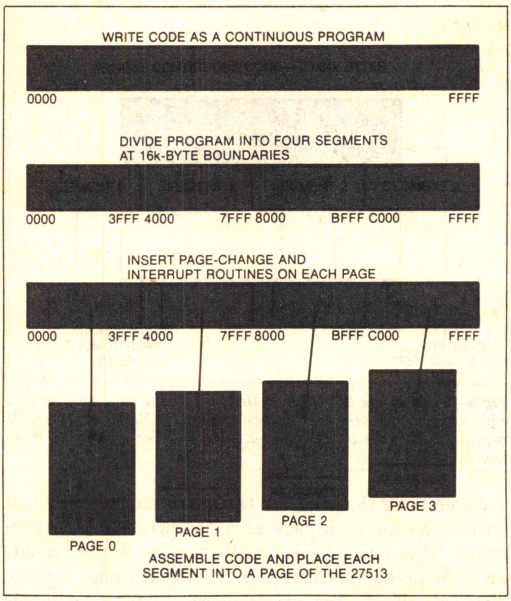

Fig 7—Automatic paging lets you write continuous code. *After assembling the code, you must break it into 16k-byte segments, each of which has a page-changing routine at the end.*

calling routine's page and relative address. **Segment 7** illustrates this technique.

A pagecall routine (**Segment 8**) extracts page and address information from the table. The JMP RETURN instruction at the end of a subroutine replaces the return instruction. Jumps between pages use the statements in **Segment 9.**

Each entry in the look-up table contains three bytes for page and address information. Thus, call and jump instructions supply labels that point to table entries for each routine. During program assembly, the assembler substitutes absolute addresses for the labels, and then places the addresses and page numbers in the table.

Automatic paging uses an index register

The automatic-paging algorithm allows you to write as many as 64k bytes of code in one block; however, the subroutine calls take place indirectly through an index register. Thus, the index register serves as a page and address pointer to subroutines. This algorithm uses a destination's two most significant address bits (as determined by the assembler) to determine the page number. A paging routine separates the page number and the relative address from the 16-bit destination address. **Fig 7** shows how the single block of assembled code fits into the four separate pages.

Each page must contain page-change and interrupt routines to connect the segments. **Segment 10** shows 8085 code for calling a subroutine via the automatic-paging method. Reset and interrupt routines, as well as paging routines (**Segment 11**), are placed at identical locations on each page (**Fig 7**). Destination addresses are loaded into the HL register. The pagecall/pageturn routine (**Segment 11**) performs "bit stripping," which handles page selection and relative addressing. Although the program memory appears to overlap the RAM, the bit-stripping procedure ensures that each occupies its unique location.

In sum, the paging routine performs four functions: It saves the old page number, isolates the two most

SEGMENT 7

```
SOURCE      STATEMENT
GETSUB      LXI   H,SUBPTRn  ;"HL" points to page information in table.
            CALL  PAGECALL   ;enter global call routine.
```

SEGMENT 8

```
PAGECALL    PUSH  D          ;save old page number.
PAGETURN    MOV   D,M        ;"D" gets new page.
            INX   H          ;point to destination's low byte.
            MOV   E,M        ;"E" gets low byte.
            INX   H          ;point to destination's high byte.
            MOV   H,M        ;"H" gets high byte.
            MOV   L,E        ;"L" gets low byte.
            MOV   M,D        ;change page.
            PCHL             ;jump to routine.

RETURN      POP   D          ;retrieve old page.
            POP   H          ;"HL" gets return address.
            MOV   M,D        ;change the page.
            PCHL             ;return to main program.
```

SEGMENT 9

```
            LXI   H,JMPPTRn  ;"HL" gets table location.
            JMP   PAGETURN   ;enter global call routine.
```

SEGMENT 10

```
SOURCE      STATEMENT
GETSUB      LXI   H,routine  ;"HL" gets destination, as determined by the
                             ;assembler.
            CALL  PAGECALL   ;call the paging routine.
```

SEGMENT 11

```
PAGECALL    PUSH  D          ;save old page.
PAGETURN    PUSH  PSW        ;save anything in accumulator.
            MOV   A,H        ;"A" gets high address byte.
            RLC              ;rotate two most significant bits to
            RLC              ;least significant locations.
            ANI   00000011B  ;mask all but page-number bits.
            MOV   D,A        ;"D" gets page number.
            MVI   A,00111111B ;"A" gets relative location mask.
            ANA   H          ;strip most significant bits from "H".
            MOV   H,A        ;"H" gets high relative-address byte.
            MOV   M,D        ;change to new page.
            POP   PSW        ;"A" retrieves old information.
            PCHL             ;jump to subroutine.

RETURN      POP   D          ;retrieve old page number.
            POP   H          ;"HL" gets return address.
            MOV   M,D        ;change page.
            PCHL             ;return to program.
```

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significant bits of the destination (these bits contain the page number), uses these bits to change the page, and allows the remaining bits to contain the subroutine's relative address.

By implementing page-addressing techniques in your new and existing 8-bit-μP designs, you can prepare to meet the program-memory requirements of tomorrow's application programs. If you use paged EPROMs such as the 27513 and 27011, you'll be able to expand your system's addressable memory to as much as 4M bytes in the future. **EDN**

Author's biography

Terry Kendall is a technical marketing engineer at Intel's Memory Components Div (Folsom, CA), where he is responsible for EPROM-product applications. Before joining Intel almost two years ago, Terry worked as an architect. He has a BA in architecture from the University of Oregon and a BSEE from California State University at Sacramento. In his spare time, Terry enjoys skiing, backpacking, and playing the guitar.

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ELECTRONIC COMPONENT NEWS

TECHNOLOGICAL HORIZONS

OTP EPROMs with Quick-Pulse Programming™ offer ideal mass production firmware storage

V. Siva Kumar
Product Marketing Engineer
Intel Corporation

In today's manufacturing environment—where production flexibility, just-in-time inventory management, and, above all, quick throughput are needed—EPROMs have established themselves as the solution for cost-effective firmware production. Intel Corporation, having invented the EPROM in the seventies, has continued to pioneer advances that have made EPROMs the choice over masked ROMs as high-volume firmware carriers. Intel's one-time programmable (QTP) plastic-packaged EPROMs, that can be programmed in a few seconds using the new Quick-Pulse Programming™ algorithm, will supplant both CERDIP EPROMs and masked ROMs in this firmware storage task.

These plastic-packaged production EPROMs, currently available in densities up to 256 kilobits, are the world's first EPROMs that are programmable using the new Quick-Pulse Programming algorithm. This programming algorithm achieves up to two orders of magnitude reduction in programming time compared to existing programming algorithms. Volume usage of high density EPROMs is now more cost-effective than ever through the use of OTP plastic packaged EPROMs with programming techniques employing this algorithm.

To high-volume users of EPROMs, programming time is a large component of throughput time. As EPROM density has continued to treadmill toward the megabit level, programming times have become a major concern to system manufacturers. Even the industry standard Inteligent™ algorithm consumes a sizable amount of time in programming mature densities. Therefore, if high-density EPROMs are to serve the manufacturing requirement of quick throughput, programming times must be reduced. Innovation yielded the answer to this problem in the form of Intel's new Quick-Pulse Programming algorithm.

EPROM programming time evolution

Until the advent of Intel's Inteligent Programming algorithm in 1983, EPROM programming was done using a nominal 50-millisecond programming pulse per EPROM byte, a method that required about 1.5 minutes to program a 16 kilobit EPROM. If that same programming technique were employed for higher EPROM densities such as the 256-kilobit, as many as 24 minutes would be required to program the device. The Inteligent algorithm therefore was devised to improve programming throughput for the higher densities available at that time—namely the 64-kilobit and 128-kilobit EPROMs.

The Inteligent Programming algorithm was the first algorithm to exploit the fact that only a few EPROM cells required 50-millisecond pulses to program while a majority of the cells were successfully programmed with substantially shorter pulses.

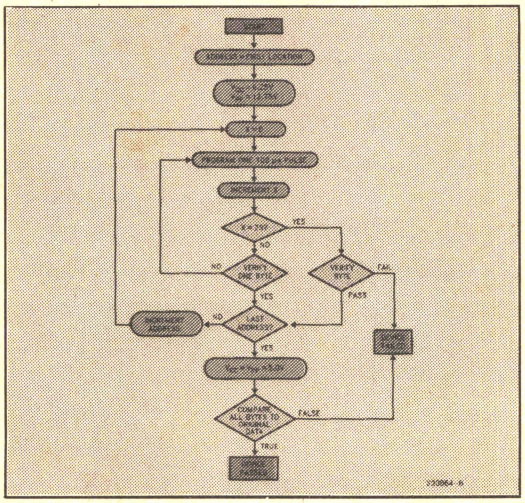

Fig. 1 — Quick-Pulse Programming Flowchart

This algorithm employed a closed-loop technique of margin checking. Nevertheless, this programming technique still required pulse widths in the millisecond range with mandatory overpulses. Hence, the Inteligent algorithm takes several minutes to program the highest density EPROMs available today (265 and 512 kilobits).

Thus, the stage was set for a breakthrough in programming algorithm development. The objectives were simple: (1) ensure the shortest possible programming time with the present technology and (2) maintain the programmability and data retention characteristics of the earlier algorithms. The Quick-Pulse Programming algorithm satisfies these objectives.

Quick-Pulse Programming algorithm

For the first time, advances in EPROM design and process technology allow the use of short programming pulses of only 100 microseconds.

The Quick-Pulse Programming algorithm takes advantage of tighter programming voltage tolerances in conjunction with the increased V_{PP} latch-up protection designed into Intel EPROMs. This latch-up protection allows V_{PP} and V_{CC} to be raised above the levels previously employed for programming, thus providing for greater program cell margins. The algorithm is made possible because of the improved HMOS II-E EPROM cell characteristics, carefully controlled cell profiles, oxide thickness and quality and channel length controls (see "Quick-Pulse—a Technical Explanation").

The flow chart of the Quick-Pulse Programming algorithm is shown in Fig. 1. One can immediately see that the algorithm is inherently similar to the earlier Inteligent Programming algorithm in that it benefits from the different characteristics of individual EPROM bits. Different cells require a varying number of programming pulses, and an iterative closed-loop scheme allows flexibility in employing just the right number of pulses required by each cell.

The programming of an EPROM using the Quick-Pulse Programming algorithm is done as follows. The programming voltage V_{PP} should be set at 12.75 V with V_{CC} set to 6.25 V (higher than the 5V V_{CC} used during normal operation). Iterative programming pulses of 100 microseconds are then applied. After each pulse, the algorithm checks the EPROM output to verify the desired programmed value. If the output is incorrect, the algorithm repeats the pulse-and-check operation. If after 25 such iterations the output of that byte still does not verify correctly, the device failed programming and is rejected. If the byte verifies accurately within 25 pulses, programming of that byte has been accomplished and the next byte is similarly treated. Data gathered from the programming characterization of the Intel EPROM cell shows that over 99 percent of the cells only require one programming pulse. After all the bytes are programmed, there is a final verification operation that compares all the programmed bytes to the original.

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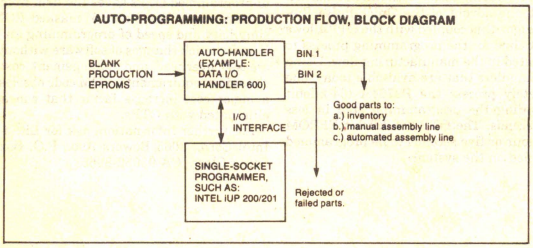


Using the Quick-Pulse Programming algorithm, the 256-kilobit EPROM can be programmed in a theoretical minimum time of 3.3 seconds compared to about four to six minutes required if the Inteligent algorithm were used. This fast programming time is achievable when the overhead associated with the programming equipment is minimized. The term "overhead" refers to the time required by the EPROM programming equipment to perform some operations needed to program an EPROM. Some of these operations are (a) verifying that the EPROM is inserted into the socket in the correct orientation, (b) reading the EPROM device identifier and manufacturer's code, (c) selecting the appropriate programming voltages, and (d) checking to see if the EPROM is in an unprogrammed state.

Most programmers currently available in the market are based on older and slower microprocessor designs and consequently have large programming overhead. However, newer programmer designs anticipated in the near future will utilize more efficient microprocessors, such as the Intel 80186 or 80188, and should therefore have substantially reduced overhead. The Quick-Pulse Programming algorithm, when used in conjunction with low programming overhead, achieves programming times close to the theoretical minimum, yielding a major improvement over the Inteligent Programming algorithm. Many manufacturers using large volumes of EPROMs design their own programmers or employ "on-board" programming (in-circuit programming of EPROMs). This new programming algorithm will allow these manufacturers to obtain the benefits of the reduced programming time. Table 1 shows the comparison of the programming times possible with the Quick-Pulse Programming algorithm on programmers available today as well as the theoretical minimum programming time with no programmer overhead.

PROGRAMMING TIMES

With Data I/O Model 120/121 (Firmware version V10):

	2764A	27128A	27256
Current algorithm	62 sec.	124 sec.	272 sec.
Quick-Pulse	16 sec.	32 sec.	68 sec.
Improvement	3.9×	3.9×	4×

With Intel Fast 27/K[a]

	2764A	27128A	27256
Current algorithm	41 sec.	80 sec.	158 sec.
Quick-Pulse	10 sec.	14 sec.	35 sec.

Theoretical limit with no overhead on programmer

2764A	27128A	27256
0.9 sec.	1.7 sec.	3.3 sec.

Table 1

Comparison: Quick-Pulse Programming vs. Inteligent Programming

The two main reasons that the Quick-Pulse Programming algorithm achieves its speed are the extremely short programming pulses and the elimination of the over-programming pulses.

The Inteligent Programming algorithm needed longer pulses of 1 millisecond for programming. However, the use of a higher V_{PP} programming voltage in the Quick-pulse algorithm (12.75 V compared to 12.5 V) increases efficiency (due to higher drain voltage) and maximum margin (due to higher gate voltages). This reduces the need for longer pulses and allows the new algorithm to employ pulses of 100 microseconds.

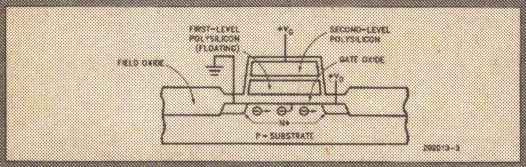
The Inteligent Programming algorithm utilizes a 3× over-program pulse at the end of each byte verification to ensure programming margin. This means that even when a cell takes only one 1-millisecond pulse to program, the over-programming caused the cell programming time to be 4 milliseconds; if the cell takes 2 milliseconds to program, the total time increases to 8 milliseconds. Thus, if the cell needed the maximum of 25 pulses to program, the total time consumed for program pulses and overprogram pulse would add up to 100 milliseconds.

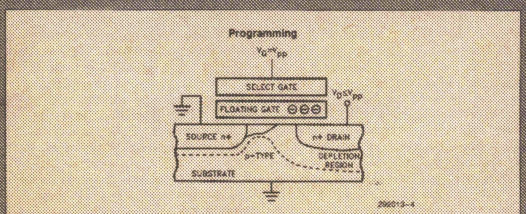
The Quick-Pulse Programming algorithm does not need the over-programming pulse to ensure adequate programming margins. The use of a higher V_{CC} is a more direct means of achieving the same result.

Thus, other than the reduction in the pulse width and the elimination of the over-programming pulse, the Quick-Pulse Programming algorithm resembles the Inteligent Programming algorithm, with both V_{CC} and V_{PP} programming voltages increased by 0.25 V. Table 2 shows the comparison of the two algorithms.

(cont. on next page)

Quick-Pulse — a technical explanation





Quick-Pulse Programming has been made possible through improved cell characteristics, carefully controlled cell profiles, oxide thickness quality, and channel length control.

Intel's HMOS II-E process uses a second level bipolar latch-up programming phenomenon which occurs when an N-channel MOS device acts like an NPN bipolar transistor. The source of the substrate junction becomes forward biased due to a high level of impact ionization currents being formed during normal MOS operation. This secondary current acts as base drive for the NPN-like structure which has formed.

This second level condition causes the drain current to increase significantly over normal available MOS levels of current. This chain reaction event is controlled through a depletion device configured in the form of a constant current source, effectively acting as a current limiter for the phenomenon. The end result of this process is that with injection efficiency being the same, the increased drain current due to the second level programming causes increased program current to the floating gate. The result is the user is directly reflected in greatly reduced programming time.

Intel's capability to mass produce HMOS II-E has in the tight process control of the cell profile, dropping levels of channel length, channel depth and oxide thickness.

COMPARISON: QUICK-PULSE VS. INTELIGENT PROGRAMMING

	Quick-Pulse	Inteligent
Pulse width	0.1 msec.	1 msec.
Max. # of pulses	25	25
Over-prog. pulses	no	yes (3× msec.)
V_{PP}	12.5–13.0 V	12.0–13.0 V
V_{CC} (programming)	6.0–6.5 V	5.75–6.25 V

Table 2

Programmability and data retention test results for the Intel P2764A and P27256 EPROMs are as follows for 168-hour burn-in: P2764A 1700 tested/0 failed; 7685 tested/0 failed. The test results show that the Quick-Pulse Programming algorithm does not compromise reliability and quality to achieve programming speed. Extensive characterization and reliability data were accrued to validate the algorithm.

OTP & Quick-Pulse Programming: cost-effective combination

The EPROMs currently qualified to be programmed using the Quick-Pulse Programming algorithm are Intel's production EPROMs, the P2764A, the P27128A and the P27256, which are plastic-packaged OTP (one-time programmable) versions of the 64-, 128-, and 256-kilobit EPROMs respectively. The P27512 and the P27513, the plastic-packaged 512-kilobit EPROMs, as well as upcoming plastic leaded chip carrier (PLCC)-packaged EPROMs, will also be qualified on this new algorithm.

Intel's OTP production EPROMs have qualities that are well suited for high-volume firmware manufacturing environments. It is in such high-volume manufacture that the benefits of reducing the programming time per device are magnified into large gains in productivity through reduced throughput. Thus the combination of production EPROMs with the Quick-Pulse Programming algorithm offers a significant advantage to large-scale firmware producers.

The reduction in programming times for the mature densities with the Quick-Pulse algorithm is significant. The savings in programming time translates directly into savings in programming costs, and, of course, the cost savings increase as the number of programmed parts increases.

Programming combines with auto-handling of OTPs

The high-reliability plastic package of the OTP EPROM has several unique advantages over the CERDIP package that make it highly suited for completely automated manufacture. The plastic package is extremely rugged and will not chip or crack in tube-to-tube auto-handling unlike the brittle ceramic package. The CERDIP package also may not have its base and lid aligned in exactly the same orientation, which also causes breakages when machine handled. The plastic packages are molded in one single piece with no separate lid or base and consequently have no alignment-related auto-handling losses.

Modern production technology is increasingly focusing towards complete automation as the means of improving quality and reliability and reducing manufacturing costs. With full automation as the goal, the advent of the Quick-Pulse Programming algorithm coupled with the OTP allows for the first time for the programming process to be incorporated in the manufacturing flow. Using automatic handlers that are available today, one can completely process the P2764A (64-kilobit OTP), including the programming step in less than two seconds. The OTP 256-kilobit EPROM only takes four or five seconds to be programmed and assembled on the system.

OTPs make ROMs obsolete

OTP plastic EPROMs have a major advantage to traditional ROM users and that is greater flexibility. In the fiercely competitive environment of today, quick time to market with the right product that meets the customers' changing needs is of the utmost importance. Maintaining an inventory of unprogrammed OTPs saves the firm from having to store many line items of masked ROMs. The simplicity and speed of programming an OTP allows for quick changes of software without any increased overhead and management costs. With changing requirements, ROM code obsolescence is a major cost increase factor that can again be eliminated with OTPs.

For further information, ask for Lit. # W-361, Intel Corp., 3065 Bowers Ave., P.O. Box 58065, Santa Clara, CA 95052-8065.

FLASH-EPROMs (Flash-Erasable Programmable Read Only Memories)

5

FLASH-EPROMs
(Flash-Erasable Programmable
Read Only Memories)

57F64
64K (8K x 8) CHMOS FLASH EPROM

- **Flash-Erase**
  - **Two Second Typical Array Electrical Erasure**
- **High Performance Speeds**
  - **150 ns Maximum Access Time**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current for Power-Down Savings**
- **Quick-Pulse Programming™**
  - **One Second Typical Chip Program**
- **On-Board Program/Erase**
  - **New Modes Simplify In-Module Firmware Upgrades**
- **2764A and 27C64 JEDEC Pinout**
  - **28 Pin Cerdip Package**

  (See Packaging Spec., Order # 231369)
- **CHMOS* Process Base**
  - **3 Year Manufacturing Base**
  - **$\pm$10% V_{CC} Tolerance**
  - **Improved Latch-Up Immunity through EPI Processing**

Intel's 57F64 CHMOS* Flash EPROM is a 64K bit non-volatile memory organized as 8192 bytes of 8 bits. The 57F64 electrically array erases, making it ideal for EPROM applications where U.V. erasure is impractical or time consuming. Electrical erasure allows manufacturers to efficiently implement code changes for testing and end-of-line final configuration.

To decrease the cost of servicing and updating program code, the 57F64 offers new programming and erase modes called On-Board modes. These modes simplify in-circuit programming and erasure by maintaining V_{CC} at 5V, and $\overline{CE}$ and $\overline{OE}$ at standard logic levels. Devices socketed or soldered to circuit boards can be erased and programmed via an edge connector to a PROM programmer, or via the board tester already available. The Flash-Erase and On-Board features give system designers innovative capabilities. Compared to byte alterable E^2PROM, these features address industry's need for a cost-effective code update solution.

Intel's unique CHMOS II-E Epitaxial (EPI) processing provides excellent latch-up immunity. Prevention of latch-up is specified for stress up to 100 mA from $-1V$ to $V_{CC} + 1V$ on address and data pins. All high voltage pins are protected from overshoot up to 14V.

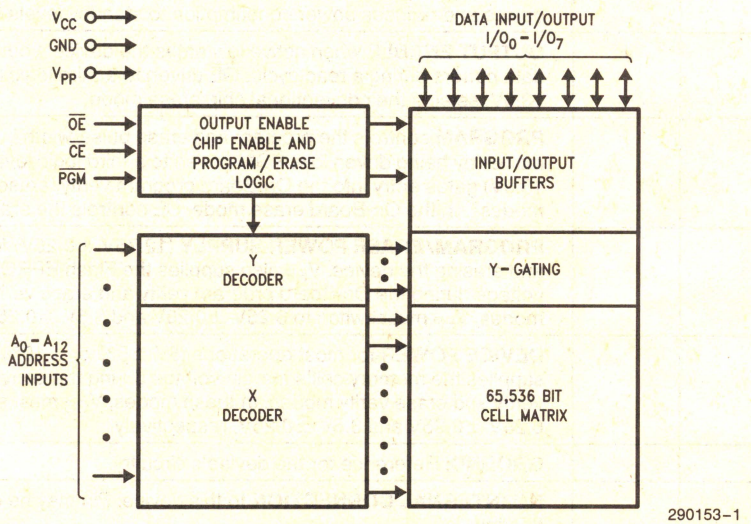


Figure 1. 57F64 Internal Block Diagram

*CHMOS is a patented process of Intel Corporation.

November 1987
Order Number: 290153-001

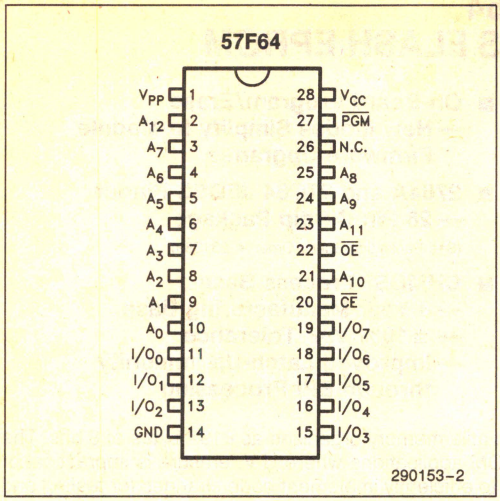


Figure 2. Cerdip (D) Pin Configuration

Pin Names

A_0–A_{12}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
V_{PP}	Program/Erase Power
V_{CC}	Device Power
GND	Ground
N.C.	No Internal Connection

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{12}	I	**ADDRESS BUS** inputs the memory addresses, and selects the 8 bits in the 256 row by 256 column array.
I/O_0–I/O_7	I/O	**DATA BUS** inputs data during memory program cycles; outputs data during memory read cycles. The data bus is active high and floats to tri-state OFF when the chip is deselected or the outputs disabled.
$\overline{CE}$	I	**CHIP ENABLE** activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	I	**OUTPUT ENABLE** when active low gates the device's output through the data buffers during a read cycle. $\overline{OE}$ driven to a third logic level V_H 11.5V–13.0V, selects the conventional chip erase mode.
$\overline{PGM}$	I	**PROGRAM** controls the program and erase pulse-width in the conventional modes by being driven low. $\overline{PGM}$ driven to a third logic level V_H (11.5V–13.0V) gates entry into the On-Board program verify, erase, and erase verify modes*. In the On-Board erase mode, $\overline{CE}$ controls the erase pulse width.
V_{PP}		**PROGRAM/ERASE POWER SUPPLY** (12.75V ±0.25V) for programming and erasing the device. V_{PP} also supplies the Flash EPROM cell margin voltage during the On-Board program verify and erase verify modes. In these modes, V_{PP} must switch to 6.25V ±0.25V and 3.5V ±0.25V, respectively.
V_{CC}		**DEVICE POWER** for most operations (5V ±5% or ±10%). V_{CC} also supplies the memory cell's margin voltage during the conventional program verify and erase verify modes. In these modes, V_{CC} must switch to 6.25V ±0.25V and 3.5V ±0.25V, respectively.
GND		**GROUND:** Reference for the device's circuitry.
N.C.		**NO INTERNAL CONNECTION** to this device. Pin may be driven or left floating.

NOTE:
*For complete discussion and explanation of the On-Board modes, refer to the On-Board device operation section.

PRINCIPLES OF OPERATION

The 57F64 features two distinct modes of operation—conventional EPROM and On-Board. Both follow the same program and erase algorithms although the implementations differ. Due to specified V_{CC} levels, the conventional modes tend to be more suited to programming and erasure in a PROM programmer, than to in-circuit code alteration. Intel offers the new program and erase methodology (On-Board modes) in consideration of the new trends in system design and manufacturing.

In all cases, the 57F64 Flash EPROM performs the read and standby functions exactly like Intel's 2764A and 27C64 EPROMs.

The following sections discuss the read mode and then the specifics of the two program/erase methodologies. Discussion of conventional modes precedes that of On-Board modes.

READ MODE

The 57F64 is functionally equivalent to the 2764A or 27C64 in the read mode, and can replace either in existing designs. The 57F64 has two read control pins, both of which must be logically active to obtain data at the outputs. Chip Enable ($\overline{CE}$) controls device selection and activates internal circuitry. Output Enable ($\overline{OE}$) controls the selected device's I/O buffers and gates data onto the output pins. The address access time (t_{ACC}) specifies the maximum delay time from stable address inputs to valid data out, with $\overline{CE}$ and $\overline{OE}$ active low. The chip enable access time (t_{CE}) specifies the maximum delay from $\overline{CE}$ active low to valid data, assuming stable addresses and $\overline{OE}$ driven low. Valid data becomes available on the outputs a maximum of t_{OE} after $\overline{OE}$ transitions high to low. The t_{OE} specification assumes stable chip selection and addresses for $t = t_{ACC} - t_{OE}$ or $t_{CE} - t_{OE}$. (See Figure 3. Read Operation A.C. Waveforms for graphical explanation.)

STANDBY MODE

With $\overline{CE}$ at a logic high (V_{IH}), the standby mode disables most of the 57F64's circuitry and substantially reduces the device's power consumption to 100 μA (with CMOS inputs). The outputs assume a high impedance state, independent of the $\overline{OE}$ input.

Table 2. Conventional Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Program/Erase Inhibit	X	X	X	X	X	V_{CC}(4)	5.0V	
Program	V_{IL}	V_{IH}	V_{IL}	X	X	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	12.75V	6.25V	D_{OUT}
Flash-Erase	V_{IL}	V_H(2)	V_{IL}	X	X	12.75V	3.5V	High Z
Erase Verify	V_{IL}	V_{IL}	V_{IH}	X	X	12.75V	3.5V	D_{OUT}
inteligent ID™ Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}(3)	V_{CC}	5.0V	89H
inteligent ID™ Device	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}(3)	V_{CC}	5.0V	03H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $11.5V \leq V_H \leq 13.0V$.
3. $A_1 - A_8$, $A_{10} - A_{12} = V_{IL}$.
4. With $V_{PP} \leq V_{CC}$, the 57F64 inhibits all erase and program functions.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C(1)
During Program/Erase ..... 25°C ±15°C

Temperature Under Bias ..... −10°C to +80°C

Storage Temperature ..... −65°C to +125°C

Voltage on Any Pin with Respect to Ground ..... −2.0V to +7V(2)

Voltage on Pin A_9, $\overline{PGM}$, or $\overline{OE}$ with Respect to Ground −2.0V to +13.5V(2, 3)

V_{PP} Supply Voltage with Respect to Ground During Programming/Erase ..... −2.0V to +14V(2, 3)

V_{CC} Supply Voltage with Respect to Ground ..... −2.0V to +7.0V(2)

Program/Erase Cycles 100

Output Short Circuit Current ..... 100 mA(4)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2V for periods less than 20 ns.
3. Maximum D.C. Voltage on A_9, $\overline{PGM}$, $\overline{OE}$, or V_{PP} is 13V. $\overline{OE}$, $\overline{PGM}$ or A_9 may overshoot to 13.5V for periods less than 20 ns. V_{PP} may overshoot to 14V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

Table 3a. Read Operation

D.C. CHARACTERISTICS TTL/NMOS Compatible

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	μA	$V_{CC} = V_{CC}$ max, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current		±10	μA	$V_{CC} = V_{CC}$ max, $V_{OUT} = V_{CC}$ or GND
I_{SB}	V_{CC} Standby Current		1.0	mA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current		20, 30	mA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA(1, 4)
I_{PP1}	V_{PP} Read Current		100	μA	$V_{PP} = V_{CC}$(2)
V_{IL}	Input Low Voltage	−0.5	0.8	V	$V_{PP} = V_{CC}$
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	$V_{PP} = V_{CC}$(3)
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA, $V_{CC} = V_{CC}$ min
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ min

NOTES:
1. Maximum active read power is the sum of I_{CC} active + I_{PP}. The maximum current value is with the outputs unloaded.
2. V_{PP} may be equal to V_{CC}, or one diode drop below V_{CC}.
3. If driven higher than V_{CC} + 0.5V during programming, the data input transistors will forward bias and pull down the bus driver.
4. 20 mA for STD versions; 30 mA for -2 and 150 ns versions.

Table 3b. Read Operation (Continued)

D.C. CHARACTERISTICS CMOS Compatible

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	μA	$V_{CC} = V_{CC}$ max, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current		±10	μA	$V_{CC} = V_{CC}$ max, $V_{OUT} = V_{CC}$ or GND
I_{SB}	V_{CC} Standby Current		100	μA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{CC} \pm 0.2V$(7)
I_{CC1}	V_{CC} Active Read Current		20, 30	mA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA(1, 5, 6)
I_{PP1}	V_{PP} Read Current		100	μA	$V_{PP} = V_{CC}$(2)
V_{IL}	Input Low Voltage	−0.5	0.8	V	$V_{PP} = V_{CC}$(3)
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	$V_{PP} = V_{CC}$(3, 5)
V_{OL}	Output Low Voltage		0.40	V	I_{OL} = 1.6 mA, $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage	0.85 V_{CC}		V	I_{OH} = −2.1 mA, $V_{CC} = V_{CC}$ min
V_{OH2}		V_{CC} − 0.4		V	I_{OH} = −100 μA, (4) $V_{CC} = V_{CC}$ min

NOTES:
1. Maximum active read power is the sum of I_{CC} active + I_{PP}. The maximum current value is with the outputs unloaded.
2. V_{PP} may be equal to V_{CC}, or one diode drop below V_{CC}.
3. To maintain CMOS leakage current specifications, do not drive the data inputs above V_{CC} or below ground.
4. V_{OH2} specifies the minimum high output voltage with 100 μA of bus leakage.
5. If driven higher than V_{CC} + 0.5V during programming, the data input transistor's will forward bias and pull down the bus driver.
6. 20 mA for STD versions; 30 mA for -150, -170 and -200 ns versions.
7. Signal driving $\overline{CE}$ is assumed to be in the CMOS logic "1" steady state.

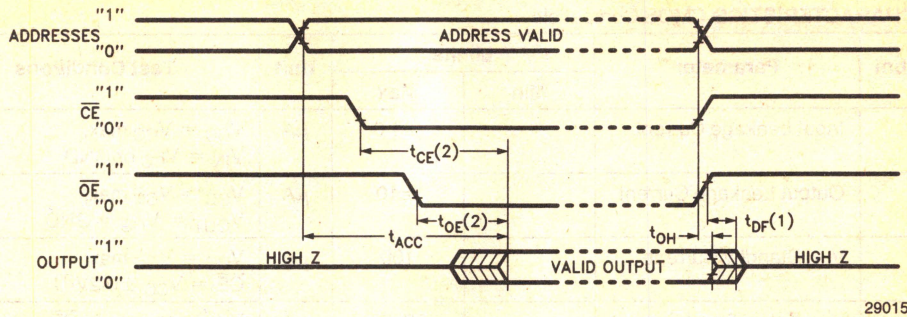
READ OPERATION

Table 4. Read Operation

A.C. CHARACTERISTICS 57F64(1) $0 \le T_A \le 70°C$

Versions	V_{CC} ±5%	D57F64-150V05		D57F64-170V05		D57F64-200V05		D57F64-250V05		Unit
	V_{CC} ±10%					D57F64-200V10				
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		65		70		75		100	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z		35		35		55		60	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First	0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OH} = 2.0V and V_{OL} = 0.8V.
2. Guaranteed and sampled.



NOTES:
1. This parameter is only sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

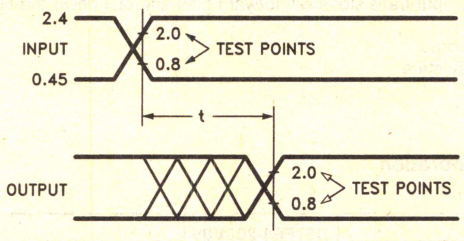
Figure 3. A.C. Waveforms 57F64

CAPACITANCE(1) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	pF	$V_{OUT} = 0V$

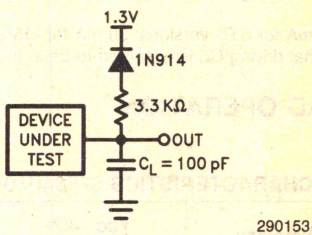
NOTE:
1. Sampled. Not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".
Rise/Fall Time ≤ 10 ns

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

CONVENTIONAL OPERATION

PROGRAM MODE

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

In the conventional program mode, the 57F64 operates like the P2764A and the 27C64 EPROMs. The Quick-Pulse Programming algorithm enables one second programming of the entire Flash array. (See Figure 8. Quick Pulse Programming Algorithm.)

Erasure removes charge from the Flash EPROM memory cells leaving the array in the logic high state (0FFH). Programming injects charge onto the floating gate, changing selected cell data to the low state. Data bytes can include both unaltered erased state and programmed state bits.

The method by which you enter the 57F64 into the programming mode is as follows: raise V_{CC} to 6.25V, raise V_{PP} to 12.75V, lower $\overline{CE}$ to V_{IL}, and select the desired address. While applying eight bits of data in parallel to the device's inputs, toggle $\overline{PGM}$ low to program the byte. (See Figure 4. Conventional Programming/Verify Waveforms.)

PROGRAM VERIFY MODE

Setting V_{PP} to 12.75V, V_{CC} to 6.25V, $\overline{PGM}$ to V_{IH}, $\overline{CE}$ and $\overline{OE}$ to V_{IL}, places the device in the program verify mode. V_{CC} provides an elevated reference level which guarantees a minimum of ten years' data retention in the normal read mode.

The Quick-Pulse Programming algorithm (Figure 8) requires a final array verify after the completion of byte programming. The system should verify the entire array with V_{CC} and V_{PP} at 6V.

FLASH-ERASE MODE

The Flash-Erase mode of the 57F64 eliminates the requirement of U.V. light for device erasure. Electrical erasure removes charge from all bits of the array in parallel, via Fowler-Nordheim tunneling.[1] The Flash-Erase algorithm controls the electrical erasure and verification sequence. (See Figure 9. Flash-Erase Algorithm.)

Enter the device into the Flash-Erase mode by lowering V_{CC} to 3.5V, raising V_{PP} and $\overline{OE}$ to 12.75V, and setting $\overline{CE}$ to V_{IL}. Toggling $\overline{PGM}$ low controls the erase pulse width. (See Figure 5. Conventional Flash-Erase/Verify Waveforms.)

ERASE VERIFY MODE

After returning $\overline{PGM}$ to a logic "1" level in the Flash-Erase mode, change $\overline{OE}$ from a high voltage level (12.75V) to V_{IL} to select the erase verify mode. Sequentially verify each address in the array for valid erased data (0FFH). V_{CC} at 3.5V provides the erased reference level for the Flash memory cell. Verification at this level guarantees ten years of data integrity for normal read mode operation.

Once all bytes in the array verify, the algorithm returns the device to the read mode, and performs a final erase verify at V_{CC} = 5V.

PROGRAM AND ERASE INHIBIT MODE

With V_{PP} and V_{CC} at 5V, the 57F64 effectively bars spurious programming and erasure of the Flash memory array. Other ways to control the program or erase modes include maintaining $\overline{PGM}$ or $\overline{CE}$ at a V_{IH} logic level.

inteligent Identifier™ MODE

The inteligent Identifier mode outputs the manufacturer code (89H) and device code (03H). Programming equipment automatically matches a device with its proper algorithms.

With $\overline{PGM}$ at V_{IH}, $\overline{CE}$ and $\overline{OE}$ active low, and A_1 through A_{12} at V_{IL}, raising A_9 to a high voltage level (11.5V–13V) activates the inteligent Identifier mode. Byte 0 (A_0 = V_{IL}) represents the manufacturer's code, and byte 1 (A_0 = V_{IH}) represents the device identifier.

REFERENCE

1. R. Williams, *Phys. Rev.*, Vol. 140, p. 569, 1965.

Table 5. Conventional Programming/Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Leakage Current (All Inputs)		±1.0	µA	$V_{IN} = V_{CC}$ or GND(7)
V_{IL}	Input Low Level (All Inputs)	−0.5	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5$ mA
I_{CC2}	V_{CC} Programming Current		30	mA	$\overline{CE} = V_{IL}$(3, 6)
I_{PP2}	V_{PP} Programming Current		30	mA	$\overline{CE} = V_{IL}$(3, 6)
V_H	High Voltage Detect Level	11.5	13.0	V	(Notes 4, 5)
V_{PP2}	V_{PP} Program/Verify Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(6)
V_{CC2}	V_{CC} Program/Verify Supply	6.0	6.5	V	$\overline{CE} = V_{IL}$(6)

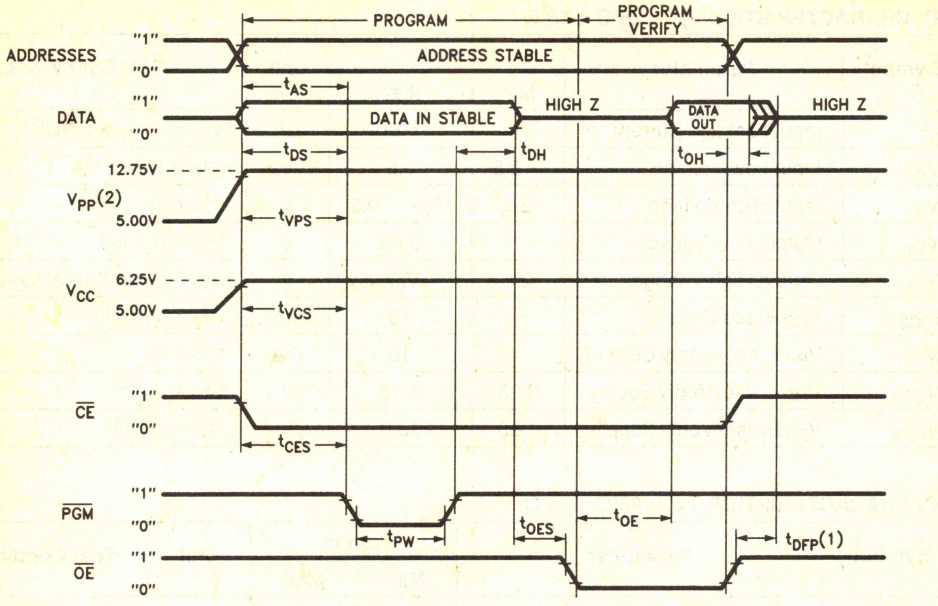
A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits				Test Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{CES}	$\overline{CE}$ Setup Time	2			µs	
t_{PW}	Program Pulse Width	95	100	105	µs	Quick-Pulse™
t_{OE}	$\overline{OE}$ to Output Delay			150	ns	

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied to the 57F64 before V_{PP} and removed from the device after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with the outputs unloaded during verfication.
4. V_H is the third logic level. The range of V_H encompasses the traditional 11.5V–12.5V, as well as the Quick-Pulse Programming V_{PP} range 12.5V–13.0V.
5. Forcing V_H on pin A9 and the proper levels on the control pins puts the device into the int$_e$ligent Identifier mode.
6. This specification applies to both programming and verification. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.
7. During program verify, the output leakage current $I_{LO} = \pm 10$ µA maximum. $V_{OUT} = V_{CC}$ or GND.



NOTES:
1. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
2. When programming the 57F64, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

Figure 4. Conventional Programming/Program Verify Waveforms

Table 6. Conventional Flash-Erase/Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	μA	$V_{IN} = V_{CC}$ or GND(7)
V_{IL}	Input Low Voltage	−0.5	0.8	V	(Note 1)
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.5$	V	(Note 1)
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 1.6$ mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	$I_{OH} = -400\ \mu A$ at V_{OH} (min)
I_{CC3}	V_{CC} Erase Current		10	mA	$\overline{CE} = V_{IL}$(5, 6)
I_{PP3}	V_{PP} Erase/Verify Current		10	mA	$\overline{CE} = V_{IL}$
V_{CC3}	V_{CC} Erase/Verify Supply	3.25	3.75	V	$\overline{CE} = V_{IL}$(6)
V_{PP3}	V_{PP} Erase/Verify Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(6)

A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
t_{VPS}	V_{PP} Setup Time	2		μs	(Note 2)
t_{VCS}	V_{CC} Setup Time	2		μs	(Note 2)
t_{CES}	$\overline{CE}$ Setup Time	2		μs	
t_{EW}	Erase Pulse Width	1	1855	ms	(Note 3)
t_{OES}	$\overline{OE}$ Setup Time	2		μs	
t_{PO}	$\overline{OE}$ to V_{IH} from $\overline{PGM}$ Hi	1		μs	
t_{ACC}	Address to Output Delay	2		μs	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay	2		μs	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		ns	
t_{DFE}	$\overline{OE}$ High to Output Float Delay	0	130	ns	(Note 4)

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is $V_{CC} + 0.5$V, which may overshoot to $V_{CC} + 2$V for periods less than 20 ns.
2. V_{CC} must be applied to the 57F64 before V_{PP} and removed from the device after V_{PP}.
3. Erase pulse width varies with pulse number. (See Flash-Erase algorithm.)
4. This parameter is only sampled and not 100% tested.
5. The maximum current value is with the outputs unloaded during verification.
6. This specification applies to both erasure and verification. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.
7. During erase verify, the output leakage current $I_{LO} = \pm 10\ \mu A$ maximum. $V_{OUT} = V_{CC}$ or GND.

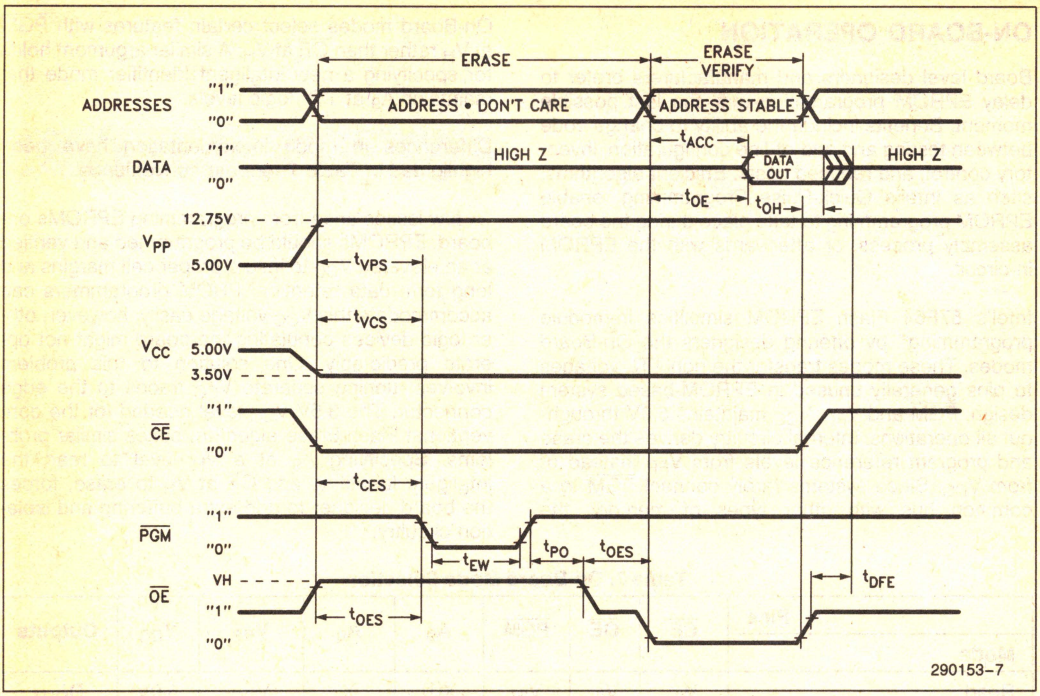


Figure 5. Conventional Flash-Erase/Verify Waveforms

ON-BOARD OPERATION

Board level designers and manufacturers prefer to delay EPROM programming until the last possible moment. Benefits include the ability to change code between testing and end-of-line configuration, inventory control, and reduced costs. Efficient algorithms, such as Intel's Quick-Pulse Programming, enable EPROM programming to take place during the board assembly process, or afterwards with the EPROM in-circuit.

Intel's 57F64 Flash EPROM simplifies in-module programming* by offering designers the On-Board modes. These modes transfer the non-TTL voltages to pins generally unused in EPROM-based system design: $\overline{PGM}$ and V_{PP}. V_{CC} maintains 5.0V throughout all operations. Internal circuitry derives the erase and program reference levels from V_{PP} instead of from V_{CC}. Since systems rarely connect $\overline{PGM}$ to a common bus with other types of memory, the On-Board modes select certain features with $\overline{PGM}$ at V_H rather than $\overline{OE}$ at V_H. A similar argument holds for specifying a new int$_e$ligent Identifier mode that maintains A_9 at TTL logic levels.

Differences in mode implementation have been highlighted in Table 7 for your convenience.

*A few issues arise from programming EPROMs on-board. EPROMs should be programmed and verified at an elevated V_{CC} to insure proper cell margins and long term data retention. PROM programmers can accommodate this V_{CC} voltage easily; however, other logic devices populating the board might not operate predictably. One solution to this problem involves running separate V_{CC} traces to the edge connector. The 3.5V V_{CC} level needed for the conventional Flash-Erase algorithm poses similar problems. Specifying A_9 at a V_H level to read the int$_e$ligent Identifier, and $\overline{OE}$ at V_H to erase, forces the board designer to add extra buffering and isolation circuitry.

Table 7. On-Board Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Program/Erase Inhibit	X	X	X	X	X	V_{CC}(4)	5.0V	
Program	V_{IL}	V_{IH}	V_{IL}	X	X	12.75V	5.0V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_H(2)	X	X	6.25V	5.0V	D_{OUT}
Flash-Erase	V_{IL}(5)	V_{IH}	V_H	X	X	12.75V	5.0V	High Z
Erase Verify	V_{IL}	V_{IL}	V_H	X	X	3.5V	5.0V	D_{OUT}
Int$_e$ligent ID™ Manufacturer	V_{IL}	V_{IL}	V_{IL}	V_{IL}(3)	V_{IL}(3)	V_{CC}	5.0V	89H
Int$_e$ligent ID™ Device	V_{IL}	V_{IL}	V_{IL}	V_{IL}(3)	V_{IH}(3)	V_{CC}	5.0V	03H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $11.5 \leq V_H \leq 13.0V$.
3. $A_1 - A_{12} = V_{IL}$.
4. With $V_{PP} \leq V_{CC}$ the 57F64 inhibits all erase and program functions.
5. $\overline{CE}$ controls the erase pulse width.

SIMILARITIES TO CONVENTIONAL MODES

The On-Board read, output disable, standby, and program/erase inhibit modes all operate identically to the conventional equivalent modes. See appropriate conventional mode sections for descriptions and details.

PROGRAM MODE

With the exception of V_{CC} specified at 5V, the On-Board program mode functions exactly like its standard EPROM counterpart. Programming with V_{CC} at 5V eliminates the need for dual V_{CC} power buses for in-circuit programming. Users of On-Board programming still enjoy all the benefits attributed to Intel's Quick-Pulse Programming algorithm. (See Figure 8. Quick-Pulse Programming Algorithm, and Figure 6. On-Board Programming/Verify Waveforms.)

PROGRAM VERIFY MODE

After completing each program pulse ($\overline{PGM}$ transition from logic 0 to 1), lower V_{PP} to 6.25V, raise $\overline{PGM}$ to V_H level (11.5V–13.0V), and set $\overline{OE}$ to V_{IL} to enter the program verify mode. Invalid data indicates the need for another program pulse; lower $\overline{PGM}$ from V_H to V_{IH} prior to raising V_{PP} to 12.75V. Valid data indicates completion of the programming loop.

The Quick-Pulse Programming algorithm (Figure 8) requires a final array verify after completion of byte programming. The system should verify the entire array with V_{PP} at 6V, and $\overline{PGM}$ at V_H.

FLASH-ERASE MODE

To select the Flash-Erase mode, set $\overline{CE}$ and $\overline{OE}$ to V_{IH}, V_{CC} to 5.0V, V_{PP} to 12.75V, and $\overline{PGM}$ to V_H (11.5V–13.0V). Toggle $\overline{CE}$ low for the predetermined erase pulse width. Note that $\overline{CE}$ controls the erase time in the On-Board mode, not $\overline{PGM}$. (See Figure 7. On-Board Erase/Verify Waveforms and Figure 9. Flash-Erase Algorithm.)

ERASE VERIFY MODE

To transition from Flash-Erase to erase verify mode, raise $\overline{CE}$ to V_{IH} for 1 μs, then lower V_{PP} below 2V, and $\overline{CE}$ to V_{IL} for 2 μs. Raise V_{PP} to the 3.5V erase verify level, place the address to be verified on the bus, and gate the data from the device outputs by lowering $\overline{OE}$ to V_{IL}. Continue checking through the array until an address does not verify, and then raise $\overline{CE}$ to V_{IH} to set up for the next erase pulse.

inteligent Identifier™ MODE

Board programmers can read the On-Board inteligent Identifier™ by setting V_{CC} and V_{PP} to 5.0V, A_1–A_{12} to V_{IL}, and $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ to V_{IL}. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer's code (89H) and byte 1 ($A_0 = V_{IH}$) represents the device identifier (03H).

Table 8. On-Board Program/Program Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$ (Notes 1, 2)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{CC4}	V_{CC} Program/Verify Current		30	mA	$\overline{CE} = V_{IL}$(4, 5, 6)
I_{PP4}	V_{PP} Program/Verify Current		30	mA	$\overline{CE} = V_{IL}$(4, 5, 6)
V_{CC4}	V_{CC} Program/Verify Supply	4.50	5.50	V	$\overline{CE} = V_{IL}$(5, 6)
V_{PP4}	V_{PP} Program Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(6)
V_{PPV4}	V_{PP} Verify Supply	6.0	6.5	V	$\overline{CE} = V_{IL}$(6)

A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
t_{AS}	Address Setup Time	2		µs	
t_{DS}	Data Setup Time	2		µs	
t_{VPS}	V_{PP} Setup Time	2		µs	
t_{CES}	$\overline{CE}$ Setup Time	2		µs	
t_{PW}	Program Pulse Width	95	105	µs	
t_{DH}	Data Hold Time	2		µs	
t_{VPH}	V_{PP} Hold Time from $\overline{PGM} = V_{IH}$	0		µs	
t_{MS}	Margin Setup Time	0		µs	
t_{OES}	$\overline{OE}$ Setup Time	2		µs	
t_{OE}	$\overline{OE}$ to Output Delay		150	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0			
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0	130	ns	(Note 3)

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns

Input Pulse Levels . . . . . 0.45V to 2.4V

Input Timing Reference Level . . . . . 0.8V and 2.0V

Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied to the 57F64 before V_{PP} and removed from the device after V_{PP}.
2. See Conventional and On-Board Read Operation D.C. Characteristics tables for I_{LI}, I_{LO}, V_{IL}, V_{IH}, V_{OL} and V_{OH} values.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven.
4. The maximum current value is with the outputs unloaded during verification.
5. This specification applies to both programming and verification.
6. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.

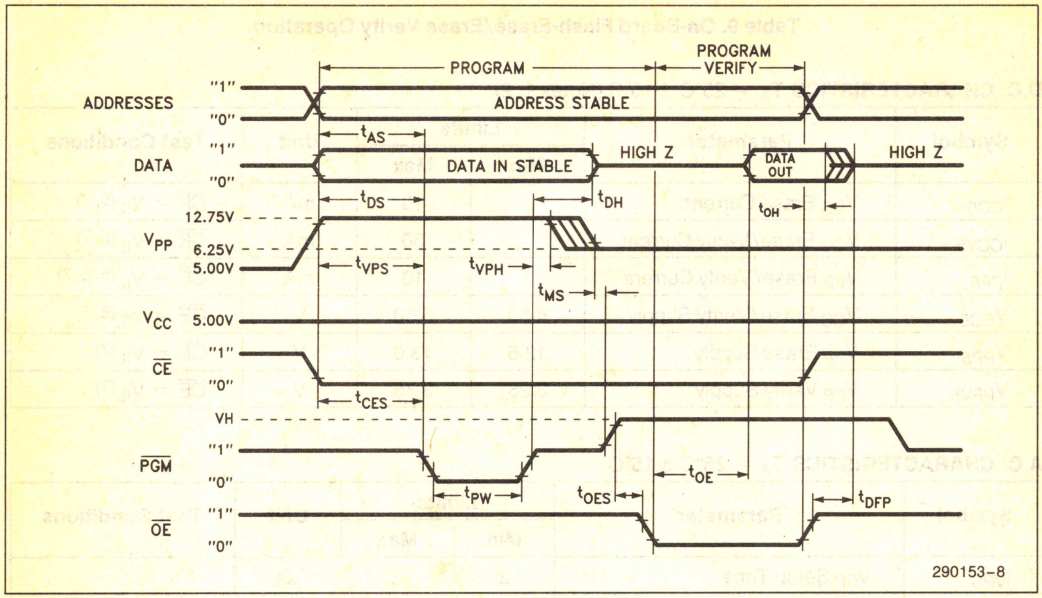


Figure 6. On-Board Programming/Verify Waveforms

Table 9. On-Board Flash-Erase/Erase Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$ (Notes 1, 2)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{CC5}	V_{CC} Erase Current		10	mA	$\overline{CE} = V_{IL}$(5, 7)
I_{CCV5}	V_{CC} Erase/Verify Current		30	mA	$\overline{CE} = V_{IL}$(5, 7)
I_{PP5}	V_{PP} Erase/Verify Current		10	mA	$\overline{CE} = V_{IL}$(5, 6, 7)
V_{CC5}	V_{CC} Erase/Verify Supply	4.50	5.50	V	$\overline{CE} = V_{IL}$(6, 7)
V_{PP5}	V_{PP} Erase Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(7)
V_{PPV5}	V_{PP} Verify Supply	3.25	3.75	V	$\overline{CE} = V_{IL}$(7)

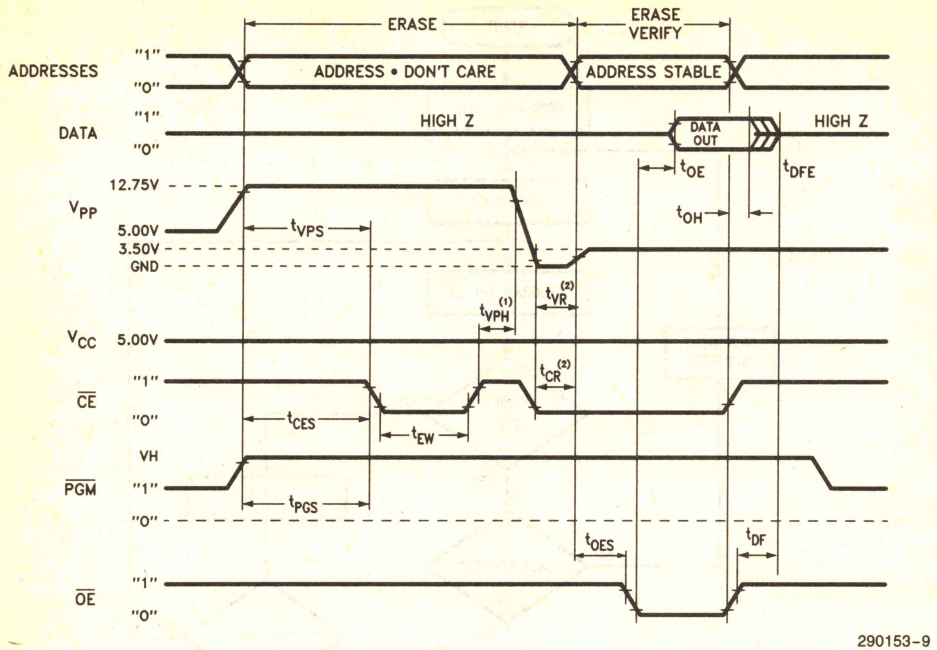
A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
t_{VPS}	V_{PP} Setup Time	2		µs	
t_{CES}	$\overline{CE}$ Setup Time	2		µs	
t_{PGS}	$\overline{PGM}$ Setup Time	2		µs	
t_{EW}	Erase Pulse Width	1	1855	ms	(Notes 3, 8)
t_{VPH}	V_{PP} Hold Time from $\overline{CE} = V_{IH}$	1		µs	
t_{VR}	V_{PP} Recovery Time	2		µs	
t_{CR}	$\overline{CE}$ Recovery Time	2		µs	
t_{OES}	$\overline{OE}$ Setup Time	2		µs	
t_{OE}	$\overline{OE}$ to Output Delay	150		ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0			
t_{DFE}	$\overline{OE}$ High to Output Float Delay	0	130	ns	(Note 4)

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied to the 57F64 before V_{PP} and removed from the device after V_{PP}.
2. See conventional and On-Board Read Operation D.C. Characteristics for I_{LI}, I_{LO}, V_{IL}, V_{IH}, V_{OL} and V_{OH} values.
3. Erase pulse width varies with pulse number. (See Flash-Erase algorithm).
4. This parameter is only sampled and not 100% tested.
5. The maximum current value is with the outputs unloaded during verification.
6. This specification applies to both programming and verification.
7. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.
8. $\overline{CE}$ controls the erase pulse width in the On-Board Flash-Erase mode.



NOTES:
1. Raise $\overline{CE}$ to complete the erase pulse prior to lowering V_{PP}.
2. V_{PP} and $\overline{CE}$ must be at V_{IL} at the same time, for a period of 2 μs.

Figure 7. On-Board Flash-Erase/Verify Waveforms

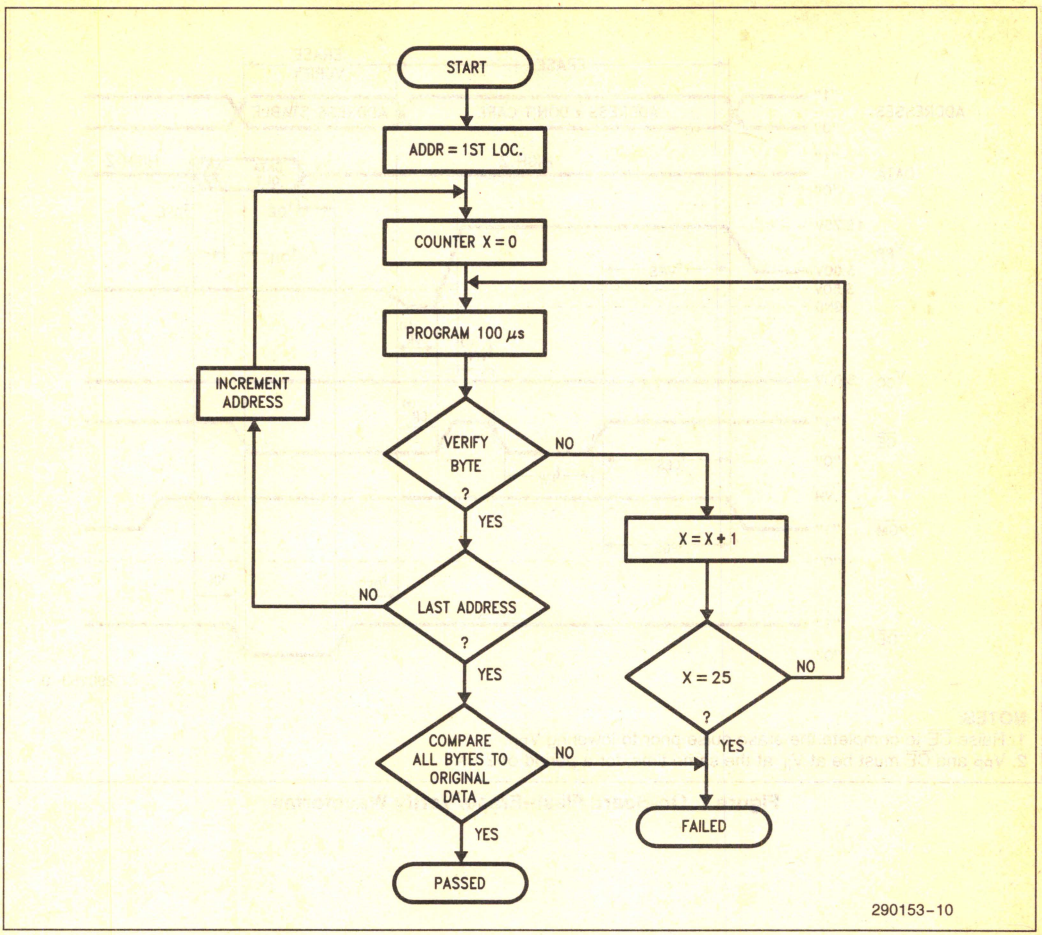
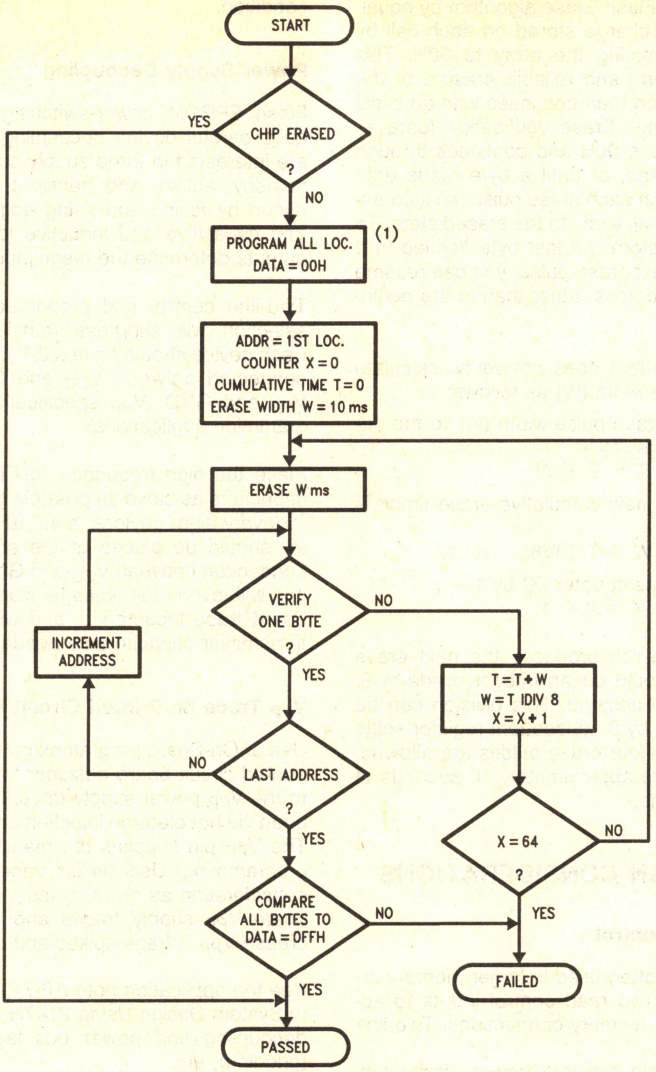


Figure 8. Quick-Pulse Programming™ Algorithm

QUICK-PULSE PROGRAMMING™ CHARACTERISTICS

The Quick-Pulse Programming™ algorithm specifies a higher V_{PP} voltage than the int$_e$ligent Programming™ algorithm to provide greater programming energy. This energy leads to faster device programming. A higher reference level checks cell margin and eliminates the time consuming over-program pulses. After entering the program mode, toggle $\overline{PGM}$ low for 100 μs, and immediately follow with a byte verification. The algorithm allows up to twenty-five program pulses per byte, although most bytes verify on the first or second pulse. When all bytes have been programmed, set V_{PP} or V_{CC} to its 6.0V final verify mode voltage. Compare all bytes to the original data to confirm proper programming. See Figure 8 for the Quick-Pulse Programming™ algorithm.

NOTE:
Use the program verify mode for this final verify. Choice of supply (V_{PP} or V_{CC}) depends on implementation. Use of the conventional program verify mode requires setting V_{CC} equal to 6.0V ±0.25V for final verify, use of the On-Board program verify mode requires setting V_{PP}.



NOTE:
1. Program the array using Quick-Pulse Programming™ algorithm.

Figure 9. Flash Erase Algorithm

FLASH-ERASE ALGORITHM

Intel's Flash-Erase algorithm enables efficient removal of charge from all bits in the array simultaneously. The algorithm erases the device for the minimum amount of time necessary to simulate U.V. erasure, by employing a closed-loop flow similar to Quick-Pulse Programming. Although the algorithm allows a maximum erase time of 10 seconds, erasure usually occurs within 1–2 seconds. This is three orders of magnitude faster than typical U.V. erase times.

Prior to erasing a device, you should check its present status. If it passes the erase verify test, go directly to code programming. Flash EPROMs leave

the factory in the erased state for your convenience. You must begin the Flash-Erase algorithm by equalizing the amount of charge stored on each cell by Quick-Pulse Programming the array to 00H. This provides for a uniform and reliable erasure of the array. Erase execution then continues with an initial erase pulse of 10 ms. Erase verification (data = FFH) starts at address 00H and continues through the array until the end, or until a byte reads data other than 0FFH. With each erase pulse, an increasing number of bytes will verify to the erased state. To improve efficiency, store the last byte verified in a register. After the next erase pulse, you can resume verification at that address rather than at the beginning of the array.

Upon finding a byte that does not verify, calculate the next erase pulse width (W) as follows:

a) add the current erase pulse-width (W) to the cumulative erase time (T)—
$$T = T + W;$$
b) integer divide the new cumulative erase time (T) by 8—
$$W = T \text{ IDIV8};$$
c) increment the pulse counter (X) by 1—
$$X = X + 1.$$

Note that step b, which produces the next erase pulse width (W), should be an integer divide-by-8, with the remainder truncated. This division can be easily accomplished by 3 subsequent register shifts right. A total of sixty-four erase pulses are allowed, which corresponds to approximately 10 seconds of cumulative erase time.

SYSTEM DESIGN CONSIDERATIONS

Two Line Output Control

Flash EPROMs are often used in larger memory arrays. Intel provides two read control inputs to accommodate multiple memory connections. Two-line control provides for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder output should enable $\overline{CE}$, while the system's read signal controls all Flash EPROMs and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low-power standby condition.

Power Supply Decoupling

Flash EPROM power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of Chip Enable. The capacitive and inductive loads on the device outputs determine the magnigtudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and GND, and between V_{PP} and GND (V_{PP} specifically in On-Board programming applications).

Place the high frequency, low inherent inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Use of On-Board programming features requires the printed circuit board designer to pay extra attention to the V_{PP} power supply trace. Flash EPROMs program via hot electron injection onto the floating gate. The V_{PP} pin supplies the memory cell currents for programming. Use similar trace widths and layout consideration as given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

See the application note AP-74, High Speed Memory System Design Using 2147H, for more details on decoupling and power bus layout considerations (gridding), etc.

Power Up/Down Sequencing

Upon powering up the 57F64, V_{CC} must reach its steady state value before raising V_{PP} to the 12.75V level. In addition, upon power down, V_{PP} must be at ground before lowering V_{CC}. Failure to follow either of the above sequences could inadvertently place the 57F64 into the Flash-Erase or Program mode.

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